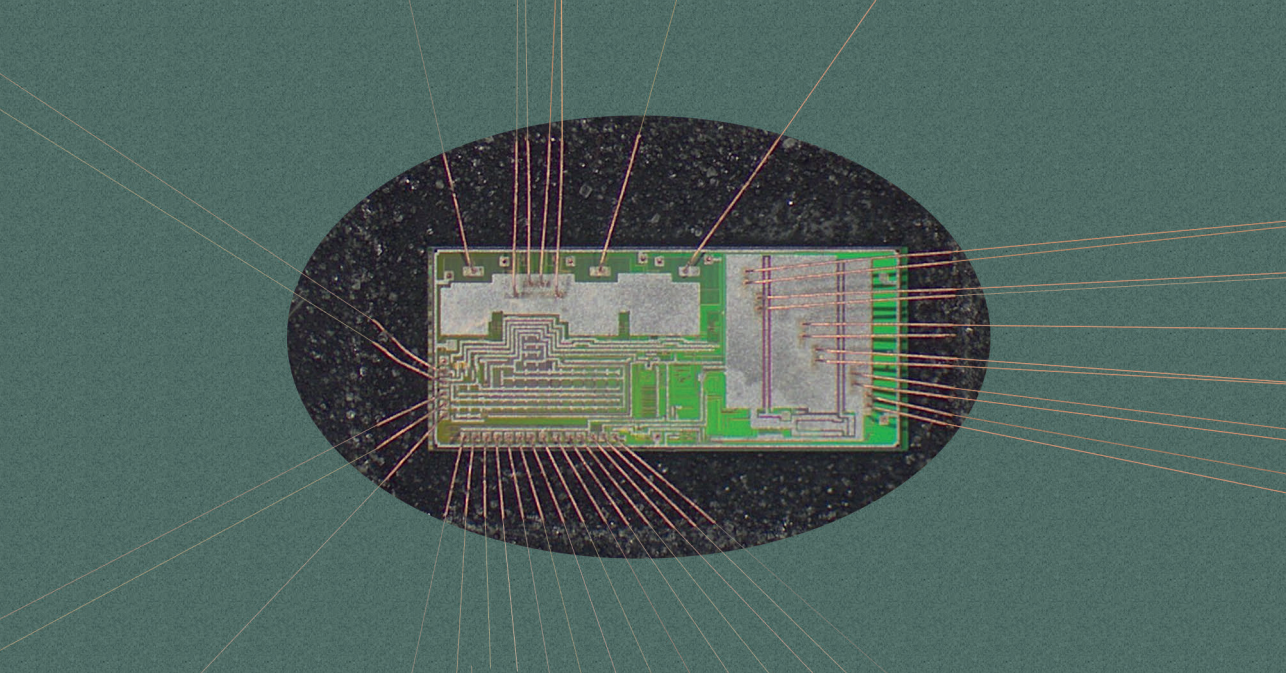




FAU Forschungen, Reihe B, Medizin, Naturwissenschaft, Technik 38

Alexander Schade

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**Physikalisch basierte Methodologie für den
EMV-konformen Entwurf und die
Verifikation von Automotive System ICs**

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der Friedrich-Alexander-Universität
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Abstract

In the recent decades, automotive electronics has undergone a rapid evolution towards highly complex multi-function chips. So-called Automotive System ICs can integrate multiple DC/DC-converters, a logic core, linear regulators, smart switches, sensor interfaces and transceivers on a single die. If electromagnetic compatibility (EMC) issues are discovered late, the complex investigations and the required rework can significantly prolong the time-to-market. Moreover, if the EMC is already improved on the chip level, less effort is required to achieve electromagnetic compatibility. The methodology developed in this thesis employs novel physically-based modeling techniques for IC-package and substrate parasitics. Furthermore, the modeling of inductances and RF-losses in on-die power routing were advanced in a proprietary BCD-technology. The presented modeling techniques cope with the accuracy requirements of EMC-simulations.

The requirements on IC-package models for the use in EMC-simulations go far beyond what is typically used in function verification. Mutual pin-loop inductances of three orders of magnitude below typical pin-inductances can already cause non-compliance with the EMC-requirements. It will be shown that, if magnetic shielding by the PCB-ground plane is neglected, errors in the predicted RF-emissions of the DC/DC-converter can be up to 19 dB. The presented novel approach can take a large number of small mutual pin-loop inductances into account at a high accuracy.

In this thesis, the inductances as well as the inductive RF-losses in the power routing will be quantified experimentally and reproduced by means of field simulation and parasitic extraction. In future high-frequency extensions of DPI-testing, internal resonances, the quality factor of which depends on the RF-losses, may increase in relevance. It was demonstrated how eddy-current losses in the metallization can be exploited to dampen these resonances.

Furthermore, in this thesis, a flexible substrate extraction tool is developed. It is distinguished by the fact that the precise semantics of the field model are transparent and available to the user. Moreover, a novel marker layer concept helps to precisely configure the model's level of detail. This marker layer concept and a novel 3D mesh compression technique (S-EHRFEM) helps to drastically reduce the simulator run time.

The developed test-IC contains a DC/DC-converter running at 3 MHz and a digital disturber clocked at 32 MHz, both of which can act as disturbance sources. The RF-emissions are evaluated at three different transceiver pins, in each case in the recessive and dominant bus state. In the complete frequency range from 3 MHz to 1 GHz, the simulations achieve a good accuracy in the prediction of the DC/DC's RF-emissions, with deviations typically less than ± 6 dB. The involved RF-coupling mechanisms are analyzed in detail. These discussions are enabled by an automated simplification using sensitivity analyses, and are based on low-dimensional substrate models, in which the n-buried layer is approximated as equipotential. Furthermore, various counteractive measures are tested and discussed. For example, it was experimentally verified that separating the digital from the system ground is highly effective, and can achieve reductions of 31 dB at 50 MHz and 15 dB at 300 MHz.

Kurzfassung

In den letzten Jahrzehnten hat die Elektronik in Fahrzeugen eine rasante Entwicklung in Richtung hochkomplexer multifunktionaler Chips durchlaufen. Sogenannte „Automotive System ICs“ können mehrere DC/DC-Wandler, einen digitalen Kern, Linearregler, intelligente Schalter, Sensorschnittstellen und Transceiver auf einem einzigen Chip integrieren. Wenn Probleme mit der elektromagnetischen Verträglichkeit (EMV) erst spät festgestellt werden, können die komplexen Untersuchungen und die erforderlichen Nachbesserungen die Markteinführung entscheidend verzögern. Außerdem wird weniger Aufwand benötigt, um elektromagnetische Verträglichkeit zu erreichen, wenn die EMV bereits auf der Chipebene verbessert wird. Die in dieser Arbeit entwickelte Methodik verwendet neuartige physikalisch-basierte Modellierungstechniken für IC-Gehäuse- und Substratparasiten. Des Weiteren wurden in einer proprietären BCD-Technologie die Modellierung von Induktivitäten und RF-Verlusten in der Leistungsverdrahtung auf dem Chip vorangetrieben. Die vorgestellten Modellierungsverfahren erfüllen die Genauigkeitsanforderungen von EMV-Simulationen.

Die Anforderungen an IC-Gehäusemodelle zum Einsatz in EMV-Simulationen gehen weit über das hinaus, was in der funktionalen Verifikation typischerweise verwendet wird. Gegeninduktivitäten von Pinschleifen, die drei Größenordnungen unterhalb der Eigeninduktivität liegen, können bereits zu EMV-Beeinträchtigungen führen. Es wird gezeigt, dass die Vorhersage von RF-Emissionen des DC/DC-Wandlers einen Fehler von bis zu 19 dB aufweisen kann, wenn die magnetische Abschirmung durch die PCB-Massefläche vernachlässigt wird. Der vorgestellte neuartige Ansatz kann eine große Anzahl kleiner Gegeninduktivitäten von Pinschleifen mit hoher Genauigkeit berücksichtigen.

In dieser Arbeit werden die Induktivitäten sowie die induktiven RF-Verluste in der Leistungsverdrahtung experimentell quantifiziert und mittels Feldsimulation und Parasitenextraktion nachgebildet. In zukünftigen Hochfrequenzerweiterungen des DPI-Tests könnten interne Resonanzen, deren Resonanzschärfe von den RF-Verlusten abhängt, an Bedeutung zunehmen. Es wird demonstriert, wie Wirbelstromverluste in der Metallisierung genutzt werden können, um diese Resonanzen zu dämpfen.

Des Weiteren wird in dieser Arbeit ein flexibles Substratextraktionswerkzeug entwickelt. Dieses zeichnet sich besonders dadurch aus, dass die genaue Semantik des Feldmodells transparent und dem Benutzer zugänglich ist. Außerdem dient ein neuartiges Markierebenenkonzept dazu, den Detaillierungsgrad des Modells genau zu kontrollieren. Dieses Markierebenenkonzept sowie eine neuartige Kompressionstechnik für 3D-Netze (S-EHRFEM) erlauben es, die Simulatorlaufzeit stark zu reduzieren.

Der entwickelte Test-IC enthält einen DC/DC-Wandler (betrieben mit 3 MHz) und einen digitalen Störer (betrieben mit 32 MHz), welche beide als Störquellen wirken können. Die RF-Emissionen werden an den drei unterschiedlichen Transceiverpins evaluiert, jeweils im rezessiven sowie im dominanten Buszustand. Im gesamten Frequenzbereich von 3 MHz bis 1 GHz erreichen die Simulationen der RF-Emissionen des DC/DC-Wandlers eine gute Genauigkeit, mit Abweichungen typischerweise unterhalb ± 6 dB. Die beteiligten RF-Kopplungsmechanismen werden im Detail ana-

lysiert. Diese Diskussionen werden durch eine maschinelle Vereinfachung mittels Sensitivitätsanalyse ermöglicht, und sie bauen auf niedrigdimensionalen Substratmodellen auf, in welchen die n-Epitaxieschicht als Äquipotentialfläche angenähert wird. Außerdem werden verschiedene Gegenmaßnahmen getestet und diskutiert. Zum Beispiel wurde durch Experimente bestätigt, dass eine Abtrennung der Digitalmasse sehr effektiv ist, und eine Emissionsreduktion von 31 dB bei 50 MHz und 15 dB bei 300 MHz erzielen kann.

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List of Abbreviations

ABS	Anti-lock Braking System
ASIC	Application-Specific Integrated Circuit
ATL	Artificial Thin Layer
BCD	Bipolar-CMOS-DMOS
BDF	Backwards Differentiation Formulae
BEM	Boundary Element Method
CAD	Computer-Aided Design
CAN	Controller Area Network
CEFU	Central Functions
CLI	Capacitive-Layer Impedance
CMOS	Complementary Metal-Oxide-Semiconductor
DMOS	Double-diffused Metal-Oxide-Semiconductor
DPI	Direct RF-Power Injection (IEC 62132-4)
DUT	Device Under Test
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EM	Electromagnetic
ESD	Electrostatic Discharge
ESL	Equivalent Series Inductance
ESP	Electronic Stability Program
ESR	Equivalent Series Resistance
FDM	Finite Difference Method
FEM	Finite Element Method
FFT	Fast Fourier Transform
FLOP	Floating Point Operation
GSG	Ground-Signal-Ground
GS	Ground-Signal
HDL	Hardware Description Language
HV	High Voltage
IBF	Interface Basis Function
IC	Integrated Circuit
IRQ	Interrupt Request
LDMOS	Laterally-Diffused Metal-Oxide-Semiconductor
LDO	Low-Dropout Regulator

LIN	Local Interconnect Network
LQFP	Low Profile Quad Flat Package
LTE	Local Truncation Error
LTi	Linear Time-Invariant
LVS	Layout Versus Schematic
LV	Low Voltage
MIS	Metal-Insulator-Semiconductor
MNA	Modified Nodal Analysis
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPBF	Mesh Point Basis Function
MV	Medium Voltage
NMOS	N-type Metal-Oxide-Semiconductor
OTA	Operational Transconductance Amplifier
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCCD	Prescribed Constant Current Density
PCD	Prescribed Current Density
PCV	Prescribed Constant Voltage
PDE	Partial Differential Equation
PLL	Phase-Locked Loop
PMIC	Power-Management Integrated Circuit
PMOS	P-type Metal-Oxide-Semiconductor
PSS	Periodic Steady State
PV	Prescribed Voltage
PWC	Piecewise Constant
PWL	Piecewise Linear
PWM	Pulse-Width Modulation
RF	Radio Frequency
RLCG	Series Resistance (R), Series Inductance (L), Shunt Capacitance (C), Shunt Conductance (G)
RLCK	Resistance (R), Inductance (L), Capacitance (C), Inductive Coupling Coefficient (K)
RMS	Root-Mean-Square
RTL	Register-Transfer Level
SBC	System-Basis-Chip
SMD	Surface-Mounted Device
SOI	Silicon-on-Insulator

SOLT	Short, Open, Load, Thru
SPI	Serial Peripheral Interface
SoC	System-on-a-Chip
TEM	Transverse Electro-Magnetic
V2I	Vehicle-to-Infrastructure
V2V	Vehicle-to-Vehicle
VCVS	Voltage-Controlled Voltage-Source
VNA	Vector Network Analyzer

CHAPTER 1

Introduction

1.1 Automotive Electronics and EMC

Many recent key improvements in fuel-efficiency, increased safety, eco-friendliness and driver convenience were achieved by advancements in car electronics. In the course of this development, the amount of electronic components in cars, as well as the integrated circuit complexity has increased sharply. Current and future Advanced Driver Assistant Systems (ADAS), such as Autonomous Emergency Brake Assist (AEB) or the use of vehicle-to-vehicle/infrastructure communication (V2V, V2I), will continue this trend [9], [55], [130]. This thesis is concerned with Automotive System ICs, which are among the most complex Smart Power ICs designed for automotive applications. Automotive System ICs can contain step-up and step-down DC/DC-converters, post-regulating LDOs, digital supervision functions, an SPI-interface, smart switches, sensor interfaces, and multiple transceivers for automotive buses. These functions are usually integrated on a single die. Moreover, many customers nowadays demand Smart-Power System-On-a-Chip solutions tailored towards their next generation product – so-called Application-Specific Integrated Circuits (ASIC).

The rapid design cycles of Automotive System ICs and the related Smart-Power ASICs requires the use and assembly of pre-developed circuit modules. Nevertheless, the integration of multiple different modules on a single die is a highly involved task in itself. One of the key challenges is to ensure that the electromagnetic compatibility (EMC) requirements are fulfilled [81], [199]. For example, digital cores and DC/DC-converters can be a potent source of electromagnetic interference [104]. On the other hand, automotive buses such as LIN, CAN and FlexRay, which are directly interfaced with pins of Automotive System ICs, place very rigorous limits on the RF-emissions [10], [127], [186]. These limits are motivated by the fact that the cable harness, which interconnects the Electronic Control Units (ECUs) [20], [151] can distribute or radiate this interference, which can disturb radio communication. EMC is subject to a large number of international standards and laws, a complete coverage of which would be far beyond the scope of this work [21, Ch. 3, Ch. 5]. Since it is of great interest to the IC manufacturer that its product can be used to build cost-optimized yet EMC-compliant systems, IC manufacturers are usually involved with designing for EMC-compliance. One approach for the EMC-testing of ICs is the use of international standards specifically developed

for integrated circuits, such as IEC 62132-4 (direct RF power injection – DPI) or IEC 61967-4 (150 Ohm method). In contrast to the testing according to the requirements of ECUs (ISO 11452-2, CISPR-25) [21, Ch. 9], these standards have a higher and application-independent reproducibility, and the modeling of IC-external system is strongly simplified [103].

Pre-silicon predictability and ensuring compliance with the EMC requirements by design is certainly the “holy-grail” of EMC in IC-design. Besides that, it is also important to estimate the EMC early in the concept phase, where critical decisions are made that affect the EMC. Moreover, if an EMC-requirement violation is detected experimentally, there is strong need to analyze this issue quickly and precisely, such that it can be safely resolved in the next tape-out. Models capable of predicting the EMC can be extremely complicated, and often require that substrate-, package- and PCB-parasitics are accounted for with a very high accuracy. Another practical barrier is the large number of potentially relevant effects and coupling paths, a relevance differentiation among which is most complicated.

The semiconductor technologies used for today’s highly-integrated Automotive System ICs are significantly different from the Smart Power technologies of the previous IC-generations [6], [156]: Leading-edge BCD-technologies facilitate placing separate functional modules on a single die, feature multiple metal layers, use low-current-bias CMOS OTAs located in a single n-epitaxial pocket, and are based on deep trench isolation. Therefore, previous scientific analyses of the EMC of Smart Power IC is only partly transferable [169]. Automotive System ICs are also very different from microcontrollers: This is due to the fact that their logic gates reside on top of a low-ohmic n-buried layer, a very low-ohmic power metallization is available and IC-pins can drive switching currents of multiple amperes. Thus, also prior research into the EMC of microcontrollers or mostly-CMOS low-power SoCs [26] is only not fully applicable to Automotive System ICs. This motivates the aim of this work, which is to develop a methodology for the EMC-compliant design and verification that can handle Automotive System ICs. The EMC-models developed in this thesis are physically-based and computer-generated.

Since to date, the EMC test methods for ICs in IEC 62132-4 and IEC 61967-4 are limited to 1 GHz, this thesis is mainly concerned with this frequency range. Extending the developed methodology beyond 1 GHz requires modifications, which will not be thoroughly elaborated.

1.2 Smart Power ICs and BCD-Technologies

Semiconductor industry is well known for its decade-long, rapid progress in miniaturization of MOSFETs, also known as “Moore’s Law”. Moore’s law

also strongly affected the evolution of power electronics. In the mid-eighties, advancements in micro-lithography led to the integration of CMOS-logic into power bipolar technologies. In the same decade, DMOS transistors, a kind of power-MOSFET, started to outperform power bipolar transistors in some applications, which was also enabled by increasingly fine lithography. Adding DMOS transistors to technologies that integrate CMOS with bipolar devices came only at a small extra cost because many dopant profiles could be shared with CMOS and bipolar devices. This was the genesis of *Bipolar-CMOS-DMOS semiconductor technologies*, also known as *BCD-technologies*. [6], [156]

BCD-technologies enable the integration of power electronics, such as voltage regulators and motor drivers, with sophisticated self-diagnosis and safety functions, as well as with digital logic. Such integrated circuits, which are also known as *Smart Power ICs*, can be superior to multi-chip solutions in terms of power consumption, power efficiency, fail-safety and form factor: For example, Automotive *System Basis Chips* nowadays feature a stand-by mode, in which the power consumption is reduced to as little as 15 – 25 μA [90], and DC/DC-converter efficiency was strongly improved due to reduced parasitics in the path to the DMOS gates [22]. Integrated diagnostic and autonomous logic functions enable fail-safety of smart switches in case of over-temperature, overload or short circuit [63]. Form factor improvements refer to the size reduction of IC-packages, which became possible due to reduced power dissipation, and by integrating multiple functions on the same die [63].

BCD-technologies have undergone a rapid change between the mid-eighties and around the year 2010. A shrinkage of the minimum line width from 4 μm to roughly 0.1 μm has led to strong performance improvements of the DMOS transistors, and to a more than thousandfold increase of CMOS logic density. Already in the mid-nineties, DMOS transistors had superseded bipolar transistors in most applications, and in state of the art BCD-technologies, bipolar transistors are considered outdated. Moreover, BCD-technologies have seen a shift in the way power devices are isolated from each other. Modern BCD-technologies mostly use *deep trench isolation* instead of *junction isolation* for vertical isolation, and some use *silicon on insulator* (SOI) instead of highly doped buried layers for lateral isolation. A benefit of SOI for the EMC is that SOI strongly suppresses parasitic substrate couplings. Albeit SOI is also advantageous in other respects, only few vendors have adopted it, because of manufacturing difficulties and because heat dissipation is impaired. [6], [156]

Since around 2010, the structure minimization in BCD-technologies have stagnated, in contrast to pure CMOS technologies. This is due to the fact that DMOS transistors do not benefit from minimum line width reductions below

100 nm: While a further shrinkage would allow more logic to be integrated, it would also unnecessarily increase the costs per square millimeter for the power part. Thus, further miniaturization is considered uneconomical. [156]

Smart Power ICs are a vast topic. This work concentrates only on subset, which is known as *System ICs* or *Smart Power SoCs* [36], [63], [166]. They are highly-integrated multi-function ICs, implemented in modern MOSFET-centered BCD-technologies, for example:

- *Power-Management ICs (PMIC)*: They typically contain a step-up¹ and a step-down DC/DC-converter, as well as multiple post-regulating LDOs. Standard features are a watchdog mechanism and an in-built register bank that is read and written via SPI. [89]
- *System Basis Chips (SBC)*: SBCs can be understood as an extension of PMICs that additionally include, e.g., CAN- or LIN-transceivers. Depending on the required power output, they may also contain DC/DC converters. [90], [91]
- *Engine Management System ICs*: ICs tailored to the needs of automotive engine management systems. They function as a kind of SBC and additionally contain, for example, low-side switches, half bridges, ignition drivers and hall sensor interfaces. [88]

An in-depth description of internal functioning of System ICs is found in sec. 2.1, and the BCD-technology used in this thesis is further described in sec. 2.2.

1.3 The Development Process of ICs and the Involvement of EMC

There are different project management approaches for IC development: They all have in common that their starting point is the *definition stage* [52]. Here, the *functional system requirements* are fixed [48]. Furthermore, in the definition stage, decisions are made regarding the IC-package and which semiconductor technology will be used. After the definition stage, the project development commences (development stage). Depending on the project management approach, a project may undergo multiple development stages, each of which is followed by the production of IC-samples. The system definition is *not* allowed to change in subsequent development stages. This is due

¹ The step-up converter is used only in the corner case in which the battery voltage is temporarily reduced.

to the high development costs associated with altering fundamental system requirements or the IC-package.

It is important to understand the implications of this process: Since the IC-package is decided at the very beginning, for example, the ground-pinning, the die thickness and the die-backside connection is mostly fixed. Also, since pin placement entail circuit module placement, their location on the die is already very constrained. Since these degrees of freedom are relevant for the EMC, already in the definition and concept phase, EMC-considerations should be included.

Similar to functional requirements, the EMC requirements are fully specified at the definition stage. However, in the case of EMC requirements, it has proven far more difficult to deduce concrete implications on the circuit-design and -layout. This is due to various practical barriers: For example, the EMC is influenced by the complex interplay of parasitic effects, which arise from multiple domains, e.g. RF-modeling, PCB-layout, IC-package and substrate parasitics. Moreover, there is often a large number of potentially relevant effects, in combination with a large number of susceptibility and emission measurements. Traditional approaches for EMC-compliant IC-design are rather heuristical. For examples, some approaches attempt to extrapolate observations from prior designs, and if EMI-issues are expected, they are countered by, e.g., simply increasing the distance between circuit modules. Other approaches rely on very specific knowledge that was gained by past efforts in improving the EMC. These methods, however, rely more on human experience rather than on machine-readable representations, and thus do not scale well with complexity. Moreover, simple models gained from case studies often have only limited generality, which makes their prediction considerably uncertain. Thus, if the analysis of such a model calls for design changes that are in conflict with production costs, project managers are often reluctant to implement these adaptations.

1.4 Goals and Structure of this Thesis

The goal of this thesis is to develop a methodology for EMC-compliant design and verification of Automotive System ICs. This thesis puts an emphasis on computer-supported methods, in order to overcome the complexity challenges of System ICs as well as the uncertainties of prior EMC engineering approaches: The focus on automation is leaned upon approaches that are already well-established in the field of functional verification [132]. For example, functional verification aims to execute a large number of fully-automated test benches in order to cover the large number of test cases and modes of operations [113]. The EMC-models developed in this thesis account for a large

number of potentially relevant parasitics, and are automatically generated by software. The development of such tools requires a deep understanding of the effects implicated in EMC-violations of System ICs, which shall be advanced in this thesis: Within this thesis, the EMC-models shall fulfill the following requirements:

- **Ab-initio, physically-based and fit for pre-silicon analysis:** Computer-based tool flows used for obtaining simulatable models should be derived *from the design data only* and *using physical laws only*. Otherwise strong modeling assumptions would be required, which is unreliable before silicon testing.
- **Accurate and tailored towards EMC:** Simple schematic-based models, e.g. as used for functional verification, often neglect effects relevant for EMC.
- **Numerically Stable:** Analog circuit simulation uses numerical algorithms. A model which is numerically ill-defined model or which violates conservation laws can lead to simulator failures.
- **Computationally Efficient:** Since an increased time per simulation run cannot be easily improved by supercomputing due to Amdahl's law, the models must be sufficiently efficient in themselves when subject to the numerical analyses.

In addition, the employed simulation technique and specifics about their implementation play a vital role in the computational efficiency [17], [56], [119], [121], [147], [202]. The methodology presented in this thesis is mainly geared towards AC-analysis and RF-simulation techniques [109], [111], [114], but also transient simulation is supported.

Chapter 2 summarizes the background knowledge about the design of automotive System ICs, the simulation and modeling techniques and the EMI-receiver according to CISPR-16-1-1. In chapter 3, a modeling method for IC-packages, tailored to the accuracy needs of EMC-simulations, is developed. Furthermore, test-wafers were developed in the course of this thesis, with the aim to probe the high-frequency physics of the on-die ground and power supply network. The results are presented in chapter 4. Moreover, chapter 4 explains how RLCK parasitic extraction tools are properly evaluated and used in EMC-simulations. Chapter 5 describes how the substrate should be modeled, and the path towards a suitable balance between accuracy and efficiency is set out. On the one hand, the low-dimensional substrate models described in sec. 5.1 provide the highest level of abstraction. They can facilitate the construction of simplified circuit models for pencil-and-paper calculations

with surprisingly good accuracy. On the other hand, the developed substrate extraction tool (sec. 5.2) covers a more broad range of effects, yet these models are still amenable for AC-simulations of complex IC-layouts. Finally, a test-IC that resembles an Automotive System IC was developed, in which the RF-emissions at transceiver pins are predicted and measured. These investigations, which evaluate the developed physically-based methodology, are presented in chapter 6. Additional topics in chapter 6 include a feasibility study of various *counter-measures* targeting the disturbance coupling path, as well as useful insights about the leading-order EMI coupling mechanisms, which are useful in the concept phase.

CHAPTER 2

Technological State of the Art and Theoretical Background

2.1 Description of Modules used to Build Automotive System ICs

This section discusses the features and the architecture of today's Automotive System ICs, and relate them to the underlying electrotechnical and economical constraints. Furthermore, it is elaborated how the mitigation of ground bounce and inductive pin-couplings is subject to economical trade-offs, and may require additional ground pins, additional circuitry and changes in the power routing.

A rather simplistic exemplary schematic of an Automotive System IC is shown in fig. 1. Pins that carry a high current may be double-bonded or might even be duplicated, e.g. VBAT, BSW and BGND. The basic building blocks of Automotive System ICs are the “central functions”, the “pad-row”

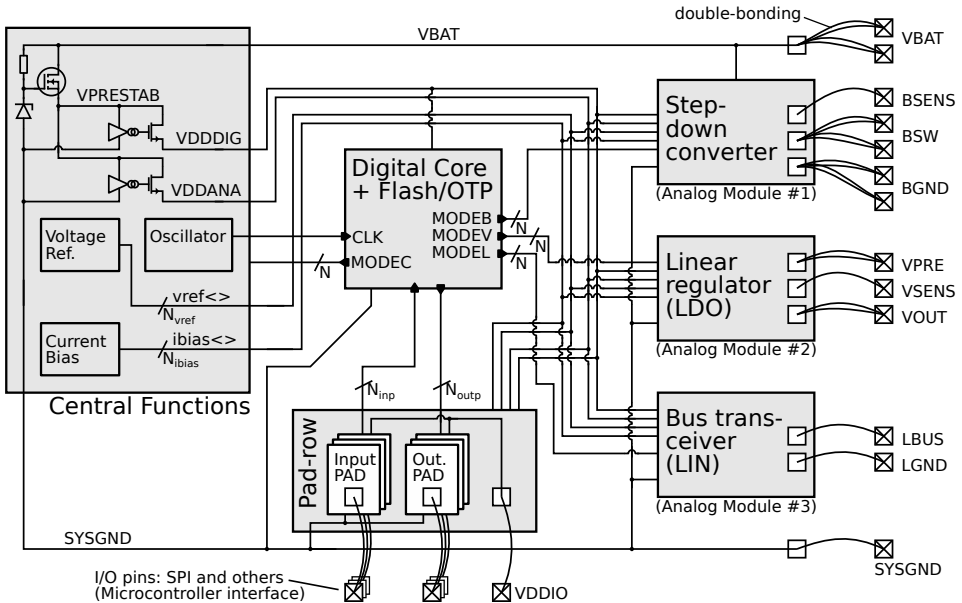


Figure 1: Explanatory illustration of an example Automotive System IC. Depending on the functionality, the number and the type of analog modules varies (here: module #1: DC/DC, module #2: LDO and module #3: LIN).

and the “digital core”. In addition, Automotive System ICs contain a number of purpose-specific analog modules [144]. ESD diodes are not depicted in fig. 1, despite they might have an influence on the EMC. The central functions module contains voltage-, current- and frequency-reference generators as well as internal voltage regulators. They are shared among all analog modules, the digital core and the pad-row. The pad-row implements digital I/O-pads [197] for 3.3 V or 5 V logic signals that are local to the ECU, e.g. an SPI-interface with a microcontroller. The digital core contains clock-synchronous and combinatory logic, registers and possibly flash- or OTP-memory [197]. IC-pins can either be dedicated to a module, or they can be shared among multiple modules, as for instance VBAT and SYSGND in fig. 1. In the following, different kinds of modules will be examined in detail.

Central Functions Module (CEFU) The 12 V vehicle power standard provides a battery voltage which is much too high for today’s highly-integrated digital and analog circuits. Therefore, Automotive System ICs which are directly powered from the battery require integrated regulators for internal low-voltage supplies. There must be at least two voltage levels (VDDDIG, VDDANA in fig. 1) because analog circuits require more headroom [149] and, hence, a higher supply voltage. In real ICs, typically there is a much larger number of system-level power domains than shown in fig. 1, some of which are powered down depending on the operating state (wake, standby, etc.).

The CEFU’s voltage regulators are typically two-stage, with a simple pre-regulator providing a pre-stabilized voltage VPRESTAB. Without pre-regulator, the internal VDDDIG and VDDANA regulators would have to tolerate a large voltage dropout because automotive standards entail that the device must withstand large transient pulses at the battery voltage pin of e.g. 45 V [63]. This requirement would lead to a strong increase in their silicon area. System level power domains like VDDDIG and VDDANA are always referred and stabilized to the system ground (SYSGND). Since large on-chip bypass-capacitors [197] are rather costly, these integrated voltage regulators usually *do not only* rely on capacitors for stabilizing the output. Rather, beyond the cutoff frequency of their OTA, they may exploit the source-follower behavior of their pass device [18], [39], and only at considerably higher frequencies, the on-chip bypass-capacitor becomes relevant. This is important for understanding their output impedance characteristic. Such system level power domains can typically provide DC currents of up to a few ten milliamperes.

The voltage regulators for VDDDIG and VDDANA require a precise reference voltage, such as from a bandgap reference circuit [39], [149]. In order to avoid unnecessary redundancy, the CEFU distributes various reference voltages ($v_{ref<>}$ in fig. 1), which are derived from its bandgap, among other modules.

Analog circuits like OTAs additionally require current biasing. For this purpose, the CEFU module typically also contains a PVT¹-compensated [149] reference current generator. N_{ibias} reference currents are distributed on the system level by the $\text{ibias}\langle\rangle$ -wires, where each wire carries a precisely known DC-current. These bias currents are in the order of micro-amperes [36]. Finally, the CEFU also generates a clock signal at the greatest accuracy feasible using an electronic oscillator, which is used as master clock of the digital part. Some digital cores may divide the clock signal and re-distribute it to some analog modules, which may require it for charge pumps, chopped OTAs, switched capacitor circuits [149] or to realize precise timing.

In general, the components of the CEFU realize a kind of bootstrapping mechanism, by providing “clean” power supplies and precise references, from a “dirty” battery voltage and in the presence of strong temperature and semi-conductor process variations. These components are needed by almost every analog module, and by sharing them, expensive “silicon real-estate” is saved. Components of the CEFU are never interfaced directly to IC pins.

Pad-Row Block Communication with digital ICs located on the same ECU requires a multi-pin digital interface. Such digital input, output and bidirectional pins are each bonded to an I/O-pad [197] in the pad-row. These pad drivers amplify and level-shift the low-power internal digital signals for external circuits. Input-pads feature Schmitt-triggers, which provide suitable logic rise and fall times and ensures signal integrity, and optional features of output-pads are tri-state, pull-up and pull-down modes [197]. The pad-row is typically supplied by an external I/O-voltage (VDDIO) [88] which may also be shared with other modules [90]. The N_{inp} input signals and the N_{outp} output signals on the (VDDDIG, SYSGND)-power-domain are directly connected between the digital core and the pad-row. The digital core may then gate, latch or otherwise process this information, and then forward it to analog modules. Similar to analog modules, the circuitry of the I/O-pads typically requires biasing-currents, a reference voltage and the VDDANA supply.

Digital Core and Flash/OTP The digital core contains synchronous and combinatory logic, and is synthesized from a RTL-description written in a Hardware Description Language (HDL) like Verilog. In contrast to the analog modules, its circuit synthesis and layout is done in a fully automated way, for example using standard cell based design [197]. It internally consists of multiple modules as well, and each analog module typically has a counterpart inside the digital core. Despite this block structure is also very important for the structuring of the implementation, it has no implications on the IC's

¹ Process, Voltage and Temperature

internal analog-electronic characteristics, and it is therefore not considered in the following.

The main task of the digital core typically consists of managing the SPI-communication, storing trimming values, maintaining a state machine for the operation mode (wake, sleep, etc.), implementing watchdog functions, and realizing the proper power-up sequence [38], [90]. In addition, the digital part takes part in the built-in self-test and in erroneous state handling, such as over-voltage treatment and safety shutdowns (fail-safe behavior). It can signal anomalies to an external logic IC via IRQs, which then reads the error code via SPI [90]. Some digital cores may even be customer-programmable. The digital core interfaces with the analog modules and with the CEFU using many point-to-point digital connections on the (VDDDIG, SYSGND)-power-domain. For example, the connection to the DC/DC-converter (MODEB) might be about $N = 30$ bits wide, not accounting for additional wires for built-in self test.

The flash- or OTP-memory is, strictly speaking, not part of the digital core, and it is not synthesized using the standard-cell approach. Rather, it might be considered as an analog module. For clarity however, fig. 1 depicts it as a part of the digital part, and omits the higher-voltage power domains, reference voltages and biasing currents it requires.

The digital part has a comparatively high DC current consumption and its synchronous logic emits very sharp current spikes [70, Ch. 4] towards power and ground. As will be elaborated in the next paragraph, this can lead to an detrimental ground offset between SYSGND and the PCB-ground, which is implicated in RF-emissions and in the degradation of IC-input signals. Despite a dedicated digital ground pin might mitigate this, such a pin is typically not realized. This is because it entails a large number of additional level shifters², as well as duplications of parts of the CEFU, which will also be elaborated further in the next paragraph.

Analog Modules by the example of the Step-down converter Fig. 2 shows a simplified schematic of the internals of an analog module: A synchronous step-down converter with an integrated high-side (MH) and low-side (ML) power MOSFET, operating from the battery voltage VBAT [8]. The regulation loop and control circuit senses the output voltage via the signal FEEDBACK, and makes binary decisions when to open MH or ML. The resulting signals HSON and LSON on the (SYSGND, VDDDIG)-domain then trigger actions of the rather complex low-side and high-side gate driver circuitry. (Power, ground, voltage reference and current-bias connections of the high side driver, the generation of FEEDBACK from BSNS, and ESD diodes are

² The use of level shifters at the interface to the digital core is further elaborated in sec. 6.2.

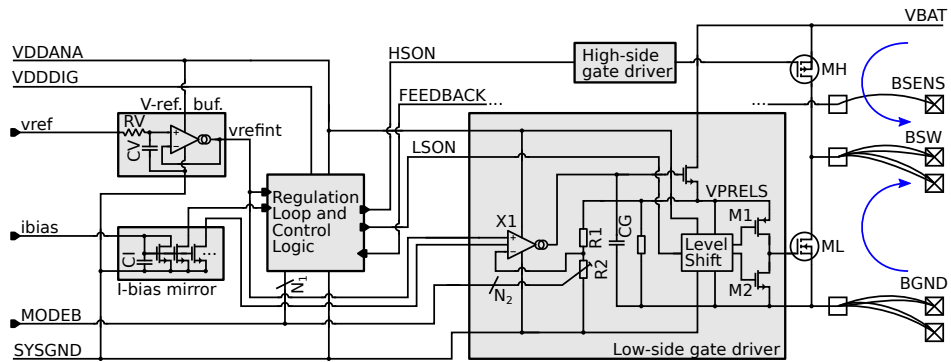


Figure 2: Highly simplified schematic of a step-down DC/DC-converter module in an Automotive System IC. Blue arrows indicate large-amplitude current loops over the bond wires and the lead-frame occurring during its operation.

not shown for clarity.) Realistic DC/DC-converters may additionally include over-current- and over-temperature-protection and slew-rate control circuits.

DC- and AC-currents through a module's SYSGND-connection lead to a static and dynamic voltage drop, respectively. This undesirable effect is known as ground bounce [42], [94], [115]. A distinction must be drawn between the "global" ground offset between SYSGND and the PCB-ground³ and the "local" ground offset of individual modules relative to the CEFU. Both are caused by inductances and resistances in the ground path. The impact of the global ground bounce is a degradation of signals which cross over from the PCB to the IC. For example, the regulator feedback VSENS in fig. 1 can be affected, and SYSGND-transients larger than the Schmitt-trigger hysteresis can disturb digital input pads. Moreover, the global ground bounce also plays an important role in RF-emissions via the substrate, as will be show in sec. 6.7. Conversely, a local ground bounce between modules and the CEFU degrades the accuracy of the reference voltage signals. If the DC part of this local ground bounce is small, it is easily eliminated by means of a simple RC low-pass filter in each module – for example see CV and RV in fig. 2. This is different from the global ground bounce: E.g. VSENS cannot be strongly low-pass filtered because it carries information in a non-zero bandwidth. Moreover, in contrast to the global ground bounce, the module/CEFU ground offset can be somewhat mitigated by independent routing all module's SYSGND connections to star-point located at the CEFU. Note that star-point routing does *not* reduce the module's own CEFU-ground offset, but it reduces the CEFU-ground offset caused in other modules.

³ That is the voltage drop across the SYSGND bond wire and lead frame parts.

A counter-measure against global SYSGND bounce is the reduction of the SYSGND current, by introducing module-dedicated ground pins. Step-down converter modules, such as in fig. 2, which are designed for output currents in the order of few amperes, are typically equipped with dedicated power ground pins (here: BGND) [91]. Sourcing the power current from BGND helps to keep the DC-currents and AC-current emissions through SYSGND at a lower level. However, beware that, due to substrate coupling, the separation of multiple ground nets is far from perfect at high frequencies (e.g., see sec. 6.7). One should, thus, *not* presume that the global SYSGND bounce can be predicted using simple schematic-level simulations. Also note that the close proximity of the VBAT, BSW and BGND pins reduces the volume of space penetrated by the AC magnetic field, which is induced by the pin-currents (blue arrows in fig. 2). Hence, inductive cross-talk to bond wires and lead-frame parts that belong to other analog modules is diminished, which is another advantage of dedicated ground pins. As will be shown in sec. 6.5.1, this inductive cross-talk is also heavily implicated in RF-emissions of DC/DC-converters.

However, adding dedicated ground pins is often a trade-off between costs and benefits. The costs of dedicated ground pins do not only consist of the increased packaging costs alone. In addition, a separate ground entails additional internal voltage regulators, level-shifters and sometimes even additional voltage references. For example, since the dynamic voltage difference between BGND and SYSGND can be in the order of volts, VDDANA, which is stabilized to SYSGND, cannot be used to drive the gate of ML in fig. 2. Therefore, the OTA X1, the voltage divider R1/R2 and the pass device are needed to generate a BGND-based power domain VPRELS. Moreover, additional level shifters are needed to translate logic signals from the (SYSGND, VDDANA)-domain to the (BGND, VPRELS)-domain. Note that X1 and R1/R2 regulate VPRELS using a reference voltage based on SYSGND, whereas the gate of the pass device is stabilized to BGND for high frequencies using the capacitor CG. Therefore, in case dynamic of BGND-transients, VPRELS follows BGND as desired, whereas the DC-shift between BGND and SYSGND leads to a small erroneous DC-offset in VPRELS. This might be eliminated by adding a dedicated bandgap voltage reference that is based on BGND.⁴

Similar to the voltage reference input, also the reference current input of a module is subject to interference coupling. Therefore, a low-pass filter at the current reference input may be appropriate as well. This can be realized using a gate-stabilizing capacitor in a local current mirror, as depicted by CI in fig. 2.

⁴ This example supposes that the additional costs would outweigh the benefits, and thus, a dedicated bandgap is not present.

2.2 An Exemplary BCD-Technology for Automotive System ICs

In this section, MOSFET-centered BCD-technologies suitable for Automotive System ICs (see sec. 2.1) are explained in detail. Fig. 3 shows a representative cross-section. In such BCD-technologies, the whole chip area is covered by an n-epitaxial layer, which forms a p-n-junction D_{sub} with the underlying wafer-substrate⁵. This wafer-substrate, which has no functional purpose, is rather high-ohmic (resistivity ρ_{sub}). Nevertheless, displacement currents (permittivity $\epsilon_{r,\text{sub}}$) are usually not relevant below 10 GHz (see sec. 5.2.1). The n-epitaxial layer contains a highly-doped n-buried layer with a comparatively small sheet resistance R_{nepi} . This n-epitaxial layer is dissected into multiple electrically isolated silicon islands (also referred to as *pockets*) by means of *deep trench isolation*. Each n-epitaxial pocket can contain one or more semiconductor devices. The n-epitaxial pocket can be connected at multiple points by low-resistance n-sinkers (resistance R_{nsink}), or alternatively, by more compact but more high-resistive n-epitaxial contacts ($R_{\text{ncont}} \gg R_{\text{nsink}}$). The wafer-substrate is electrically connected by a conductive filling material that is embedded in the deep trenches. This conductive filling material is

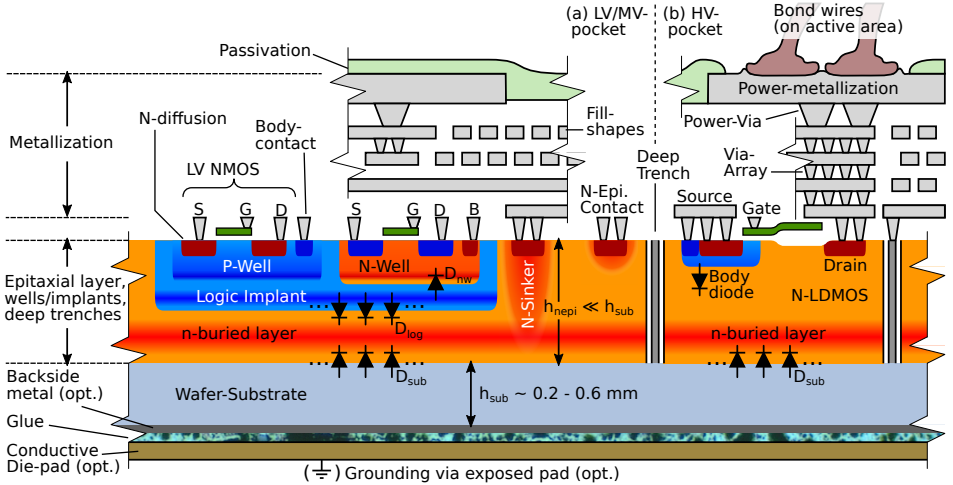


Figure 3: Simplified cross-section of a hypothetical state-of-the-art BCD-technology that is similar to the technology used in the test-IC from chapter 6. Bluish colors represent p-doping and reddish colors represent n-doping. This drawing is not to scale: The wafer-substrate thickness h_{sub} is at least one order of magnitude larger than the n-epi. layer thickness h_{nepi} .

⁵ In contrast, SOI-technologies realize a galvanic isolation instead. They might add a non-conductive buried oxide layer underneath the conductive n-buried layer [6].

parameterized by its longitudinal resistance per unit length $R_{\text{tr, long, int.}}$ and by its conductance from top to bottom per unit length $1/R_{\text{trench, z}}$. Additionally, the wafer-substrate can be electrically connected at the backside. This is enabled by an optional low-ohmic backside metallization in conjunction with a highly conductive glue and an exposed pad. If an electrical backside connection is not required, the backside metallization may be omitted, but typically nevertheless a slightly conductive glue is used and an exposed pad is present in the IC-package. This is because the combination of a conductive glue and a soldered exposed pad forms an efficient heat sink to the PCB ground plane. Details on the electrical parameterization of the die backside are found throughout sections 6.2 to 6.5. [6], [26], [37], [185], [187]

Wells and Devices Devices are formed from a variety of wells and other implants (bluish and reddish areas in fig. 3) and diffusion areas (dark red, dark blue) are added on top of the n-epitaxial layer. Within this thesis, the term *substrate* refers to union of the wafer-substrate, the n-epitaxial layer, the wells and the deep trenches. The wells and implants are associated with parasitic sheet resistances (R_{pwell} , R_{nwell}) and contact resistances (R_{pwcont} , R_{nwcont}). Also, they entail further parasitic p-n-junctions, e.g. D_{log} , D_{nw} and the body diode of the N-LDMOS. As shown in fig. 3, two kinds of pockets of the n-epitaxial layer must be distinguished: The left side (a) is a low-voltage (LV) / medium voltage (MV) n-epitaxial pocket, which contains a large number of very small, symmetric NMOS-and PMOS-transistors of a low voltage class. Such pockets can contain digital CMOS logic, OTAs, bandgap references and other low voltage analog circuitry. Usually, the p- and n-well reside in p-doped *logic implant*, which is galvanically connected with the p-well. The right side (b) is a high-voltage (HV) n-epitaxial pocket, which contains a single power transistor that can directly operate from the IC's battery pin, and must therefore withstand voltages of e.g. 45 V (see sec. 2.1). A commonly used kind of power transistor is the laterally-diffused DMOS device (LDMOS), where drain and source are asymmetric. It achieves a high source-drain breakdown voltage at a low on-resistance, while at the same time a gate-source voltage compatible with LV- or MV-MOSFETs is sufficient to enter the on-state. As shown in fig. 3, the n-epitaxial pocket housing a N-LDMOS is typically connected to its drain terminal. Conversely, the n-epitaxial layer of a P-LDMOS is typically connected to its source terminal. Some technologies may feature more advanced devices, where the n-epitaxial layer is isolated from source and drain via additional p-n-junctions, and where it may be connected separately. Moreover, some technologies may allow a circuit designer to place n-sinkers in HV n-epitaxial pockets, which can be used to reduce the connecting resistance of the n-buried layer. [136]

Metallization The technology shown in fig. 3 features four fine-pitch metal layers, as well as one thick, coarse power-metal layer. The metal layers are isolated from each other by the intermetal dielectric. For manufacturing reasons, no metal layer can be much substantially thicker than its minimal structure size. Therefore, sheet resistance of the lower four metal layers R_{metal} is large in comparison to the sheet resistance of the power metal layer R_{power} . For power transistors that conduct more than about 10 mA DC, drain and source connections are typically connected directly to the power metallization by means of large via arrays (see fig. 3 (b)). Dedicated pins carrying a high current, e.g. the DC/DC output, do not have to be routed on the die, but instead bond pads can be placed directly on top of the power transistors. Conversely, if a supply- or ground-pin is shared among multiple modules (sec. 2.1), the additional on-die resistance and inductance may become a concern. For process technical reasons, so-called fill-shapes must be added to the intermetal dielectric, as shown in fig. 3 (a). These are floating metal islands, the size of which is close to the minimal structure size. In addition, it is required that large metal plates are perforated by small pillars of intermetal dielectric, which are called cheese-shapes (not shown here for clarity). Parasitic capacitances exist between metal lines and planes as well as between the metallization and the surface of the substrate. They can be calculated from their geometry and using the dielectric constant of the intermetal dielectric ϵ_r . Parasitic inductive couplings between metal lines may have an impact on the circuit functionality, albeit they are typically considered as much less relevant than capacitive couplings. The magnetic permeability of the intermetal dielectric is very similar to vacuum. The automatic calculation of parasitic resistances, capacitances, inductances and inductive couplings associated with the metallization can be achieved by so-called *parasitic extraction* tools, see sec. 2.6. [197]

Capacitive Substrate Parasitics The deep trenches (also called trenches) are isolated from the n-epitaxial layer by an oxide layer. In comparison to the more primitive junction isolation (see sec. 1.2), this allows for more dense integration in high voltage technologies. The parasitic capacitance between the deep trench and the n-epitaxial layer per unit length is denoted by C_{trench} . While the parasitic p-n-junctions D_{sub} , D_{log} and D_{nw} are reverse-biased, their small-signal model reduces to a capacitance. The bias-dependent AC-capacitance per area is denoted by C_{sub} , C_{log} or C_{nw} , respectively. It is clear that pairs of adjacent parasitic p-n-junctions in fig. 3 actually form parasitic bipolar transistors with a non-zero current gain β . However, obviously, the current gain β is only effective in forward bias, and it can be completely neglected regarding capacitive currents across the junction. [136]

Forward Bias of Parasitic p-n-Junctions Under normal operating conditions, forward bias of these p-n-junctions is usually avoided, and in this case β can be neglected. However, unwanted forward bias of D_{sub} , D_{log} and D_{nw} may occur during ESD-events, during latch-up testing, and as part of the normal operation of some DC/DC-converter designs (see sec. 6.2). In modeling of parasitic effects, the *forward bias* of p-n-junctions like D_{sub} , D_{log} and D_{nw} (i.e. minority carrier injection) is probably the most difficult case. This is due to a number of reasons: Firstly, the associated parasitic bipolar transistors are typically multi-collector, and the currents gains of each collector are highly layout dependent. These current gains can be computed using TCAD-software from a set of coupled non-linear partial differential equations, which describe fundamental semiconductor principles such as the Fermi level and recombination processes. In contrast, for example, layout dependent resistances in the wafer-substrate under reverse bias (i.e. majority carriers only) are described by the much more simple, linear Laplace's equation (see sec. 5.2.1). Secondly, due to an effect called conductivity modulation, the parasitic series resistance in forward-biased diodes and bipolar transistors is non-linear and strongly different from reverse bias. Therefore, when experimentally characterizing substrate parasitics, one may *not* equate the AC series resistance in reverse bias with the DC resistance in forward bias ⁶. Third, the parasitic substrate diodes are often electrically in parallel to other diodes, to which they are poorly matched, e.g. because they arise from different dopant profiles. In forward bias, these p-n-junctions are competing over the current, and a very precise parameterization of these devices would be required to predict the current path. In turn, this current path would have to be known in order to predict the collector currents. For example, if the N-LDMOS's source and the trenches are connected to the same ground, then D_{sub} is in parallel to the body diode of the N-LDMOS. Even worse, if the N-LDMOS's source is connected to a different ground, the current path additionally strongly depends on the transient of the ground potential difference. [27], [49], [105], [106], [108], [167], [197]

One might suspect that circuits that cause a forward bias of D_{sub} during normal operation may cause substrate-bound RF-emissions. However, empirical evidence suggests that this contribution may be often negligible in comparison to the capacitive substrate currents (see chapter 7). This thesis has no ambitions to solve these fundamental modeling issues associated with forward bias. Rather, in this thesis, the modeling efforts regarding the substrate will be restricted to the reverse bias, which is presumably more relevant for the EMC. Where technically and economically feasible, it should be encouraged to

⁶ Throughout this thesis, parasitic resistances like R_{nsink} always correspond to reverse bias.

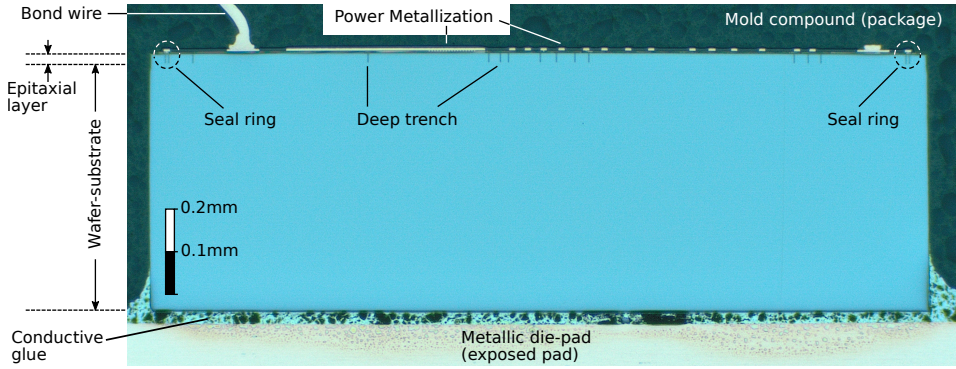


Figure 4: Optical microscope image showing a polished cross section of the test-IC (sec. 6.2, packaging variant #PI), which is built using a BCD-technology similar to fig. 3. The backside metallization is very thin and therefore cannot be seen.

develop circuits and technologies in a way that such poorly defined conditions cannot occur, even under susceptibility testing.

Fig. 4 shows a microscopic image of a test-IC with electrically connected backside in a plastic package. Table I summarizes the parameterization of parasitic elements introduced in this section. The last column specifies which parasitics are included in the substrate extractor models (table II, from #X-NC to #X-MCAP(C_{bs})) used to simulate the test-IC developed in this thesis – further details are found in sec. 6.3.1.

In the semiconductor technology used in this thesis, the die is framed by a *chip seal ring*, which, from the electrical point of view, consists of two concentric deep trench rings that are connected to an overlying very low-ohmic power metal trace. Typically, all trenches are electrically connected to this seal ring. This is achieved by, firstly, by joining all devices' trenches together with the seal-ring and with each other. Secondly, most deep trenches are re-enforced by an above-lying metal strips, to which they are connected. Therefore, the deep trench filling material in combination with this metal strip forms a conductor with a reduced effective longitudinal resistance – the so-called composite longitudinal trench resistance $R_{tr, long, comp.}$ (see table. I). If a re-enforcing metal strip of standard dimensions is used, the composite longitudinal trench resistance is much reduced in comparison to the intrinsic longitudinal trench resistance. Note that the $R_{tr, long, comp.}$ may vary depending on whether the re-enforcing metal strip is present or not, and also depending on it's width.⁷

⁷ Moreover, additional metal strips may be present that reduce the connecting resistance of the deep trenches.

Denotation	Typ. unit	Description	in test-IC substrate model?
R_{metal}	$[\Omega]$	Sheet resistance of the fine-pitch metal layers	some ‡
R_{power}	$[\text{m}\Omega]$	Sheet resistance of power metal layer	no
ϵ_r	[1]	Relative permittivity of the intermetal dielectric	some ‡
R_{nsink}	$[\Omega]$	Connecting res. of the n-buried layer by an n-sinker	some •
R_{ncont} †	$[\text{k}\Omega]$	Connecting res. of the n-buried layer by n-epitaxial contacts	some •
R_{nwcont} †	$[\text{k}\Omega]$	Connecting resistance of the N-wells	no
R_{pwcont} †	$[\text{k}\Omega]$	Connecting resistance of the P-wells	no
$R_{\text{trench,via}}$	$[\Omega]$	Resistance of deep trench contact array	yes ◇
R_{nepi}	$[\Omega]$	Sheet resistance of the n-buried layer	some •
R_{pwell}	$[\text{k}\Omega]$	Sheet resistance of P-Wells	no
R_{nwell}	$[\text{k}\Omega]$	Sheet resistance of N-Wells	no
$R_{\text{tr,long,int.}}$	$[\Omega/\text{um}]$	Longitudinal resistance of deep trench filling material (<i>intrinsic longitudinal trench resistance</i>)	yes ◇
$R_{\text{tr,long,comp.}}$	$[\Omega/\text{um}]$	Effective longitudinal resistance of deep trenches, including the above-lying connected metal strip (<i>composite longitudinal trench resistance</i>)	yes ◇
$R_{\text{trench,z}}$	$[\text{k}\Omega \text{um}]$	Resistance of deep trench filling material from top to bottom (<i>vertical trench resistance</i>)	yes ◇
C_{trench}	$[\text{fF}/\text{um}]$	Capacitance across isolating oxide of deep trench per length	yes ◇
C_{sub} *	$[\text{fF}/\text{um}^2]$	Small signal capacitance across D_{sub} per area (see fig. 3)	yes
C_{log} *	$[\text{fF}/\text{um}^2]$	Small signal capacitance across D_{log} per area (see fig. 3)	some •
C_{nw} *	$[\text{fF}/\text{um}^2]$	Small signal capacitance across D_{nw} per area (see fig. 3)	no ‡
ρ_{sub}	$[\Omega \text{cm}]$	Electrical resistivity of the wafer-substrate	yes
$\epsilon_{r,\text{sub}}$	[1]	Relative permittivity of the wafer-substrate	no
† Not constant. Depends on contact dimensions in a non-linear manner. * Depends on the voltage bias across the p-n-junction. ‡ Only metallization of n-sinkers in the intermediate region / digital part as well as above the deep trenches. • Only in the intermediate region and in the digital part. ◇ However, a large number of small trenches were removed. ‡ In the digital core: Not present in the substrate model but instead accounted for by the simulations in the form of a lumped capacitor.			

Table I: Salient parasitic elements in the described automotive BCD-technologies, not including the forward bias state of parasitic p-n-junctions and excluding the die-backside.

2.3 Operating Principles of SPICE-like Circuit Simulators

SPICE was a highly influential circuit simulator developed in the seventies. Most industrial strength simulators are backwards compatible to SPICE in terms of the circuit file format, and their simulation algorithms are similar. Such SPICE-like simulators parse a machine-readable representation of a circuit, also known as *netlist*, then apply a number of *analyses*, the results of which are then written out to a so-called *results database*. [110], [112], [138]

In the following, the basic circuit analyses are summarized:

DC Analysis (“DC”): An *equilibrium point* or *quiescent operating point* of a circuit is a state of the circuit, i.e. a value assignment of certain nodal voltages and branch currents, which does not change with time. In the DC-analysis, the circuit is excited using voltage and current sources that are constant in time. Then, a quiescent operating point is computed by solving a non-linear algebraic system of equations. Since in some circuits multiple quiescent operating points exist, the result of a DC simulation might not be unique. [110]

AC Analysis (“AC”): In the AC-analysis, the circuit is excited by one or multiple sinusoidal AC-current or -voltage sources, and a frequency sweep is performed. This yields the amplitude/phase responses of certain node voltages and branch currents as a function of the frequency, which are also known as *AC transfer functions*. This computation is based on phasor analysis. For non-linear circuits, the AC simulation additionally requires an operating point, which may be either obtained from a DC simulation or from a transient simulation.⁸ The non-linear circuit is then linearized at this operating point. Therefore, AC-analysis cannot predict distortion, frequency translation and DC shifts. In contrast to DC- and TRAN-analyses, the system of equations solved in AC-simulations is always linear. [110], [135], [143]

Transient Analysis (“TRAN”): In the transient analysis, the circuit can be excited using time-varying voltage and current sources. The transient analysis then simulates the time-dependent behavior of the circuit by numerically solving a differential-algebraic system of equations. The output of a transient simulation is a time trace for each state variable, i.e. for certain nodal voltages and branch currents. The initial state at time t_0 is typically obtained from a preceding DC-simulation. Starting from the initial state at time $t_0 = 0$, each successive time point t_j is computed by solving a non-linear algebraic system

⁸ This operating point is not necessarily quiescent if a transient is used to generate it. It is a common misconception that non-quiescent operating point might adversely affect the numerical stability of the AC-simulation – in fact, this is not the case.

of equations. The size of the time step Δt is variable, and it is re-determined at each time t_j using a time step control heuristic, such as the LTE-criterion. There are different methods for temporal discretization which strongly differ in stability, accuracy and speed (see also sec. 2.3.2). Very common methods are GEAR and the trapezoidal method, and another notable family are the Runge-Kutta methods. [110], [139], [140]

2.3.1 Circuit Equation Formulation and Equation Solvers

This section investigates the algebraic linear systems of equations that arise in the TRAN-, AC- and DC-analyses, and it outlines how they are obtained from the circuit model. Moreover, the used linear solvers and their performance characteristics are explained. A deep understanding is important in order to compactly encode FEM-models into circuits (sec. 5.2.4), to optimize the compute-performance of substrate-extractor models (sec. 2.6.2, sec. 5.2.3), and to understand the asymptotic run-time of simulators applied to netlists from RLCK-extraction (chapter 4).

The modified nodal analysis (MNA) dates back to the early archetypal circuit simulators, and today it is a quasi-standard for circuit simulators. In the MNA, state variables are introduced for all nodal voltages except ground, as shown in fig. 5. Some branch currents are also represented as state variables, i.e. the currents across voltage sources and inductors (in fig. 5: I_{V1} , I_{L1}). An alternative to the MNA is the sparse tableau analysis, which includes all branch currents and thus leads to more unknowns. [74], [110], [139], [190, Ch. 4]

The nodal voltages and branch currents from the MNA are combined to two vectors $\vec{V}$ and $\vec{I}$. In the DC- and AC-analysis, the circuit imposes a systems of equations in terms of the variables $\vec{x} = (\vec{V}, \vec{I})$. While in the DC-analysis $\vec{x}$ represents the real-valued DC nodal voltages and branch currents, in the AC-analysis $\vec{x}$ is complex valued and represents the infinitesimal amplitudes and the phase of sinusoidal voltages and currents superimposed on the operating point. In transient analysis, the variables solved for is the state at time step

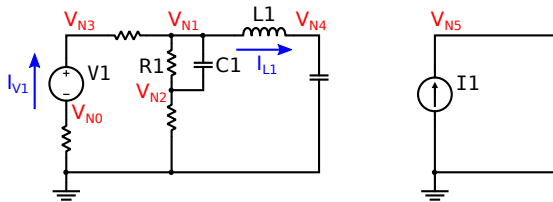


Figure 5: The modified nodal analysis (MNA) is applied to a simple linear circuit. State variables are depicted as red labels (nodal voltages) and blue arrows (branch currents).

$n + 1$ given by $\vec{x}_{n+1} = (\vec{V}, \vec{I}, \vec{Q}, \vec{\Phi})$. In contrast to DC-analysis, the state vector is extended by $\vec{Q}$ and $\vec{\Phi}$, which represent charges and fluxes of non-linear capacitors and non-linear inductors.⁹ The systems of equations can be written as follows [190, Ch. 13]:

$$0 = F_{\text{TRAN}}(x_{n+1}) := E \cdot x'(x_{n+1}) + G \cdot x_{n+1} + p(x_{n+1}) - w \quad (\text{TRAN})$$

$$0 = F_{\text{DC}}(x) := G \cdot x + p(x) - w \quad (\text{DC})$$

$$0 = F_{\text{AC}}(x) := G_{\text{AC}} \cdot x - w_{\text{AC}} \quad (\text{AC})$$

where G and G_{AC} are matrices summarizing the contributions of all linear or linearized elements, $p(x)$ summarizes the contributions of all non-linear elements, w and w_{AC} contain source terms and the matrix E realizes the time-derivatives due to inductors and capacitors. In the backwards differentiation formulae (BDF) formalism of TRAN, x' is a function of x_{n+1} which approximates the continuous time derivative at time t_{n+1} by polynomial interpolation, given the state variables at prior points in time $x_n, x_{n-1}, \dots$ as implicit arguments. For example, the N -th order GEAR method uses N prior points. [190, Ch. 13]

The solution of the non-linear algebraic systems of equations $F_{\text{TRAN}}(x_{n+1}) = 0$ and $F_{\text{DC}}(x) = 0$ is typically accomplished by the Newton's method. This is an iterative procedure, which finds nulls in F by successively refining approximate solutions $x^{(k+1)}$. The refinement step $\Delta x^{(k)} := x^{(k+1)} - x^{(k)} = (\Delta \vec{V}^{(k)}, \Delta \vec{I}^{(k)}, \dots)$ is computed by solving the following *linear* system of equations, where the linear coefficients are given by the Jacobian dF/dx at $x^{(k)}$ [190, Ch. 12, Ch. 13]:

$$\frac{dF}{dx}(x^{(k)}) \cdot \Delta x^{(k)} = -F(x^{(k)}) \quad (1)$$

The Newton's method requires an initial guess $x^{(0)}$, which is typically taken from the previous time step x_n in case of TRAN, or a null-vector in case of DC. Newton's method can diverge if the initial guess is not good enough. For TRAN, this usually isn't a problem because, in case of a divergence, it is usually automatically restarted with a smaller Δt , whereby the accuracy of the initial guess can be increased arbitrarily. However, divergences of the Newton's method are a major problem in the DC-analysis, which can be tackled both numerically (continuation methods) and in interaction with the user (nodesets). For very complex circuits DC convergence may be very difficult to

⁹ $\vec{Q}$ and $\vec{\Phi}$ are added to the state only to simplify the computation of the Jacobian dF_{TRAN}/dx . They do not add further information to the state vector since $\vec{Q}$ and $\vec{\Phi}$ are functions of $\vec{V}$ and $\vec{I}$ [190, Ch. 13].

achieve, and it is sometimes more convenient to avoid it entirely: A so-called initial-transient simulation, in which all nodes start at 0 V and where a pseudo power-up sequence is performed, can serve as a replacement for DC. [110]

Solving the linear system of equations in AC simulation can formally be regarded as a single iteration of the Newton's method in eq. (1). Thus, in all of AC, TRAN and DC, the solution process is eventually reduced to the solution of *linear* systems of equations with the linear coefficients dF/dx . In the MNA, dF/dx is of a 2×2 block structure with sub-matrices Y_R, B, C and D [74]¹⁰:

$$\begin{pmatrix} Y_R & B \\ C & D \end{pmatrix} \cdot \begin{pmatrix} \Delta \vec{V}^{(k)} \\ \Delta \vec{I}^{(k)} \end{pmatrix} = -F(x^{(k)}) \quad (2)$$

where the reduced nodal admittance matrix Y_R summarizes resistors, capacitors and voltage-controlled current sources (VCCS), and B, C and D summarize voltage sources, inductors and other controlled sources. Note that MOSFET and bipolar device models are essentially reduced to a circuit of non-linear controlled current sources, resistors and capacitors.

The computation of Y_R, B, C and D from the circuit is most intuitive in a construction called *modified nodal analysis by inspection* [190, Ch. 4], [74]: Here, the left-hand side of eq. (2) is expressed as a sum over so-called *stamps*, each of which arises from exactly one circuit element. For example, in the circuit from fig. 5, by expanding the sum over the stamps in the subset of equations $Y_R \cdot \Delta \vec{V}^{(k)} + B \cdot \Delta \vec{I}^{(k)} = \dots$, one obtains:

$$\left(\begin{pmatrix} 0 & \dots & \dots & 0 \\ \vdots & +G_{12} & -G_{12} & \vdots \\ \vdots & -G_{12} & +G_{12} & \vdots \\ 0 & \dots & \dots & 0 \end{pmatrix} + \dots \right) \cdot \begin{pmatrix} \vdots \\ \Delta V_{N1}^{(k)} \\ \Delta V_{N2}^{(k)} \\ \vdots \end{pmatrix} = \dots \quad (3)$$

Here, the shown summand corresponds to the stamp of R1 plus the stamp of C1. Depending on the simulation analysis, G_{12} is [74], [139]:

$$G_{12} = \begin{cases} R_1^{-1} & \text{for DC analysis} \\ R_1^{-1} + i\omega C_1 & \text{for AC analysis} \\ R_1^{-1} + C_1/\Delta t & \text{for TRAN analysis (GEAR)} \end{cases} \quad (4)$$

¹⁰ For simplicity, in case of TRAN, this example assumes that no non-linear capacitors/inductors are present, and thus the vectors $\vec{Q}$ and $\vec{\Phi}$ are empty.

where $\omega = 2\pi f$ is the angular frequency.

Eqs. (3,4) demonstrate that the nonzero pattern of Y_R is strongly tied to the graph-topology of the circuit. Moreover, in TRAN with the GEAR integration method, it is the same as in AC simulations¹¹. In DC simulation, additional zeros can occur, for example in nodes pairs only connected by capacitors.

The nonzero pattern of the Jacobian matrix is of fundamental importance to a class of algorithms used to solve linear systems called *sparse direct solvers*. Direct solvers derive from Gaussian elimination, but take advantage of the fact that the Jacobian matrix is sparse, i.e. that the number of nonzero elements $N_{n.z.}$ are much less than $N_{eq.}^2$, where $N_{eq.}$ is the number of equations. This is a very important optimization, as a result of which sparse direct solvers achieve lower asymptotic run times than dense Gaussian elimination. The exact asymptotic run time achieved with sparse direct solvers depends on topological properties of the nonzero pattern graph, and also on particularities of the sparse direct solver algorithm. [40], [43]

The alternative to sparse direct solvers are iterative linear solvers, in particular a class of algorithms known as Krylov subspace methods. Although the idea to use iterative linear solvers in circuit simulation is as old as SPICE itself, to this date it has not yet found widespread use in industry. Iterative linear solvers could, in some cases, provide a remedy of the sometimes strongly super-linear computational complexity of direct solvers, and they are more amenable to parallelization. [56], [121], [139], [202]

On the other hand, they are also associated with a reduced robustness: Albeit iterative linear solvers like GMRES guarantee convergence after a finite number of steps, a gain in efficiency over Gaussian elimination is only achieved if the iteration is terminated prematurely. The speed of convergence strongly depends on the *distribution of eigenvalues* of the matrix – a property which is even more elusive than its nonzero-pattern's graph topology. To improve the distribution of eigenvalues, the Jacobian must be pre-multiplied by a so-called preconditioner, which is a heuristical matrix that is constructed such that the set of its eigenvalues are compactified. Preconditioners are crucial for achieving sufficient convergence, but they are mostly heuristical, and thus they introduce additional assumptions about the system of equations. Thus, it has been speculated that iterative linear solvers do not lend themselves so well to arbitrary circuits because this is a very broadly-scoped problem class. [34], [121], [161], [202]

¹¹ However, if explicit integration methods, which are less stable, are used in TRAN, then the nonzero pattern is vastly different, and may even decompose into certain block structures, which guarantees an asymptotically linear solver runtime [110].

Nevertheless, progress has been made recently in finding suitable preconditioners for circuits [121], [202], and Infineon’s in-house simulator TITAN [17] provides an implementation using the quite general ILU-preconditioner. Therefore, within this thesis, iterative linear solvers are indeed considered a promising candidate for future fast circuit simulators.

2.3.2 Instabilities and Inaccuracies in Circuit Simulations

The transient analysis is inherently based on a number of heuristics and approximations. Any heuristic or approximation can lead to simulation errors if its underlying assumptions are violated. Moreover, the non-consideration of physical symmetries or conservation laws can lead to inaccuracies and to premature terminations of transient simulations. In the following, multiple examples, which are relevant in the construction of accurate and stable substrate and package models, are provided:

Instabilities and inaccuracies due to non-physical models A basic requirement for stable transient simulation is energy conservation: For instance, the use of reduced-order macromodels (see sec. 2.4.2) without passivity enforcement can “blow up” transient simulations [64], [66]. Other well-known quality characteristics of device or parasitic models are charge conservation, reference-independence and reciprocity (sec. 2.4.1). For example, small violations of reference-independence may lead to spurious couplings of common mode and differential mode signals. Furthermore, in a similar way to passivity violations, abstractions of transistor circuits with an unrealistic high-frequency characteristic can cause instabilities: An example is the substitution of an OTA by an ideal voltage-controlled current source.

Mistakes of the Newton’s method convergence criterion The Newton’s method used by DC and TRAN only converges towards the null of $F(x)$ without ever exactly reaching it. A criterion must be used to decide when the iteration should be terminated. Typically, this is based some norm of the update vector $\Delta x^{(k)}$, as well as a norm of the residual $F(x^{(k)})$ [110]. These depend on heuristical absolute and relative error thresholds – e.g. Spectre’s “iabstol”, which is an absolute tolerance for violations of Kirchhoff’s current law (KCL) of units Ampere. If the tuning of this heuristic is too strict, due to numerical errors inherently arising from the linear solver, the Newton’s method might not terminate. This occurs, for example, if the branch currents represent quantities that are not of units Ampere, as in some implementations of reduced-order macromodels (sec. 2.4.2) or thermo-electric models [4].

Misadjustment of the time step by the local truncation error criterion

Based on auxiliary information obtained from the integration method it is possible to estimate the error in nodal voltages, branch currents, capacitor charges or inductor fluxes due to the finite Δt . This error caused by a single time step is called the local truncation error (LTE), whereas the error for the complete transient is called global truncation error [139]. As anticipated in sec. 2.3, this is used to continuously re-adjust Δt by a so-called LTE-criterion [110]: The precise formulation of the LTE-criterion has been debated frequently and differs among simulators. Common to all LTE-criteria is the use of heuristical thresholds of units Volts or Coulomb. Therefore, very similar to the Newton's method convergence criterion, the LTE-criterion is easily upset by pseudo-circuits that represent abstract mathematical models.

Artifacts and “blow-up” due to the temporal discretization As anticipated in sec. 2.3, there are different temporal discretization methods for transient simulations which differ in stability, accuracy and computational performance. A distinction is made between *implicit* and *explicit* integration methods. A desirable property is A-stability, which ensures that the temporal discretization is stable if the underlying differential equation is stable, no matter how large the time step [139]. Many important implicit integration methods like GEAR-2 are A-stable, whereas explicit integration methods are never A-stable. Explicit methods which are not A-stable, like forwards Euler, typically immediately “blow up” if Δt is larger than the smallest time constant τ in the system [110]. Such circuits, which may arise from parasitic extraction (sec. 2.6), should not be used with explicit integration methods. Therefore, within this thesis, only *implicit* integration methods are considered, despite they entail a more connected nonzero pattern (sec. 2.3.1), which can cause a higher asymptotic run time.

To summarize, device and parasitic models should be passive, reference-independent, charge-conserving and reciprocal. Moreover, models, in which node voltages and branch currents are not of the units assumed by the simulator, should be avoided. While explicit integration methods might drastically speed up the linear solver, their practical value is limited because, in circuits with small time constants, very small step sizes would be needed.

AC simulations are not only very fast, but far more stable than transient simulations: Since AC simulations neither use Newton's method nor the LTE-criterion, they are completely free of heuristical thresholds like “iabstol”, and hence the associated issues vanish. Moreover, the instabilities of the differential-equations due to temporal discretization or due to violations of energy conservation are issues specific only to transient simulations.

Beware that many simulation instabilities stay hidden during initial testing of the model: For example, high-frequency ($\gg 1/\Delta t$) instabilities in the differential-equations may be damped out by the commonly used implicit integration methods. However, a rapid event in subsequent simulations, which causes a strong decrease of the time step Δt , can then trigger such instabilities. Note that the circuitry causing the rapid event is not the one to be blamed. Hidden instabilities may also arise from a defeat of the LTE-criterion. Here, the model error remains masked as long as there is another component in the circuit that enforces a sufficiently small Δt .

2.3.3 Advanced Simulator Features and Analyses

Industrial strength circuit simulators have advanced features and other analyses, some of which go beyond the feature set inherited from SPICE:

Advanced AC Analyses (“XF”, “SP”): Simulators like Spectre or TITAN support a multi-source transfer function analysis called XF [110]. This allows for potentially drastic speed improvements: A run of XF is equivalent to multiple AC simulations, in each of which a different AC-source is enabled, while the AC transfer function to a single node is recorded. However, XF can compute an *arbitrary number* of such AC transfer functions with the same effort as a *single* AC simulation. This will be exploited in sec. 6.3.2. Another extension of the AC analysis is the S-parameter analysis (SP) [110]. The SP-analysis determines the frequency-dependent $N_{\text{port}} \times N_{\text{port}}$ S-parameter matrix, which completely characterizes the system’s reaction to small signal excitations (sec. 2.4). Note that the SP-analysis can be up to N_{port} times faster than a naive computation of the S-parameters using repeated execution of AC-simulations: This is because a single LU-decomposition (see also sec. 5.2.3) can be used to compute all columns of the S-parameter matrix.

Sensitivity and Alteration analyses (“SENS”, “ALTER”): Motivations for studying the behavior of a circuit under parameter variation are, either, to find the parameters with a leading-order contribution to the circuit’s performance, or to investigate consequences of process variation. An application will be described in sec. 6.7. The user is usually interested in the variation of a large number parameters because no strong prior expectation about their relevance is given. In sensitivity analysis (SENS), the partial derivatives of a simulation output with respect to multiple circuit parameters are evaluated. Some simulators support sensitivity analysis on top of DC-, AC- and even TRAN-analysis [190, Ch. 8]. In contrast, the alteration analysis (ALTER) quantifies the impact of changing the circuit parameters to considerably different values, rather than merely computing the tangential sensitivity. Here, substitute values for

each parameter must be provided to the simulator. Regarding run time, the ALTER-analysis can be understood as a loop over all examined circuit parameters, which repeatedly invokes AC-, DC- or TRAN-analyses. Conversely, the SENS-analysis can be implemented more efficiently [190, Ch. 8].

RF-Analyses (“HB”, etc.): As anticipated in sec. 2.3, the limitations of AC-simulation include the neglect of distortion, frequency translation and DC-shift. This is resolved by a method called harmonic balance (HB), which adds amplitudes and phases of higher harmonic frequencies and DC offsets to the set of variables [109], [114]. RF-analyses like harmonic balance directly obtain periodic steady state (PSS) solutions, and are much faster than transient simulation. This might be useful in EMC simulations regarding the immunity of analog circuits, where mainly the PSS is of interest [72]. Since RF-analyses were introduced, RF-methods have grown in their capability of handling large circuits [111].

2.4 Characterization and Simulation based on Network Parameters

Network parameters are a frequency-dependent complex-valued matrices which quantify the response of a time-invariant subcircuit to externally applied small-signal AC excitations. The essential property of network parameters is that they *completely* characterize the externally observable behavior of linear time-invariant (LTI) subcircuits [16]. Since network parameters obfuscate the internal dynamics of the characterized systems¹², they can be regarded as a “black-box” description. There is a large variety of different flavors of network parameter representations, which are termed Y-, Z-, S-, H-, ABCD-, or T-parameters, et cetera. They contain the same information, and hence, can be arithmetically converted into one another. Network parameters can be directly measured using *Vector Network Analyzers*, and they can be obtained from circuit or finite element simulations. In turn, a network parameter dataset can be instantiated as a “black-box” subcircuit in subsequent circuit simulations, which has important applications in RF engineering [182] and in EMC simulations.

2.4.1 Theory of Network Parameters

Fig. 6 shows two subcircuits #1 and #2, with AC excitations (here: AC voltage sources) connected to pairs of terminals. Such a pair of terminals is called

¹² A network parameter dataset is merely an equivalence class of subcircuits, and admits for multiple realizations [16]

a port [16]. For example, (T1, T3) in fig. 6 (a) forms port 1, and (T4, T3) in fig. 6 (b) forms port 3. In the following, the voltage across port n is denoted by V_n and the current flowing over the attached source is denoted by I_n . The voltages V_n are the components of the voltage vector V , and the currents I_n form the current vector I .

Assuming that subcircuits #1 and #2 are *linear time-invariant* (LTI), e.g. transistor circuits linearized at an operating point, phasor analysis can be applied. Now let the external AC excitations be in the form of AC voltage sources with $V_n^{(x)} = \delta_{i,x}$.¹³ The subcircuit then responds with an AC current vector $I^{(x)}$. Given that the response $I^{(x)}$ is known for each $x \in [1, 2, \dots]$, the AC current response I to an arbitrary AC voltage excitation vector V can be obtained using the superposition principle:

$$I = Y \cdot V \quad (5)$$

where the so-called Y-parameters Y , also called admittance parameters, are a complex-valued matrix, the rows of which equal $I^{(x)}$. The Z-parameters Z , also called impedance parameters, are the matrix inverse of Y , and can be understood analogously as the circuit's response to AC current excitations.

Clearly, the complex-valued matrices Y and Z are frequency-dependent. Now assume $Y(f)$ and $Z(f)$ are known over the entire frequency range. Using this information, the subcircuit's response $I(t)$ to a *transient*, i.e. time-dependent, excitation $V(t)$ can be predicted as well: In the following, $\hat{V}(f) := \mathfrak{F}\{V\}(f)$ and $\hat{I}(f) := \mathfrak{F}\{I\}(f)$ denote the Fourier transform of $V(t)$ and $I(t)$,

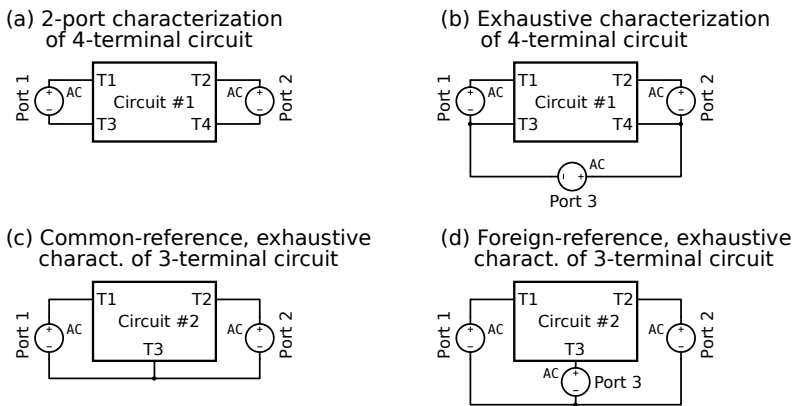


Figure 6: Different port configurations for a 4-terminal subcircuit (Circuit #1) and a 3-terminal subcircuit (Circuit #2). The port configuration (a) is not exhaustive.

¹³ The so-called Kronecker delta symbol $\delta_{a,b}$ equals zero if $a \neq b$ and equals one if $a = b$.

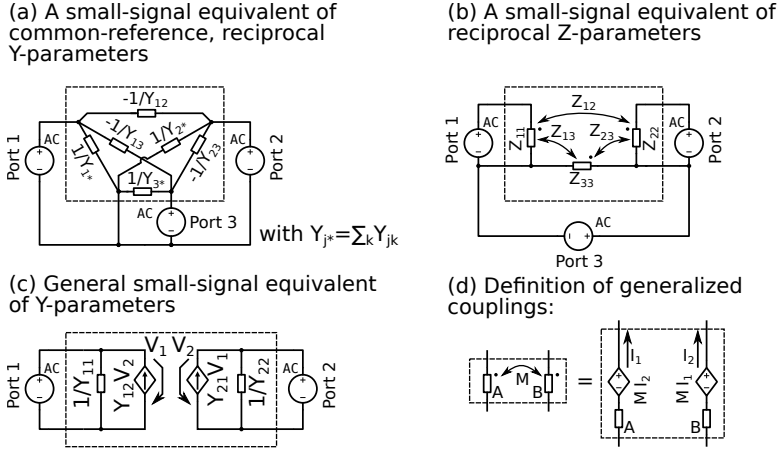


Figure 7: (a–c) depict various small-signal equivalent circuits for Y- and Z-parameters. In the special case of two ports, (a) is also known as π -equivalent [198]. All shown impedances and controlled sources are frequency-dependent and complex-valued. For $A(\omega) = i\omega L_1$, $B(\omega) = i\omega L_2$ and $M(\omega) = i\omega M_{12}$, the generalized couplings from (d) are equivalent to inductive couplings [16].

respectively. It is a decomposition of the transient excitation and response into phasors. Eq. (5) relates $\hat{V}(f)$ and $\hat{I}(f)$, and hence [135]:

$$I(t) = \mathfrak{F}^{-1}\{Y \cdot \mathfrak{F}\{V\}\} \quad I(t) = \mathfrak{F}^{-1}\{Y\} \star V \quad (6)$$

where $\star$ is the time-convolution operator. The second identity then follows from the first using the convolution theorem [135]. This explains why network parameters *completely* describe the external behavior of LTI subcircuits [16].

The set of ports and the set of terminals form the edges and vertices, respectively, of a graph. This graph may not contain cycles because otherwise the excitation vector would contain redundancies. If the ports form a spanning tree over the set of terminals, within this thesis, the network parameter representation is called *exhaustive*. In non-exhaustive representations, only a subspace of the possible terminal-excitations are characterized by the network parameters. For example, fig. 6 (b) is exhaustive, whereas fig. 6 (a) is not: In fig. 6 (a), the response to a current externally forced from T3 to T4 is not included in the network parameter description. However, assume the current-response of circuit #1 to port 3 in fig. 6 (b) is zero for all frequencies. In this case, the characterizations fig. 6 (a) and (b) are equivalent, and circuit #1 is called a *true 2-port network*. Finally, the term *common-reference* network parameters is introduced: It refers to all ports sharing the same reference, as exemplified in fig. 6 (c).

Fig. 7 (c) shows the general small-signal equivalent circuit of 2-port Y-parameters¹⁴. This is merely a circuit representation of eq. (5). Note that the voltage-controlled current sources have complex-valued and frequency-dependent gains and therefore cannot be directly realized in a transient circuit simulation (see sec. 2.3). In contrast, AC-simulations can directly work with network parameter data in a tabular format.

In the following some important properties of network parameters are defined:

Reciprocity It can be shown that network parameters of subcircuits consisting exclusively of resistors, capacitors, inductors and inductive couplings satisfy $Y = Y^T$, $Z = Z^T$ et cetera. This property is also known as reciprocity [16]. More general, network parameters obtained from solutions of Maxwell's equations are reciprocal as well if the materials are isotropic [182]. However, in general, reciprocity is not satisfied for subcircuits containing transistors. It is worth taking a look at small-signal equivalent circuits of reciprocal network parameters: Fig. 7 (a) demonstrates how reciprocal common-reference Y-parameters are canonically mapped to a circuit of impedances without internal nodes. Moreover, fig. 7 (b) and (d) show how reciprocal Z-parameters can be interpreted as a circuit of generalized impedances and couplings without internal nodes. These equivalent circuits are useful for converting Y-, C- and L-matrices from field simulators into networks of lumped resistors, capacitors and inductors (sec. 2.5, sec. 3.3.3, sec. 5.2.4).

Passivity The power output P of a subcircuit can be defined as follows:

$$P = - \int_{-\infty}^{\infty} I(t) \cdot V(t) dt \quad (7)$$

where $V(t)$ and $I(t)$ are the time-dependent port-currents and -voltages in a vectorial form as defined above. By applying Parseval's theorem and eq. (5), and using $Y(-f) = \overline{Y(f)}$ and $\hat{V}(-f) = \overline{\hat{V}(f)}$, one obtains:

$$P = - \int_0^{\infty} \hat{V}(f)^H \cdot (Y(f) + Y(f)^H) \cdot \hat{V}(f) df \quad (8)$$

where $\star^H$ denotes the Hermitian conjugate. Eq. (8) allows to speak of the power output at a frequency f , i.e. $-\hat{V}(f)^H \cdot (Y + Y^H) \cdot \hat{V}(f)$. A subcircuit is called *passive* if and only if $P \leq 0$ holds for any excitation $V(t)$. Using eq. (8)

¹⁴ The generalization to an N -port network and the analogon for Z-parameters is a simple exercise for the reader.

it can then be derived that the subcircuit is passive if and only if the hermitian part of Y , i.e. $\frac{1}{2}(Y + Y^H)$, has only non-negative eigenvalues. And thus ¹⁵:

$$\begin{aligned} \text{passive} &\Leftrightarrow Y(f) \text{ is positive semidefinite at all frequencies} \\ &\Leftrightarrow Z(f) \text{ is positive semidefinite at all frequencies} \end{aligned}$$

Charge conservation and reference independence Consider the port definition in fig. 6 (d), which, within this thesis, will be called *foreign-reference*. This is a common-reference representation in which the reference is not a terminal. Since all AC terminal currents must sum to zero due to Kirchhoff's current law, the row sum of the matrix $Y(f)$ must equal zero [16]. This property is called charge conservation. Moreover, an AC voltage offset common to all ports may not change the response of subcircuit #2 because its behavior is a function of the terminal voltage differences only. Therefore, columns of $Y(f)$ must sum to zero. This symmetry is called reference independence. Charge conservation and reference independence can be violated, because of numerical errors or due to measurement artifacts. In addition, they can be are violated if subcircuit #2 is not a proper subcircuit, i.e. if there is a hidden current path from the inside to the simulator ground. Reference independence and charge conservation are dual properties for reciprocal networks, in the sense that with $Y = Y^T$ a zero row sum follows from a zero column sum and vice versa. Note that charge conservation and reference impedance imply a zero determinant of Y , and hence the Z-parameters are undefined.

In the following, other network parameter representations are introduced:

S-Parameters The S-parameters or *scattering parameters* for the reference impedance $Z_0 \in \mathbb{R}$ can be defined in terms of Y-parameters [16], [182] ¹⁶:

$$S = (\mathbb{1} - Z_0 Y) \cdot (\mathbb{1} + Z_0 Y)^{-1} \quad (9)$$

They allow for very amenable calculations in RF-engineering because S-parameters of ideal transmission lines with characteristic impedance Z_0 are a diagonal matrix. It can be shown that a network is passive if and only if the so-called power-absorption matrix $\mathbb{1} - S^H S$ is positive semidefinite [23]. As a corollary, $|S_{m,n}| \leq 1$ holds for a passive network, which can be an advantage in numerical processing (see also sec. 2.4.2). Moreover S-parameters are

¹⁵ One might naively think that a passive non-linear circuit only exhibits passive linearizations. However, this is not true in general.

¹⁶ A generalization of S-parameters allows for the reference-impedance to differ among the ports, i.e. Z_0 is an arbitrary diagonal matrix. In this case, eq. (9) does not apply but must be generalized [16], [182].

usually well-defined full-rank matrices. In contrast, the components of Y and Z parameters can approach infinity at resonance frequencies or even at DC, and Y -parameters are almost singular matrices in cases as simple as a series inductance (sec. 2.4.2). On the downside, eq. (9) implies that S -parameters suffer from cancellation if the Y -parameters strongly differ from Z_0^{-1} .

Hybrid Parameters Assume an N -port network where ports are divided into two disjoint groups: The first N_e ports form the first group, and the subsequent $N_i = N - N_e$ ports from the second group. The defining equations of Y - and Z -parameters then read:

$$\begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{pmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{pmatrix} \cdot \begin{pmatrix} V_e \\ V_i \end{pmatrix} \quad \begin{pmatrix} V_e \\ V_i \end{pmatrix} = \begin{pmatrix} Z_{ee} & Z_{ei} \\ Z_{ie} & Z_{ii} \end{pmatrix} \cdot \begin{pmatrix} I_e \\ I_i \end{pmatrix} \quad (10)$$

where $V_e, I_e \in \mathbb{C}^{N_e}$ and $V_i, I_i \in \mathbb{C}^{N_i}$ are vectors of the ports' AC-voltages and -currents. These relations can be equivalently written in terms of certain network parameters with mixed units:

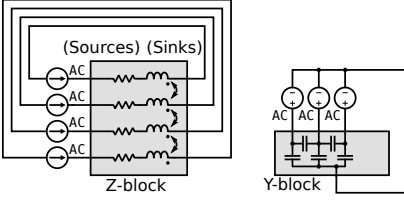
$$\begin{pmatrix} V_e \\ I_i \end{pmatrix} = \begin{pmatrix} H_{ee} & H_{ei} \\ H_{ie} & H_{ii} \end{pmatrix} \cdot \begin{pmatrix} I_e \\ V_i \end{pmatrix} \quad \begin{matrix} [H_{ee}] = \Omega & [H_{ei}] = 1 \\ [H_{ie}] = 1 & [H_{ii}] = \Omega^{-1} \end{matrix} \quad (11)$$

This entries of this matrix are called *hybrid parameters* or *H-parameters*. In this representation, the first group of N_e ports are called Z -ports, and the second group of N_i ports are called Y -ports. H_{ee} is also called the Z -block of the hybrid parameters, and H_{ii} is called the Y -block. Formulas for computing hybrid parameters from Y - or Z -parameters as given in [150].

Hybrid parameters are a canonical representation for networks that decompose into series impedances with comparatively large shunt impedances, e.g. as in electrically small parasitic RLCK-networks (see sections 2.5.2, 3.2.2 and 3.3.3): Fig. 8 (b) exemplifies an arbitrary network of exhaustively coupled inductors and resistors that is shunted by an arbitrary capacitor network. In its hybrid-parameters, H_{ee} represents the inductors and resistors (RLK), whereas the capacitor (C) network is represented by H_{ii} . The mixed blocks, which satisfy $H_{ei} = -H_{ie}$ for reciprocal networks, are adjacency matrices that encode the connection between the RLK- and the C-part.

ABCD-Parameters Assume two subcircuits with port-definitions as shown in fig. 6 (a). When connecting port 2 of the first subcircuit to port 1 of the second subcircuit, a new 2-port subcircuit is formed. This operation is called cascading. There are representations of network parameters, for which cas-

(a) Port definitions for the Y-parameters of the Y-block (exhaustive, common-ref.) and the Z-parameters of the Z-block



(b) Port definitions for H-parameters (exhaustive, common-ref.) of the composite system

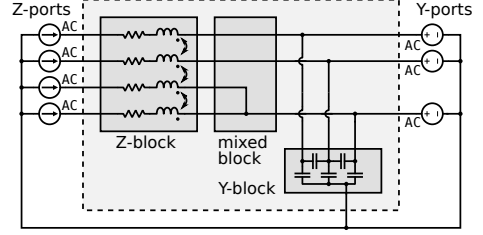


Figure 8: (b) shows an equivalent circuit of hybrid parameters with exhaustive, common-reference port definitions, in which the mixed blocks H_{ei} and H_{ie} are (signed) binary matrices and $H_{ei} = -H_{ie}$. The Z-block in (b) is a true 4-port network, the Z-parameters of which equal H_{ee} w.r.t. the port definitions in (a). Similarly, the Y-block in (b) exhibits common-reference Y-parameters equal to H_{ii} .

cading is equivalent to a matrix multiplication. Among them are the so-called ABCD-parameters, which are defined as follows [135]:

$$\begin{pmatrix} V_{out} \\ I_{out} \end{pmatrix} \cdot \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = \begin{pmatrix} V_{in} \\ -I_{in} \end{pmatrix} \quad (12)$$

where $a_{11}, a_{12}, a_{21}, a_{22} \in \mathbb{C}$, and where V_{in}, I_{in} (resp. V_{out}, I_{out}) are the AC voltage and current at port 2 (resp. port 1). Formulas for conversion from and to Y- and Z-parameters can be found in literature [135]. ABCD parameters are well suited for the description of transmission lines, and they can be used for the extraction of their RLCG parameters [41], [162]. This will be used in sec. 4.4.

Eq. (12) defines ABCD parameters for 2-port networks. They can be generalized to $2n$ -port parameters, which then have n input ports (conventionally drawn on the right side) and n output ports. To define multiport ABCD-parameters, eq. (12) is reinterpreted, such that $a_{11}, a_{12}, a_{21}, a_{22}$ become $n \times n$ complex matrices, and V_{in}, V_{out} (resp. I_{in}, I_{out}) become vectors of AC voltages (resp. currents) at the input and output ports. Note that the arithmetic form conversion formulas from Y- and Z-parameters to ABCD parameters does not carry over, and must be changed in the multiport case. A summary of these conversion formulas can be found in [150].

2.4.2 Network Parameters in Circuit Simulation

As anticipated in sec. 2.4.1, a network parameter representation can be easily instantiated as a subcircuit in AC-simulations¹⁷ This section will describe how network parameter datasets can be included in transient simulations.

There are two classes of approaches: The first one tries to realize the frequency-dependent and complex-valued controlled sources and impedances in fig. 7 (c) using synthesized filters [7], [65]. Such methods are known under the names *reduced-order (macro)models*, *linear macromodels* or simply *vector fitting* [1], [31], [68]. This terminology tries to indicate that the number of state variables in the resulting model is much smaller than in the characterized, original system. The second class of approaches numerically evaluates the convolution in eq. (6) [80], [99]. Despite convolution methods offer advantages in accuracy [192], they also have their own distinct numerical disadvantages [93], [125]. Moreover, in contrast to reduced-order macromodels, convolution methods require direct support by the circuit simulator, and this is only provided by few simulators. Therefore, convolution methods are beyond the scope of this thesis.

It can be shown that any linear lumped element model has network parameters $Y_{m,n}$, $S_{m,n}$ or $Z_{m,n}$ (in the following called $P_{m,n}$) which are rational functions of the frequency [16]. Additionally, most real-world systems like printed-circuit boards, cables and transformers can be approximated by rational functions with rather few poles. This gave rise to the idea of fitting individual components $P_{m,n} \in \mathbb{C}^{N,N}$ to rational functions of the following form [1]:

$$P_{m,n}^{(\text{fit})}(\omega) = c_{m,n} + \sum_{l=1}^{q_{m,n}} \frac{k_{m,n,l}}{i\omega - p_{m,n,l}} \quad (13)$$

where $c_{m,n} \in \mathbb{R}$ are the constant terms, $k_{m,n,l} \in \mathbb{C}$ are the residuals and $p_{m,n,l} \in \mathbb{C}$ are the pole locations in the complex plane¹⁸. Poles are constrained to appear in complex conjugate pairs, which reflects the property that $\mathfrak{F}\{P\}$ must be real valued. Rather primitive implementations of reduced-order macromodels then directly use such a per-component rational fit for filter synthesis [7]. More advanced implementations simultaneously fit multiple components of $P_{m,n}$ with a common set of poles in the so-called state-space

¹⁷ A source of numerical error is the interpolation of network parameters between the sampled frequencies. This can be avoided by making the frequency points in the AC simulation equal to frequency points in the network parameter dataset.

¹⁸ All poles must be *stable* which means that $\text{Re}(p_{m,n,l}) < 0$ [1], [68]. This nomenclature is confusing because stable poles do *not* guarantee a stable transient simulation – rather, passivity enforcement does. A more proper term would be *causal* poles since $\mathfrak{F}^{-1}\{P_{m,n,l}\}$ is zero for $t < 0$ if and only if all poles satisfy $\text{Re}(p_{m,n,l}) < 0$ [118].

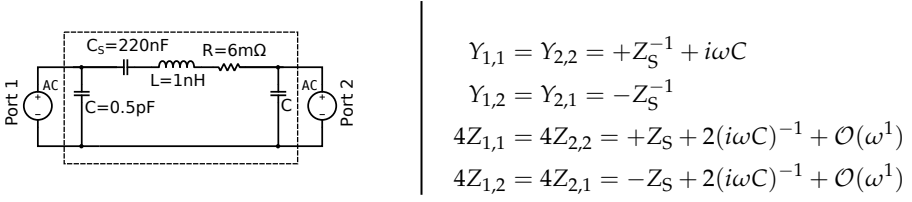


Figure 9: Y- and Z-parameters of a 220 nF 0805 SMD capacitor on a typical 4-layer PCB including its ESR, ESL and the pad parasitic capacitances. (here: $Z_S = R + i\omega L + (i\omega C_S)^{-1}$).

formulation [1]. This allows for a much smaller total number of poles. Since each pole corresponds to a state variable in the synthesized circuit, thereby, a more compact equivalent circuit is obtained. Different methods have been proposed to simultaneously fit $P_{m,n}$ with a minimum number of states n , notably *vector fitting* [68]¹⁹ and *complex frequency hopping* [1].

Any curve fitting procedure requires that a scalar quantity is defined and made subject to minimization. This fit deviation might be defined as the maximum or the sum over the individual network parameters' fit deviations, which are computed by applying a function norm to $P_{m,n}(f) - P_{m,n}^{(\text{fit})}(f)$. For example, this function norm might be an RMS-norm in logarithmic or linear units and with logarithmic or linear frequency weighting. Other authors have proposed to instead define the fit deviation in eigenspace [67], but apparently this is not widely used. In practice, point-wise errors of the fit-result in the range of 0.1% to 10% must be expected from the fitting procedure [68].

Passivity enforcement [66] is a post-processing step which tweaks the fitted state space representation such that the reduced-order macromodel is passive at all frequencies. It is well known [64] that reduced-order macromodels must be passivity-enforced, for otherwise stable transient simulations cannot be guaranteed (see also sec. 2.3.2). Hence, passivity enforcement should be considered mandatory. Detrimental passivity violations of fitted reduced-order macromodels may occur for frequencies in-between frequency samples and especially for out-of-band frequencies, even if the input dataset is passive [64]. Different passivity enforcement methods exist, some of which do only provide heuristical guarantees of passivity [66]. The state-of-the-art tool IDEM [31] provides an advanced passivity enforcement method called Hamiltonian passivity enforcement [64]. Note that passivity enforcement can significantly worsen the accuracy of the initial fit (sec. 3.2.3).

Of course, fit errors are by orders of magnitude larger than numerical or measurement errors in the network parameter dataset, which is one reason why reduced-order macromodels should be used with caution. Fig. 9 shows a

¹⁹ Open source implementations of the algorithm are readily available [69].

simple example where these fit errors lead to problems in simulations: If a Y-parameter representation is chosen, the pad capacitances C are only encoded in $Y_{1,1}$ and $Y_{2,2}$. However, for frequencies $f \ll f_R = \frac{1}{2\pi\sqrt{LC}} = 7.1 \text{ GHz}$, the magnitude of $Y_{1,1}$ and $Y_{2,2}$ is strongly dominated by $Z_S^{-1} \approx (i\omega L)^{-1}$. If a fit error of 1% is assumed, then for $f < f_R \cdot 1\% = 71 \text{ MHz}$ the information about C in Y vanishes in the fit error. Conversely, if the Z-parameters are fitted, as can be seen in the equations in fig. 9, for $f \ll \sqrt{2}f_R$, the series impedance Z_S is strongly affected by fit errors. Therefore, neither Y- nor Z-parameters can capture both the ESL and the pad capacitance in this case. In its essence, this error is due to the fact that the Y- and Z-parameters are approximately low-rank for $f \ll f_R$ (sec. 2.4.1), and the information about C or L , respectively, is encoded in the subordinate eigenvalue. This observation generalizes to electrically small parasitic RLCK-networks. S-parameters with the optimum $Z_0 := \sqrt{|L/C|}$, generally perform better than Y- and Z-parameters, but they also suffer from cancellation errors for electrically small networks. This has important implications on the vector fitting of package models (sec. 3.2.3). It must be understood that no parameter representation truly universal, and the representation must be properly chosen to match the use case. This shows that reduced-order macromodels are not truly a “black-box method”.

Besides accuracy issues due to fitting and passivity enforcement, reduced-order macromodels often cause instabilities in transient simulation (see sec. 2.3.2): Reduced-order macromodels are abstract mathematical models. Thus, when used to synthesize circuits, the units of electrical nodes and branches do not represent physical quantities, which can defeat the LTE-criterion as well as the Newton convergence criterion. The latter might be fixed by implementing the filters using simulator features, e.g. as Laplace-filters operator in Verilog-A. To be on the safe side, a constant time step might be enforced²⁰, which disables the LTE-criterion. If iterative linear solvers are used, yet more severe issues might arise because, different from the Newton’s method, their convergence criterion may not simply neglect the filters’ internal states. Therefore, this thesis strongly recommends that the combination of iterative linear solvers and reduced-order macromodels in transient simulations is avoided. Other causes of instabilities are non-physical sharp HF-resonances at out-of-band frequencies.

²⁰ However, this is a burden to the user, and it results in compute-performance degradation because a suboptimal time step is used.

2.4.3 On-Wafer-Measurements using Vector Network Analyzers

Vector Network Analyzers (VNA) are instruments that measure network parameters in amplitude and phase [124], [176]. The frequency range of commercially available VNAs for radar applications can be up to 100 GHz [87].

Fig. 10 illustrates a typical measurement setup for on-wafer measurements with two ports. The device under test (DUT), which can be an active circuit (i.e. powered transistors) or a passive circuit (e.g. metal strips), and the metal interconnect that connects it to the pads were processed in semiconductor fabrication plant. This test structure is electrically contacted by means of two ground-signal (GS) wafer probes [51], [124]. The ground pins (G) of the wafer probes are connected to the shield of the coaxial cable, whereas the signal pins (S) are connected to the coaxial cable's central conductor. The coaxial cables connect the wafer probes to the vector network analyzer.

After the measurement was started, the vector network analyzer activates one port at a time. The activated port will then be driven by a low amplitude sinusoidal excitation with the characteristic impedance, and a frequency sweep will be performed between the selected minimum and maximum frequency. Meanwhile, the power wave incident to all ports of the VNA will be measured in amplitude and in phase relative to a reference phase of the excitation. [176] The so-obtained table of complex numbers are the *raw* S-parameters.

Observe that the macroscopic, parasitic system consisting of cables, connectors, wafer probes may be many orders of magnitude larger than the DUT itself, for example, in terms of its capacitance. Therefore, the *raw* S-parameters contain enormous frequency-dependent offset-, phase- and scaling-errors. These must be removed by calibration. The calibration terms depicted by the red arrows in fig. 10 correspond to the 8-term error model (also known as

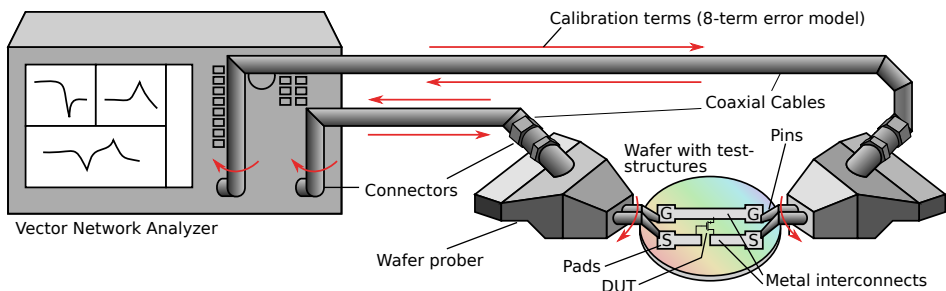


Figure 10: Presentation of the principles of a 2-port on-wafer measurement using a vector network analyzer.

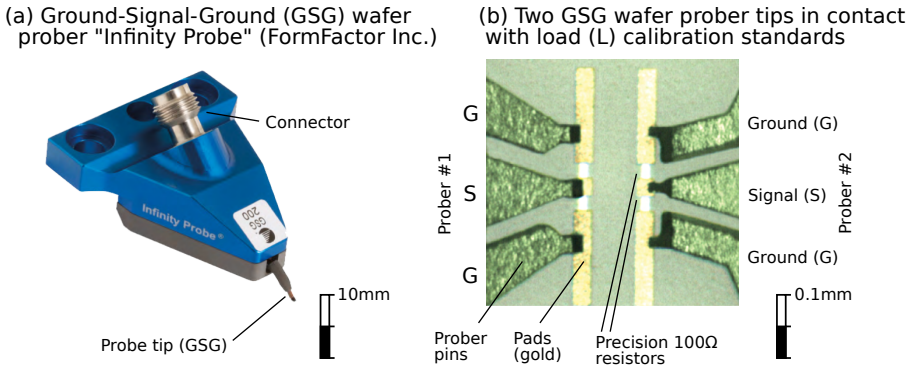


Figure 11: (a) Macroscopic and (b) microscopic photos of ground-signal-ground (GSG) wafer probers. Reprinted from [51].

7-term error model or error boxes) [126]²¹. The 8-term error model stores two S-parameter datasets, i.e. one for each port, which, in this case, characterize the connectors, cables and wafer probers including their pins. The calibration correction then removes these S-parameter datasets from the raw S-parameters by an inverse cascading operation (see sec. 2.4.1) [126]. This is typically done by the firmware of the VNA, but it can also be done offline in software²².

In order to obtain the calibration terms, a number of calibration measurements must be performed. For example, fig. 11 (b) shows a photo of two wafer probe tips, each touching down on a 50 Ω termination. There is a large number of different calibration techniques, most notably SOLT (Short-Open-Load-Thru) and TRL (Thru-Reflect-Line) [124], [176]. The SOLT calibration technique requires four calibration standards, namely short-circuited pads (SHORT), unconnected pads (OPEN), a 50 Ω termination (LOAD) and a through-connection of both ports (THRU). No calibration standard is ideal – for example the SHORT-standard has a frequency-dependent parasitic series inductance [176]. Those non-idealities are provided by the calibration substrate manufacturer, and must be set up correctly in the VNAs. After the calibration measurements are completed, extreme caution must be taken in order not to perturb the measurement system. For example, a change of the ambient temperature, a movement of the cables or opening of the connectors may void the calibration [176].

²¹ Modern VNAs are rather based on the 12-term error model, which also allows to correct crosstalk between the ports and asymmetries in the VNA's samplers [124], [126].

²² Scikit-RF [184] is an excellent tool for the processing of network parameters, and it also supports offline calibration.

Calibration can only remove the parasitics up to the point in the transmission chain where the calibration standards were connected. More concisely, this point is called the *reference plane* or *calibration plane*. For example in fig. 10, the calibration was performed up to, but not including the pads on the wafer. The removal of additional parasitics from the measured data, in this case parasitics of the pads and of the metal interconnects, is called *de-embedding* [176]. This is achieved by characterizing certain dummy structures [124], [133]. There is a large variety of de-embedding approaches, which differ accuracy and in the applicable frequency range.

2.5 Electromagnetic Field Simulation Techniques

Electromagnetic field simulation is the solution of the Maxwell's equations, or subsets thereof, using numerical software. In many cases, the electromagnetic field simulation must be connected to a circuit simulation. This can be achieved using a variety of approaches: One approach numerically solves the full time-harmonic form of Maxwell's equations [182] or subsets of Maxwell's equations, which yields network parameters [82], [101]. These are then connected to the circuit simulation as described in sec. 2.4.2. Another approach numerically solves multiple quasistatic approximations of Maxwell's equations and combines the resulting resistance, capacitance and partial inductance matrices into a lumped-element model [84], [96], [137]. This is called parasitic extraction.

2.5.1 Obtaining Network Parameters from Field Simulation

There are various tools [82], [101] that discretize the full Maxwell's equations using the finite-element method (FEM) or the boundary elements method (BEM). In FEM, the boundary of the system is then typically a box finite size, whereas in BEM the domain extends to infinity. If radiation is not of interest, the choice of these boundary conditions is typically not very relevant.

The most simple type of excitations are *lumped ports* [82], which is depicted by red rectangles in fig. 12. At these rectangles, a constant current density, which points from the reference conductor to the terminal conductor, is prescribed. The voltage response at port #3 and #4 is quantified by integrating the E -field over the path P_3 and P_4 , respectively, in fig. 12 (b) ²³. Then, in a similar fashion to S-parameter simulation in SPICE-like simulators (sec. 2.3.3), the network parameters are computed over a given frequency range.

²³ To be more specific, it must be averaged over the whole sheet area, for otherwise the resulting network parameters would slightly violate reciprocity.

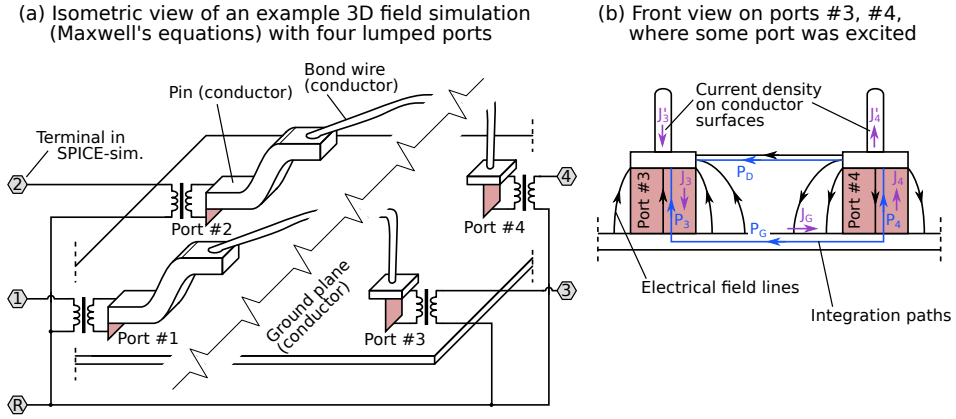


Figure 12: Simplistic example of a 3D field simulation (not to scale) that solves the time-harmonic form of Maxwell's equations, under excitation by so-called lumped ports (red rectangles). Here, all ports are referred to the PCB ground plane. When included in a circuit simulation, the circuit interfaces with the EM-system via the terminals R, 1, 2, 3 and 4 (gray hexagons in (a)).

To include the resulting network parameters in a circuit simulation (sec. 2.4.2), the electromagnetic model with N lumped ports is represented by an $(N + 1)$ -terminal subcircuit. The semantics of this construction are as illustrated in fig. 12 (a): As symbolized by the ideal transformers connecting SPICE-terminals and lumped ports, a current I_k entering terminal # k in the SPICE-simulation will cause a reaction corresponding to an injection of $+I_k$ into the terminal conductor and $-I_k$ into the reference conductor, e.g. the ground plane. Moreover, the semantics of the terminal voltage # k , measured relative to the terminal R, is the integral of the E -field towards the ground plane.

Also the voltage difference between two close terminals has a meaningful interpretation in terms of a line-integral over the E -field: For example, the voltage difference between terminals #3 and #4 approximately equals the integral of the E -field over the path P_D in fig. 12 (b). This is entailed by the following approximations: Firstly, if the loop formed from P_3 , $-P_4$, P_G and $-P_D$ is sufficiently small, then the integral of the E -field over this loop is almost zero. Secondly, the integral of the E -field over P_G is approximately zero because the ground plane is a good conductor. More generally, for a group of close lumped ports, the electric field can be approximated as locally curl-free, and one can assume a local electric potential $\phi_{loc.}$ with $E \approx -\nabla\phi_{loc.}$. This potential is zero at the reference conductor by convention. Then, the terminal voltages can be interpreted as values of $\phi_{loc.}$ at the conductors interfaced by these lumped ports.

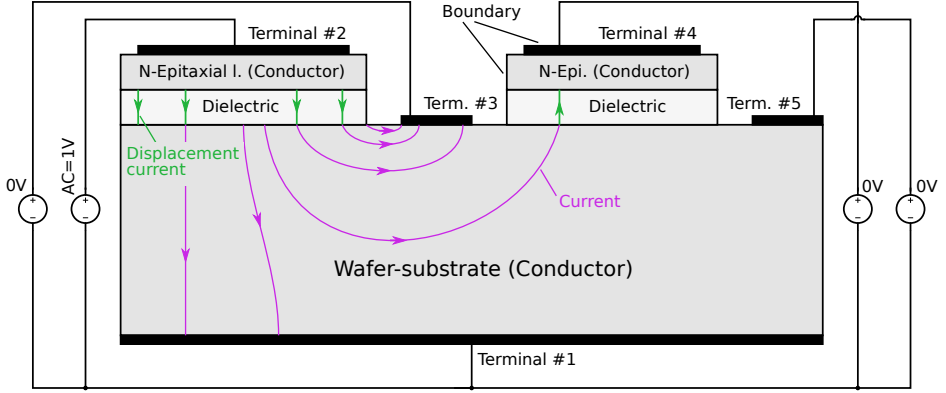


Figure 13: Field simulation of the 2D AC-conduction equation. This example depicts the wafer-substrate with multiple n-epitaxial pockets on top. A thin dielectric layer emulates the capacitance of the p-n-junction (see also sec. 5.1.2). The five terminals of this system are grouped to four ports (exhaustive common-reference characterization; sec. 2.4). The depicted current and displacement current fields visualize a voltage excitation of terminal #2, which is used to compute the first column of the Y-parameter matrix.

If the approximation $\partial B / \partial t \approx 0$ is applied to the Maxwell-Faraday equation, i.e. if induction is neglected, then one arrives at the AC conduction equation [83], [97]. In the time-harmonic form, and expressed in terms of the electric potential ϕ , it reads:

$$\nabla \cdot \underbrace{((\sigma + i\omega\epsilon_0\epsilon_r) \nabla \phi)}_{:= J_F + J_D} = 0 \quad (14)$$

where ϵ_r and σ are location-dependent, J_F is called the free current and J_D is called the displacement current. Special cases of this equation include electrostatics ($\sigma = 0$) and DC conduction ($\epsilon_r = 0$). It reduces to Laplace's equation if σ and ϵ_r are constant in x , y and z .

Since the electrical field is curl-free in the AC conduction problem, integrals over the electric field are path-independent, and a construction akin to lumped ports is not required. Instead, terminals are associated with patches of the boundary where typically a constant Dirichlet boundary condition for ϕ is used. The ϕ -field at these patches is then equated with the terminal's voltage, and the terminal current is defined as an integral of $J_F + J_D$ over this patch. This is depicted in fig. 13. The remaining non-connected part of the boundary typically has a Neumann boundary condition which enforces that no current $J_F + J_D$ is leaking.

As exemplified in fig. 13, the network parameters are typically [83] obtained using exhaustive, common-reference port definitions. For this purpose, some

terminal must be selected as a global reference ²⁴. In the special case of DC conduction ($\epsilon_r = 0$), the resulting Y-parameters are frequency-independent, real-valued and reciprocal, and thus can be converted into a lumped resistor circuit by the equivalent circuit from fig. 7 (a) in sec. 2.4.1. In the special case of electrostatics ($\sigma = 0$), the *capacitance matrix* defined as $C := Y/i\omega$ is frequency-independent, real-valued and reciprocal. Similar to DC-conduction, the capacitance matrix C can be converted into a lumped capacitor circuit using the construction from fig. 7 (a).

2.5.2 Parasitic Extraction for IC-Packages and PCBs

This section develops an understanding of parasitic extraction tools for IC-package and PCB applications. Widely-known implementations are FastCap [137], FastHenry [96] and Ansys Q3D [84] ²⁵. The theoretical underpinning will be described in terms of the potential formulation in Lorentz gauge [182], which is equivalent to the microscopic Maxwell's equations – here, in their time-harmonic form:

$$\nabla^2 \phi + \frac{\omega^2}{c^2} \phi = -\frac{\rho}{\epsilon_0} \quad \nabla^2 A + \frac{\omega^2}{c^2} A = -\mu_0 J \quad (15)$$

where $\phi : \mathbb{R}^3 \rightarrow \mathbb{R}$ is the electric potential and $A : \mathbb{R}^3 \rightarrow \mathbb{R}^3$ is the so-called magnetic vector potential. The electric field E and the magnetic field B relate to ϕ, A as follows:

$$E = -\nabla \phi - i\omega A \quad B = \nabla \times A \quad (16)$$

This formulation allows to define a potential between two points p_1, p_2 as the difference $\phi(p_1) - \phi(p_2)$, which is independent of an integration path, despite the E -field is not curl free. Moreover, it is mathematically non-contradictory, even if the current field J violates the continuity equation eq. (17) in some areas, i.e. it allows to sink and source charges in an “non-physical manner”:

$$\nabla \cdot J = -i\omega \rho + J_{\text{source}} \quad (17)$$

Observe that eq. (15) reduce to simple Laplace's equations as in electrostatics if the terms $\omega^2/c^2 \phi$ and $\omega^2/c^2 A$ are dropped. These terms are responsible for time-of-flight delays in response of the ϕ and A -fields to a change in ρ and J , also known as *retardation* [158], [159]. Neglecting retardation is clearly

²⁴ This is just a formality and does not change the information content of the network parameters. Some simulators may also allow for the foreign-reference convention.

²⁵ The nomenclature in this section is mostly inclined towards Q3D.

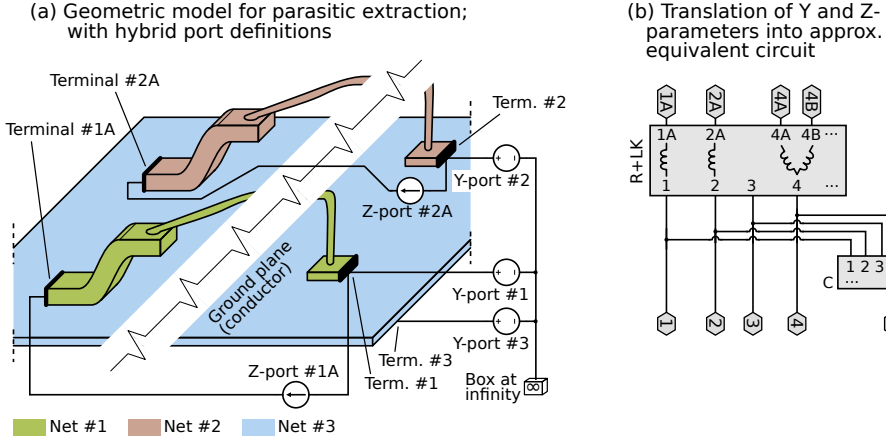


Figure 14: Application of parasitic extraction to the IC-package model from fig. 12: Part (a) shows the division of the 3D geometry into nets, the definition of terminals and the port definition scheme for the terminal-based H-parameters. The capacitances connecting to ∞ in (b) are also known as *self capacitances*. The net #4 in (b) is a multi-terminal net that is not shown in (a) for clarity.

well justified if the system is electrically very small. Counterintuitively, if retardation is neglected, radiation in free space is eliminated, but the wave-propagation of TEM-modes is still described very well. Therefore, e.g. ADS Momentum suggests to neglect retardation effects even up to $\lambda/2$ [101], and some researchers [54] have successfully applied this approximation even to *electrically very large* PCB structures.

Description of the parasitic network using hybrid parameters As depicted in fig. 14 (a), in the discussed framework, the conductors are divided into multiple disjoint regions, hereinafter referred to as *nets*. An arbitrary number of terminals can be placed on the surface of a net [84]. The process of calculating parasitic elements is best understood in terms of the hybrid-parameters (sec. 2.4.1) with the port definition in fig. 14 (a): That is, an Y-port is attached to each net, and its reference is the “voltage at infinity”²⁶ [84], [159]. Furthermore, at each net with N terminals, a number of $N - 1$ Z-ports are attached in an exhaustive, common-reference style. As explained above, the voltage across these ports is defined as a difference in electric potential ϕ , and currents across these ports leads to charge carriers being sunk and sourced at two different points in space. This is very different from the electromagnetic field simulation based on lumped ports (sec. 2.5.1), where

²⁶ This is defined as follows: The system is enclosed by a cavity of diameter D with a perfectly conducting boundary, the voltage of which is called “voltage at infinity”. Then, the limit value $D \rightarrow \infty$ is considered.

the voltage was based on the E -field and the continuity equation was not violated, i.e. $J_{\text{source}} = 0$ in eq. (17). Therefore, for disambiguation, these network parameters will be denoted by the term *terminal-based H-parameters* in the following.

Computing the capacitance, resistance and partial inductance matrices The Y-block of the terminal-based H-parameters H_{ii} is obtained by applying AC voltages at the Y-ports one by one while sampling the AC current response at all Y-ports. For sufficiently small nets, and if retardation terms in eq. (15) are neglected, this reduces to electrostatic equations. Therefore, H_{ii} can then be calculated at an arbitrary frequency and can then be converted to a frequency-independent capacitance matrix C as explained in sec. 2.5.1. Similarly, the Z-block of the terminal-based H-parameters H_{ee} is obtained by applying AC currents at the Z-ports one by one. This task, however, does typically *not* reduce to magnetostatic equations because the diameter of the nets are larger than the skin depth at the maximum frequency [84]. There are multiple approaches for computing H_{ee} at a given frequency f in a quasi-magnetostatic approximation, disregarding for retardation and for the surrounding dielectric. (These details [32], [84], [96] are beyond the scope of this thesis.) In general, $H_{ee}(f)$ can be decomposed into the resistance matrix R and the *partial inductance matrix* $L^{(P)}$ [157], both of which are frequency-dependent:

$$R(f) := \text{Re}(H_{ee}(f)) \quad L^{(P)}(f) := \frac{\text{Im}(H_{ee}(f))}{2\pi f} \quad (18)$$

The resistance matrix and the partial inductance matrix can be calculated at DC, or at some fixed frequency. Alternatively, $L^{(P)}$ and $R/\sqrt{f}$ can be calculate in the high-frequency limit [84]. The choice of a suitable frequency f for the resistance and inductance computation is important, and is subject to further discussion below. It is worth mentioning that when solving these quasi-magnetostatic differential equations for $f > 0$, not only the currents in the excited net but also the currents in all other conductors must be included. Currents in the other conductors form closed paths. These so-called *eddy currents* [84], [193] are required to describe effects like magnetic shielding, return currents in the ground plane, eddy current losses and the proximity effect.

Equivalent circuit of the terminal-based H-parameters Parasitic extraction yields an RLCK circuit model, which is obtained as follows: As shown in sec. 2.4.1, if the mixed blocks of the terminal-based H-parameters are approximately binary matrices, the construction from fig. 8 can be used. This

is satisfied if the nets are electrically small. The result is the RLCK-circuit shown in fig. 14 (b): It consists of two blocks “C” and “R+LK”, which are equivalent-circuits of $H_{ii} = 2\pi ifC$ and $H_{ee} = R + 2\pi ifL^{(P)}$, respectively. They are constructed from the C-, R- and $L^{(P)}$ -matrix using fig. 7 (a) and (b), respectively.

Semantics of the terminal-voltages and -currents As discussed above, the semantics of port-voltages and -currents are very different from field simulation based on lumped ports. For example, if an AC current is applied between terminal #3 and #1 in fig. 12, then a closed current loop is excited across the lead-frame parts, the bond-wire and the ground plane. The voltage observed between terminals #3 and #1 will be proportional to the corresponding *loop inductance*. Conversely, if a current is applied between terminal #1 and #1A in fig. 14 (b), the reaction will be equivalent to an open current path that is not returned over the ground plane. Here, the currents in the ground plane are merely eddy currents (see also sec. 3.3.1). The voltage observed between terminals #1 and #1A will reflect the corresponding *partial inductance*.

In models obtained using parasitic extraction, the *outer system* should ensure that the current paths in the magnetostatic system are approximately closed: That is satisfied, for example, if the terminals form local clusters (e.g. { #1A, #2A } and { 1, 2 } in fig. 14), the total current of which guaranteed to be zero. Then, one may interpret differences between terminal-voltages as potential-differences in a *physically meaningful* local electric potential $\phi_{\text{loc.}} := \phi$ with $E \approx -\nabla\phi_{\text{loc.}}$. In this case, the semantics are identical to electromagnetic field simulation based on lumped ports (sec. 2.5.1), except for the convention regarding the zero potential. For example, in RLCK-extraction of IC-layouts (sec. 2.6), the “outer system” reflects the set of semiconductor devices. As long as the total current into a semiconductor device is zero, the current paths in the quasi-magnetostatic field model are closed. Another example is found in sec. 3.3.3: Here, ideal transformers are applied externally, which enforces that the current-path is properly closed via the ground plane.

Summary of the errors due to the underlying approximations and possible corrective measures

- **No radiation and transmission only in the TEM-mode:** If the retardation terms in eq. (15) are neglected, electromagnetic waves cannot propagate in free space or in hollow waveguides.
- **Removed frequency dependence of R:** If R is obtained at DC, then the conductive losses are underestimated for frequencies above the skin frequency f_{skin} , and the proximity effect is neglected as well. Alternatively, if R is obtained at a fixed frequency $f \gg f_{\text{skin}}$, then losses are

only well-approximated for frequencies close to f_{skin} . Heuristical ladder-model circuits can be used to re-introduce the skin effect in the circuit simulation (see sec. 3.3.3).

- **Removed frequency dependence of L:** Changes in $L^{(P)}$ with f are very significant if planar conductors, e.g. a ground plane, are present: At DC, there are no eddy currents, whereas at sufficiently high frequencies, the eddy currents in the ground plane significantly affect $L^{(P)}$ (sec. 3.3.1). Therefore, $L^{(P)}$ should never be calculated at DC in the presence of a ground plane – instead, a good approximation is the high-frequency limit.
- **Incorrect distribution of C:** In the equivalent circuit fig. 14 (b), the complete capacitance of a net is then concentrated at a single, particular terminal. For frequencies where nets are electrically very small, capacitances C approximately commute with the partial inductances $L^{(P)}$ and the resistances R because $(i\omega C)^{-1} \gg R + i\omega L^{(P)}$. This shows that, in this case, distribution of the capacitances makes almost no difference. However, if the model should be valid for higher frequencies, the construction from fig. 14 (b) might be altered such that capacitances are more evenly distributed along the inductance²⁷. Clearly, this is only a heuristic, which is mostly tailored to transmission lines.

A more physical solution to the incorrect distribution of the capacitance is the subdivision of nets into multiple smaller ones. However, this is impractical for planar conductors because there is no generally valid and simple way to connect these fragments via additional terminals. Hence, in systems with a ground plane, one should restrict the size of the model to $\lambda/10$, e.g. the system should not be larger than about 2 cm for $f_{\text{max}} = 1$ GHz and $c_{\text{eff}} = 2c/3$.

2.6 Parasitic Extraction of IC-Layouts and Post-Layout Simulation

Parasitic circuit elements associated with the metallization can be automatically calculated using so-called *parasitic extraction* tools. Parasitic extraction of IC-layouts is achieved by rather different methods than parasitic extraction of IC-package- and PCB-simulation (sec. 2.5.2): In parasitic extraction of IC-layouts, the level of software automation and the system complexity is much higher, but the accuracy is more limited. These software tools take the circuit

²⁷ For example, the circuit exporter from Q3D by default inserts one intermediate node in each inductor that is then attached to capacitances [84].

schematic as input and augment it with a large number of parasitic elements that are computed using polygonal layout data. The result is a simulatable netlist, which is called the *extracted netlist*. [30]

Since parasitic extraction tools are an integral part of the developed methodology (chapter 4 and sec. 5.2), the state of the art of parasitic extraction will be summarized briefly. Sec. 2.6.1 treats parasitic extraction of the IC metallization. Parasitic extraction tool flows for ICs typically do not support the calculation of parasitic resistors and capacitors that are part of the substrate. However, some vendors have developed tool flows which allows to obtain a simulatable model including substrate parasitics. These tools will be explained in sec. 2.6.2.

2.6.1 Parasitic Extraction of the IC-Metallization

A prototypical fully-automated parasitic extraction flow for IC-layouts is shown in fig. 15. It proceeds in two steps²⁸: In the layout-versus-schematic (LVS) check [131], semiconductor devices from the schematic are linked to device-forming polygons, and polygons corresponding to the metallization are annotated with net names. The result is the layout netlist and the annotated layout in fig. 15 (b), which is electrically equivalent to the schematic in (a). The metal polygons are also associated with junction points, e.g. VCC-Terminal #1 in fig. 15 (b). These define where devices are connected to them, as well as where metal polygons are interconnected. In the second step, the parasitic extraction tool [30] reads the polygon-representation of the metallization and computes its parasitic resistances (R), capacitances (C), partial inductances [157] (L) and/or inductive couplings (K). These parasitic elements are then added to the netlist in fig. 15 (b), which results in the extracted netlist in fig. 15 (c). Depending on the configuration, only a subset of the parasitics are included – for example, RC-extraction includes resistances and capaci-

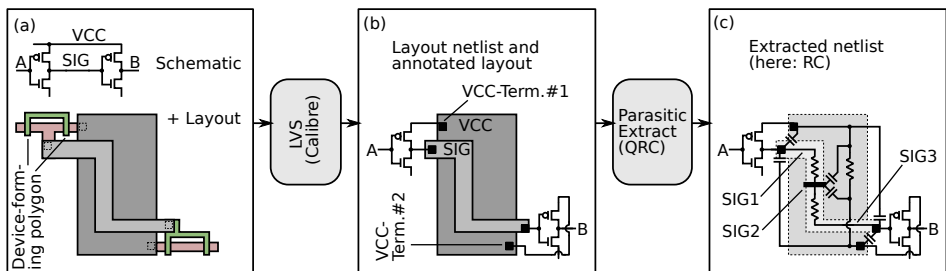


Figure 15: Parasitic extraction flow for IC-layouts using the tools Calibre [131] and QRC [30].

²⁸ This description must be understood as a strong simplification.

tances, whereas RLCK-extraction also includes partial inductances and their couplings [30].

Parasitic extraction tools automatically divide nodes into several sub-nodes, which is called *fracturing* [30]. This is exemplified by SIG1, SIG2 and SIG3 in fig. 15 (c), which are fractures of the node SIG in fig. 15 (b). In fracturing, the node's metal polygons are also subdivided into smaller polygons, and pairs of junction points are introduced at the newly-formed interfaces (see 15 (c) at SIG2). Fracturing is performed by a geometry processing “front-end”, whereas the “back-end”²⁹ is responsible for computing the parasitic elements. The relationship between fracturing and accuracy is quite intricate: Fracturing may *degrade* the accuracy of planar conductors, as explained in sec. 2.5.2. On the other hand, some approximative implementations of the “back-end” may also benefit from fracturing, as exemplified below in the case of QRC's inductance extraction. Moreover, RC- and LC-networks require a certain amount of fracturing in order to be correctly representing the distribution of the capacitance, which is necessary at higher frequencies. Users may exert control over the fracturing by imposing limits on the polygon size.

Resistances and capacitances arise from admittance- and impedance matrices that can be computed by solving DC- and AC-conduction equations in three dimensions. This was treated in detail in sec. 2.5.2. Today's parasitic extraction tools for ICs can achieve RC parasitic extraction of a full-chip quite efficiently [97]. This would not be possible without the following approximations:

- Capacitances between metal segments are neglected for distances larger than a certain cutoff distance. Otherwise the number of capacitances would grow quadratically with the number of metal segments.
- For frequently encountered shapes of metal segments, large lookup-tables of capacitances and resistances are pre-computed. Pattern match and table lookup is preferred over numerical solution of partial differential equations.

In parasitic extraction for ICs, the treatment of partial inductances and their couplings differs strongly from resistances and capacitances: Firstly, if partial inductive couplings are extracted, the resulting netlists are often extremely large because, in contrast to capacitance extraction, long distance inductive couplings cannot be removed using a cutoff distance: Different from the capacitance matrix, the partial inductance matrix typically is *not* approximately sparse, even under perfect conductor assumptions [15], [92].

²⁹ The parasitic extraction tools for IC-package- and PCB-applications (sec. 2.5.2) satisfy the requirements of a “back-end”.

Secondly, as mentioned in sec. 2.2, they are requested less frequently by circuit designers, and thus, the tool flow is of more limited quality.

The most theoretically sound approach computes partial inductances and their couplings by solving a quasistatic limit of Maxwell's equations using BEM or FEM (sec. 2.5.2). This very precise approach even correctly describes eddy currents and return currents in planar conductors. A more computationally efficient approach, which cannot handle eddy currents and planar conductors³⁰, will be outlined in the following: Assume that the interconnect subject to inductance extraction can be fractured into non-branching, path-like metal segments. For a set of non-branching, path-like metal segments, the partial inductance matrix $L^{(P)}$ can be expressed as the following integral (neglecting skin-effect) [92], [96], [157]:

$$L_{i,j}^{(P)} = \frac{\mu_0 \mu_r}{4\pi A_i A_j} \int_{V_i} d^3x \int_{V_j} d^3x' \frac{\vec{v}_i(\vec{x}) \cdot \vec{v}_j(\vec{x}')}{|\vec{x} - \vec{x}'|} \quad (19)$$

where V_k is the volume of the metal segment with index k , and A_k is its cross sectional area, and $\vec{v}_k(x)$ is a unit vector field pointing in the direction of the prescribed current flow. For known cross-sectional shapes, after decomposing the path-like metal segments into a finite number of straight line-like segments, eq. (19) might be solved analytically or using lookup-tables. As will be shown in sec. 4.6, this approach is very similar to the RLCK-extraction code of QRC. However, for an unknown reason, their “back-end” implementation does not properly handle angled path-like segments, and hence requires an unexpectedly high level of fracturing.

RC-extraction usually results in a large number of nodes with very small time constants, which can cause a severe degradation of simulator efficiency. This can be resolved by means of “parasitic reduction” [30], which typically refers to a variant of the TICER algorithm [170], [171]. TICER preserves the DC-resistance, the total capacitance per node as well as the Elmore delay [170].

2.6.2 Substrate Extraction and Substrate Noise Analysis

Substrate extraction [30], [97] is an extension of parasitic extraction for ICs (sec. 2.6.1) which, in addition, augments the netlist with a *substrate model* in circuit form. In the following, the term *substrate model* refers to a physical model including resistive and capacitive parasitics associated with the wafer-substrate, epitaxial layers, wells, deep trenches, sinkers and other sub-

³⁰ Albeit in principle it is possible to describe a ground plane as a “grid of wires” [96], this would require a very small fracture size, akin to a surface mesh in boundary element method calculations. This is clearly intolerable in full-chip extraction.

strate contacts. The term substrate model does *not* encompass the physics of minority carriers, for the reasons given in sec. 2.2. Hence, the forwards bias of parasitic p-n-junctions is *not* correctly predicted by the tools and methods described below.

In *substrate noise analysis*, the substrate model is extracted, and subsequently processed by a specialized non-SPICE simulator. In contrast to substrate extraction, the substrate model is not necessarily in the form of an electrical circuit, and the interface between extractor and simulator is usually invisible to the user. A kind of AC-simulation is performed that includes the substrate, metal interconnect, the integrated circuitry and possibly the IC-package. However, the integrated circuitry is strongly simplified: Logic gates or even larger digital circuit blocks are replaced by “macromodels” consisting of few effective resistors, capacitors and equivalent noise sources. The output of substrate noise analysis tools are noise waveforms or spectra at selected nodes as well as network parameters. For example, the noise waveforms can be used in subsequent transient simulations of presumably sensitive circuitry, and the resulting linear macromodels that include equivalent noise sources can be used in the prediction of RF-emissions. [85], [86], [146]

It is undoubtedly very difficult to realize accurate yet *efficient* simulations of the noise propagation through the substrate. This thesis primarily investigates the efficiency of the substrate model from the circuit simulator’s perspective, whereas the optimization of the substrate model generation is a different research aim: For example, a large part of the related literature essentially develops fast 3D field solvers for computing Y-parameters of the substrate [60], [61], [180], [189]. In the following, the performance of circuit simulation, when applied to an extracted substrate model, is discussed.

The n-epitaxial layer, wells and implants can be approximated as 2D conductors, whereas the wafer-substrate is a 3D structure [168]. Substrate extraction usually describes these 2D conductors using the 2D finite-elements method (FEM) or the 2D finite-difference method (FDM). Then, the associated parasitic elements are created by re-interpreting the resulting equations as a resistor network [196]. However, even this seemingly simple construction can pose a considerable burden on the circuit simulator’s linear solver: For example, the asymptotic run time of a direct sparse solver (sec. 2.3.1) on a homogeneous 2D grid scales with, at least, $\mathcal{O}(N_{2D}^{1.5})$, where N_{2D} is the number of nets in a 2D layer [43], [57].

3D conductors, e.g. the wafer-substrate, could also be converted into resistor networks using the FEM or FDM [95], [185], [196]. In the following, the wafer-substrate model is formally regarded as a subcircuit, which is called *3D substrate netlist*. The terminals of the 3D substrate netlist are surface patches,

which will be called *surface terminals*. The number of surface terminals is denoted by $N_{s.c.}$. As will be shown in sec. 5.2.3, uniform 3D meshes result in a sparse direct solver run time of roughly $\mathcal{O}(N_{s.c.}^{3.5})$, whereas special non-uniform meshes can achieve $\mathcal{O}(N_{s.c.}^2)$ in practice. Even with these non-uniform meshes, the 3D substrate netlist often by far dominates the sparse direct solver run time because it is considerably larger than the above-lying 2D meshes. In order to improve the efficiency of the 3D substrate netlist, the following approaches are proposed in literature:

Elimination of Internal Nodes Consider the “black-box” representation of the 3D substrate netlist using Y-parameters – i.e. the resistor network obtained by eliminating its internal nodes [168], [185]. Here, a quadratic amount of $N_{s.c.}(N_{s.c.} - 1)/2$ resistors are needed [97], and the run time of a direct solver³¹ is $\mathcal{O}(N_{s.c.}^3)$. Hence, for sufficiently large $N_{s.c.}$, and if these Y-parameters are not sparsified, the elimination of internal nodes will even *worsen* the efficiency. Unfortunately, the Y-parameters of thick 3D conductors cannot be sparsified easily: Some authors [180], [189] propose to simply sparsify the Y-parameter matrix using a cutoff distance. However, as will be shown in sec. 5.2.4, accuracy is only guaranteed if the cutoff-distance is a multiple of the die thickness. Thus, cutoff-distance-based sparsification is only applicable in general if the size of the surface terminals is *not* significantly smaller than the die thickness. Observe that the lack of an efficient and general sparsification procedure is a challenge shared with inductance extraction (see sec. 2.6.1). Worth mentioning is [189], in which the cutoff-distance is optimized in a loop using simulation feedback. In conclusion, the elimination of all internal nodes works best for a small number of surface terminals. Within this thesis, a wafer-substrate model with a small number of surface terminals will be referred to as *low-dimensional* (see also sec. 5.1).

Iterative Linear Solvers Iterative linear solvers (sec. 2.3.1) may perform considerably better on 2D and 3D FEM/FDM-meshes [43], [185]. This will be further detailed in sec. 5.2.3. However, the use of iterative linear solvers for general-purpose circuit simulation is still challenging (see sec. 2.3), and many state-of-the-art circuit simulators do not support it. Conversely, iterative linear solvers are more eligible for substrate noise analysis software: Here, the circuitry is more constrained, e.g. limited to RLCK-networks, and a suitable preconditioner can be found. Also note that, in RLCK-networks, the MNA yields a symmetric positive-definite matrix, which can be solved by the fast conjugate gradient method [26], [35].

³¹ This follows from the well-known property that dense Gaussian elimination is cubic in the matrix dimension.

Accelerated Boundary-Elements Method As an alternative to FEM/FDM, the boundary-elements method (BEM) can be applied to the wafer-substrate. Several methods exist which evaluate the integral operator in BEM in quasi-linear time: Among them are the fast-multipole method [123], and methods based on singular value decomposition [98] or on the fast-Fourier transform [60], [61]. This yields an *implicit representation* of the its Y- or Z-parameters that can be multiplied efficiently. Based on this, circuit simulators can be developed [25], [26] that enable a considerably more efficient “co-simulation” of substrate and circuitry. However, this does not necessarily mean that the linear solver’s asymptotic run time is of a lower order. In fact, the key advantage might rather be that it removes the intricate requirement to create a suitable non-uniform 3D mesh of the interior. Note that these implicit representations are incompatible with sparse direct solvers, and instead iterative linear solvers must be used. Therefore, these methods inherit the drawbacks discussed in the previous paragraph. Beyond that, the need to add yet more problem-specific source code to the circuit simulator can be considered a disadvantage.

Moreover, for the successful application of substrate extraction or substrate noise analysis, it is crucial to find a suitable level of abstraction, and to use an appropriate spatial resolution: This is particularly true because the linear solver run time is usually super-linear, as discussed above. In order to find a suitable level of abstraction, the relevance of the various parasitic element types must be understood. For example, as will be argued in sec. 5.1, the majority of implants, wells and contacts can usually be neglected in EMC-simulations. Further experimental evaluations are found in sec. 6.5.3. The mesh size required in the n-buried layer increases with frequency, as will be shown in sec. 5.1. In the wafer-substrate, the 3D mesh size may only be reduced to a certain degree, at which the curvature of the electric field is still well approximated [185]. Further reductions of the spatial resolution can be achieved using a novel compression technique that will be presented in sec. 5.2.4. However, this implementation cannot be ported to tool flows based on a third-party software. Note that QRC’s substrate extractor supports a feature called “substrate RC-reduction” which might follow a similar aim.

A notable commercial tool for substrate extraction is included in QRC [30]. QRC’s substrate extractor is integrated with the QRC parasitic extractor for the IC metallization, and the extracted netlist can be simulated with any SPICE-like simulator. Despite not explicitly documented, it is presumed that it uses a variant of the 3D-FEM or the 3D-FDM.

Ansyz Totem-CSE is a well-established commercial tool for substrate noise analysis. According to [86], Ansys Totem-CSE creates an RC-circuit from a 3D

FDM mesh. This circuit cannot be exported for use in SPICE-like simulators, but instead Ansys Totem's built-in simulation engine must be used.

2.7 Spectral Measurement of Electromagnetic Interference

To quantify electromagnetic interference (EMI), standards for radiated emissions (e.g. CISPR-25 [29]) and for conducted emissions (e.g. IEC 61967-4) make use of a measuring apparatus called *EMI-Receiver*. This device is standardized in CISPR-16-1-1 [28]. EMI receivers are similar to conventional FFT-based and swept spectrum analyzer instruments [45], [148], [200]. However, there are subtle but important differences in how the spectral amplitudes are quantified by EMI receivers, which will be elaborated in sec. 2.7.1. The final aim of any simulation technique for RF-emissions is to predict the measurement readings of the EMI receiver. Sec. 2.7.2 outlines how this is implemented efficiently and accurately based on AC, RF or transient analysis. Since clock jitter and spread spectrum modulation may strongly affect the EMI receiver readings, these effects must also be accounted for. Sec. 2.7.3 shows how such a phase-modulation of the clock is introduced to the simulation results in a post-processing step.

2.7.1 The EMI-Receiver according to CISPR-16-1-1

Fig. 16 shows a signal flow chart that is representative of the behavior of a typical EMI receiver [28]. Multiple, overlapping band-pass filters, centered at different frequencies, are applied to the input signal. These are activated at the

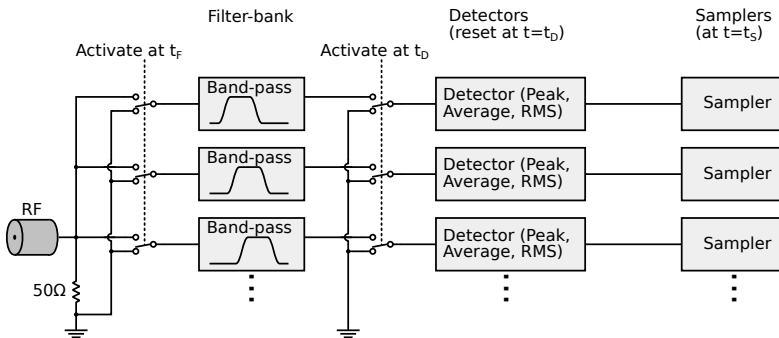


Figure 16: Simplistic filter bank model [45], [200] of an EMI receiver, which applies to FFT-based and fixed-tuned implementations (continuously swept spectrum analyzers are not described by this diagram). This signal flow chart is not representative of an actual implementation, but it is equivalent at the abstraction level used in this section.

time t_F . These filters may be interpreted as an emulation of radio receivers that are disturbed by the incident interference. At a later time $t_D > t_F$, after the detectors were reset, the filtered input signals are applied to the detectors. The following detectors can be selected [28]: The RMS-average-detector outputs the root-mean-square voltage in the time span $[t_D, t]$. Conversely, the peak- and the average-detector yields the maximum and the mean absolute voltage, respectively³². Finally, the detector output is read by the samplers at a single point in time $t_S > t_D$. This results in the following readings:

$$\begin{aligned} \text{PEAK}(g) &:= \frac{1}{\sqrt{2}} \sup_{t \in [t_D, t_S]} |g(t)| & \text{AVG}(g) &:= \frac{\pi}{2\sqrt{2}(t_S - t_D)} \int_{t_D}^{t_S} |g(t)| dt \\ \text{RMS}(g) &:= \sqrt{\frac{1}{t_S - t_D} \int_{t_D}^{t_S} |g(t)|^2 dt} \end{aligned} \quad (20)$$

For pulse sequences with a spacing larger than the filters' time constants, the reading of average- and RMS-average-detectors is indirectly proportional to the spacing [28], whereas for the peak-detector the reading is constant. Thus, the peak detector's reading is independent of the rarity of pulse-like disturbances, which is the main motivation behind the definition of peak measurements. The difference between the peak-detector and average-detector also cannot be neglected for signals with a line-like spectrum: For frequency-modulated signals the difference can be, e.g., 10 dB (see sec. 6.4) or more [142].

Conventional FFT-based spectrum analyzers [45], [200] can be understood in terms of fig. 16 as well, but the detectors might be different and, hence, not completely CISPR-16-1-1-compliant [200]. Moreover, many conventional swept spectrum analyzers are *continuously* swept [148], whereas filters in EMI-receivers are rather fixed-tuned and stepped³³. Another key difference between conventional spectrum analyzers and EMI receivers concerns the spacing and amplitude response of the used filters: In EMI receivers, the filters must have a unit voltage gain at the center frequency, and the filter amplitude response is subject to standards [28], [29]. Moreover, the filters do not necessarily have a strong overlap, and their spacing can be controlled

³² PEAK, AVG and RMS are normalized such that they return the same level for a sine voltage – namely its RMS-amplitude [28]. In addition, CISPR-16-1-1 defines the *quasi-peak detector*. It can be shown that the quasi-peak detector readings are between peak- and RMS-detector readings [200].

³³ CISPR-16-1-1 actually adds a loophole such that continuously swept spectrum analyzers can be used in EMI measurements [28], but this should be discouraged. The R&S ESIB test receiver [153] can be configured in “scan mode” (i.e. fixed-tuned) or “sweep mode” (i.e. continuously swept)

independently of the bandwidth. In contrast, filters of conventional spectrum analyzers typically can be automatically shaped and spaced and normalized [148] in a way that square-integrals over a range of data points from an RMS-detector is equal to the total power in this frequency range. As demonstrated by eq. (38) in sec. 2.7.3, the total power in a frequency range can be also obtained using EMI-receivers if the filter overlap is sufficient and an RMS-average-detector is used, but an additional normalization factor must be applied manually.

The detectors evaluate their input during the time span $[t_D, t_S]$, and this duration is called measurement time $t_M := t_S - t_D$ [28]. If the input signal is periodic, the measurement time must be at least one period, in order to get meaningful and reproducible results. The duration of the time interval $[t_F, t_D]$ shall be called *dead time*. It is clear that in the model from fig. 16, a suitable dead time is required for the filters to settle after the filters are activated at t_F . For example, assume the filters are activated at $t_F = t_D$ then the peak detector would instead observe the step response from the filters' activation at t_F , which is not the intended behavior. In case of finite impulse response (FIR) filters, i.e. when the filter bank is implemented using a short-time Fourier transform [100], a rather short dead time, i.e. equal to the impulse response time, is always sufficient. Conversely, for analog filters, e.g. as in fixed-tuned EMI receivers or emulations thereof, typically the dead time must be much larger than the filter's time constant. The standard CISPR-16-1-1 does not mention a dead time explicitly, and hence this is somewhat implementation dependent.

It must be noted that CISPR-16-1-1 is rather vague about some implementation details of EMI receivers. Strictly speaking, the description above is not valid for very low frequencies, e.g. below 1 kHz [28]:

- The peak detector according to CISPR-16-1-1 may have an implementation-specific finite discharge time, which is not accounted for by eq. (20).
- The RMS-average-detector according to CISPR-16-1-1 must like eq. (20) only for frequencies above a certain corner frequency.

It is sometimes claimed that EMI-receivers don't allow for reproducible precision measurements because CISPR-16-1-1 has rather large tolerance levels [28]. However, this is not true in general:

- CISPR-16-1-1:2015 only demands the EMI-receiver to be accurate up to ± 2 dB. However, modern instruments usually guarantee a better accuracy [154].
- CISPR-16-1-1 merely defines lower and upper bounds for the filter's amplitude response. Some instrument vendors give more detailed information about the actual filter response [154].

2.7.2 Prediction of EMI-Receiver Readings for Periodic Signals

For the sake of simplicity in the following, assume that the input RF waveform $S(t)$ is periodic with the period T . Then, it can be written as a Fourier series [45], [200] as follows:

$$S(t) = \sum_{k=-\infty}^{\infty} c_k \exp(2\pi i f_k t) \quad f_k := \frac{k}{T} \quad (21)$$

where $c_k \in \mathbb{C}$ are called Fourier series coefficients. Its *power spectral density* [200], denoted by $\mathfrak{P}\{S\}$, is related to c_k as follows:

$$\mathfrak{P}\{S\}(f) = \sum_{k=-\infty}^{\infty} |c_k|^2 \delta(f - f_k) \quad (22)$$

where δ is the Dirac delta distribution. In the limit $t_F \rightarrow -\infty$, i.e. for sufficiently long dead time, the application of the filters is equivalent to cyclic convolutions with the filters' impulse responses:

$$S_n(t) := S(t) \star y_n(t) = \sum_{k=-\infty}^{\infty} c_k^{(n)} \exp(2\pi i f_k t) \quad (23)$$

where $\star$ is the convolution operator, $y_n(t)$ is the impulse response of the n -th filter, and the Fourier series coefficients of the filtered signal $c_k^{(n)}$ are:

$$c_k^{(n)} := H_n(f_k) c_k \quad \text{with: } H_n := \mathfrak{F}\{y_n\} \quad (24)$$

where $\mathfrak{F}$ denotes the continuous Fourier transform. Furthermore, assume that the period T is an integer fraction of the measurement time t_M . This can be easily ensured by rounding up the measurement time t_M to the next integer multiple of T . Then, the RMS-average-detector reading from eq. (20) is trivially simplified to the RMS-measure of a single period:

$$\text{RMS}(g) = \sqrt{\frac{1}{T} \int_0^T |g(t)|^2 dt} \quad (25)$$

Similar simplifications apply to the average- and peak-detectors. Using Parseval's theorem [45], eq. (25) applied to S_n from eq. (23) can be expressed in frequency space as follows:

$$\text{RMS}(S_n) = \sqrt{\sum_{k=-\infty}^{\infty} |c_k^{(n)}|^2} \quad (26)$$

Using eqs. (22,24), one can rewrite eq. (26) using an integral measure applied to the power spectral density:

$$\text{RMS}(S_n) = \sqrt{\int_{-\infty}^{\infty} df |H_n(f)|^2 \mathfrak{P}\{S\}(f)} \quad (27)$$

This shows that, for periodic signals, the square of the RMS-average-detector reading is an integral measure on the power spectral density³⁴.

This formulation leads to a simple algorithm for computing the EMI receiver readings given a single period, and assuming ideal periodicity: If the period $S(t)$ is given in time-domain, first, the coefficients c_n are computed using the FFT. In case of the RMS-average-detector, the filter responses can be directly evaluated using eq. (26) and eq. (24). Usually, only few summands have to be included in eq. (26) because $H_n(f_k)$ drops off quickly. For peak- and average-detectors, the coefficients $c_k^{(n)}$ must be converted back to a time-domain representation using the inverse FFT. For reasons of efficiency, it is important to include a minimum number of coefficients $c_k^{(n)}$ around the filter's center frequency in the FFT. These coefficients are frequency-shift to DC. This results in an analytic signal [24], [181], which can be interpreted as a critically sampled I/Q-demodulation [200] of S_n .

However, note that perfect periodicity of S is often a poor approximation: Unintended jitter and phase noise as well as intended spread spectrum modulation of the clock violate this assumption. Therefore, corrections to this procedure are required, which will be discussed in sec. 2.7.3.

A single period of the electromagnetic interference S can be obtained using transient simulation or using RF-analyses like harmonic balance (sec. 2.3.3). Alternatively, multiple waveforms $S_{\text{pre}}^{(1)}, S_{\text{pre}}^{(2)}, \dots$ from a preceding transient- or RF-analysis can be propagated to the measurement point using the XF-analysis and the convolution/superposition theorems (see sec. 6.3.2). It should be stressed that neither S nor $S_{\text{pre}}^{(k)}$ should not be obtained by simply cutting out a part from a transient time trace: While this might be a good approximation for a few low-order harmonics, large errors might be introduced to the higher harmonics. This is because the periodic repetition of a part of a time trace

³⁴ More generally, for stochastic signals the square of the RMS-average-detector reading can be used to estimate the power spectral density. This is related to Welch's method [181], [195].

has artificial discontinuities at $t = kT$, $k \in \mathbb{Z}$ [181], which elevates the high frequency asymptote of the spectrum to $|c_k| \sim \mathcal{O}(f_k^{-1})$.³⁵ These artificial discontinuities can be minimized by running the transient simulation for a very large number of periods, until it rather precisely approximates the periodic steady state (PSS). However, clearly, such a “brute-force” approach may be orders of magnitude slower. Instead, the following solution is preferred in this thesis: Firstly, two subsequent periods A and B are cut from a transient simulation result. Copies of A and B , which are called A' and B' , are created and delayed by one period, such that A' overlaps B . Subsequently, AB is cross-faded with $A'B'$ using a suitable³⁶ smoothstep function $\lambda(t)$ that equals 1 at A and 0 at B' . Then, the superposition of $\lambda(t)B + (1 - \lambda(t))A'$ is extracted. This approach generated excellent results (sec. 6.3.2 and sec. 6.5.1).

Another practical concern is related to the use of high-order spline-interpolation in order to transform the transient onto an equidistantly-spaced time axis for the FFT: The adaptive time step control may rapidly alter the time step, which, for example, leads to temporary decrease in the order of the BDF-polynomial (sec. 2.3.1). If this is ignored in the post-processing, i.e. spline interpolation with a constant spline order is performed, large erroneous overshoots in the interpolated data can occur.

2.7.3 Clock Jitter and Spread Spectrum Modulation

Periodic EMI usually arises from clocked circuits. Random or deterministic variations in the clock source can lead to deviations from the assumption of a perfectly periodic EMI-transient. In this section, firstly, a perfectly-periodic estimate S , which captures only a *single clock period*, is obtained from simulation, as explained in sec. 2.7.2. Henceforth, the period of S will be called T_1 . Subsequently, a disturbed version S' of this signal is constructed as follows:

$$S'(t) = S\left(t + \frac{T_1}{2\pi}\Phi(t)\right) \quad (28)$$

where Φ models the phase noise [200]. By suitable choice of Φ in eq. (28), the non-ideal behavior of the clock source can be approximated:

- **Spread Spectrum Modulation:** A variety of schemes exist that introduce a deterministic variation of the clock period with the intent of reducing the EMI-receiver readings [142]. For example, a simple scheme

³⁵ The use of a window function [181], [195] appears to be a feasible workaround. However, in fact, windows functions may only be applied to a sequence of multiple periods. For a single period, an erroneous clock-phase-dependent weighting would be introduced.

³⁶ It is important that $\lambda(t)$ is of a high differentiability class.

is *frequency hopping spread spectrum* [79], in which the clock frequency is switched periodically. Another common scheme is triangular frequency modulation.

- **Clock Jitter:** In every physical clock source, the clock period and the duty cycle are subject to random fluctuations, e.g. due to flicker noise. Especially phase-locked loops [2], [200] exhibit a considerable clock jitter.

Note that Φ must be of a high differentiability class, in order not to introduce artificial discontinuities, kinks etc. to S' (see also sec. 2.7.2). Therefore, this construction must necessarily slightly compress and stretch S in-between its periodic intervals. This artifact should be mostly negligible if the phase modulation is *weak*.³⁷

In order to determine Φ , the clock source must be characterized. This might be achieved by defining a time-discrete stochastic process, which depends on a few parameters: For example, spread spectrum modulation schemes might be parameterized by the modulation frequency, the frequency deviation, or the hopping intervals. However, for reasons of simplicity, instead, a more general and more empirical approach is proposed: The clock source is simulated³⁸ for a large number of periods. The precise points in time of the rise- and fall-events $\lambda_k, k \in [1, 2, \dots, N]$ are recorded. Then, Φ is fixed at the discrete time points λ_k by demanding that the argument of S in eq. (28) at $t = \lambda_k$ evaluates to $kT_1/2$:

$$\Phi(\lambda_k) = 2\pi \left(\frac{k}{2} - \frac{\lambda_k}{T_1} \right) \quad (29)$$

In-between $t = \lambda_k$, the phase modulation Φ is interpolated using a spline of high order. The so-obtained Φ has a period of $T_2 := \lambda_N$. Discontinuities, kinks etc. in the periodic repetition of $\lambda_k, k \in [1, 2, \dots, N]$ must be avoided in analogy to the smoothstep-cross-fading technique in sec. 2.7.2 Furthermore, all λ_k must be slightly scaled such that $\lambda_N = T_1(N - 1)/2$.

³⁷ A strong phase modulation is present if, for some frequency f , many carriers from eq. (30) overlap. An alternative to eq. (28) would be to model non-ideal behavior of the clock source as convolution of an “EMI pulse” with a randomized Dirac comb. This approach, which appears more complicated, had led to surprisingly similar formulas, but it didn't fit into the margin of this page...

³⁸ Transient *noise* simulations, which account for electrical noise, must be used. Furthermore, it must be ensured that the PLL is locked and has reached the steady state.

The application of the so-obtained Φ to eq. (28) leads to a periodic function S' with period T_2 , which is a large integer multiple of T_1 . Now substitute eq. (28) into eq. (21) and simplify:

$$S'(t) = \sum_{k=-\infty}^{\infty} c_k C_k(t) \quad \text{with } C_k(t) := \exp(2\pi i f_k t) \exp(ik\Phi(t)) \quad (30)$$

This equation can be understood as an expansion of S' in terms of phase-modulated sinusoidal carrier signals C_k . The expansion in eq. (30) is conceptually similar to prior work [142]. However, in the following, a novel formalism is presented, which allows to simplify the computation of the EMI receiver readings considerably, and which is hence more efficient than previous brute-force approaches [100]. The second exponential C_k from eq. (30) can be expanded in terms of another Fourier series with period T_2 :

$$\exp(ik\Phi(t)) = \sum_{m=-\infty}^{\infty} c'_{k,m} \exp(2\pi i f'_m t) \quad f'_m := \frac{m}{T_2} \quad (31)$$

Substituting eq. (31) into eq. (30), and using $f_k + f'_m = f'_{m+k(N-1)/2}$, which follows from the fact that T_2 is an integer multiple of T_1 , yields:

$$S'(t) = \sum_{k,m=-\infty}^{\infty} c_k c'_{k,m} \exp(2\pi i f'_{m+k(N-1)/2} t) \quad (32)$$

$$= \sum_{m=-\infty}^{\infty} c''_m \exp(2\pi i f'_m t) \quad \text{with } c''_m := \sum_{k=-\infty}^{\infty} c_k c'_{k,m-k(N-1)/2} \quad (33)$$

Eq. (33) follows from eq. (32) by re-ordering the sum over m , and it is a Fourier-series expansion of S' with period T_2 .

This allows for the construction of an efficient algorithm for computing the EMI receiver readings in the presence of clock jitter or spread spectrum modulation, given *only a single period* of the EMI transient. First, after having obtained Φ as described above, a suitable number of coefficients $c'_{k,m}$ are pre-computed and tabulated. Similar to sec. 2.7.2, by applying the convolution theorem to $S'_n(t) := S'(t) \star y_n$ and using the rapid drop-off of H_n , the response S'_n is captured by only a small subset of the coefficients c''_m from eq. (33). In analogy to sec. 2.7.2, their $|\cdot|_2$ norm must be computed in case of the RMS-average-detector, or frequency down-conversion and inverse FFT with period T_2 yields an I/Q-demodulation of S'_n , which is suitable for evaluating peak and average detectors.

Let's consider frequency-modulation with a sinusoidal baseband signal:

$$\Phi(t) = \frac{f_{\Delta}}{f_m} \sin(2\pi f_m t) \quad (34)$$

where f_{Δ} is the frequency deviation³⁹ and $f_m := 1/T_2$ is the modulation frequency [200]. It is well known that for Φ from eq. (34), the coefficients $c'_{k,m}$ from eq. (31) have a simple closed-form solution [181]:

$$c'_{k,m} = J_m \left(\frac{k f_{\Delta}}{f_m} \right) \quad (35)$$

where J_m are the Bessel functions of the first kind. This can be interpreted as an idealized spread spectrum modulation scheme. Thereby, and using the algorithm described above, the EMI-receiver readings can be estimated quickly.

Now assume that the modulation introduced by Φ is sufficiently weak, such that the Fourier series representations of phase-modulated carrier signals C_k from eq. (30) are approximately disjoint. Furthermore assume a frequency window function $W_k(f)$ which allows to separate the carriers $C_k + C_{-k}$ from all other carriers⁴⁰. Then it can be shown that the W_k integral measure on the power spectral density of the T_2 -periodic signal S' is related to the Fourier series coefficient c_k of the T_1 -periodic signal S as follows:

$$\begin{aligned} \int_{-\infty}^{\infty} W_k(f) \mathfrak{P}\{S'\}(f) df &\approx \int_{-\infty}^{\infty} W_k(f) \mathfrak{P}\{C_k + C_{-k}\}(f) df \\ &\approx \int_{-\infty}^{\infty} \mathfrak{P}\{C_k + C_{-k}\}(f) df \approx \int_{-\infty}^{\infty} (\mathfrak{P}\{C_k\} + \mathfrak{P}\{C_{-k}\})(f) df = 2|c_k|^2 \end{aligned} \quad (36)$$

Now assume that EMI receiver measurements with an RMS-average-detector $\text{RMS}(S'_n)$ have been performed with a number of sufficiently overlapping filters H_n . Then, suitable frequency windows W_k are given by:

$$W_k(f) = \frac{\Delta f}{G_0 B_N} \sum_{n=n_1(k)}^{n_2(k)} |H_n(f)|^2 \quad \text{with: } B_N := \frac{1}{G_0} \int_{-\infty}^{\infty} |H_n(f)|^2 df \quad (37)$$

³⁹ It might be more concisely termed the frequency deviation of the fundamental frequency. The frequency deviation of the k -th carrier C_k is $k f_{\Delta}$.

⁴⁰ This frequency window W_k must be ≈ 1 in the frequency spans of C_k and C_{-k} and ≈ 0 in the frequency span of all $C_{k'}, k' \neq k, k' \neq -k$. Note that $W_k(f) = W_k(-f)$ and W_k is non-zero for negative frequencies.

where B_N is known as *noise bandwidth* [148], [200], Δf is the difference between adjacent filter center frequencies and $G_0 := |H_n(f_c^{(n)})|^2$ is the filter power gain at the center frequency $f_c^{(n)}$ ⁴¹. Then, by substituting eq. (37) into eq. (36), and using the analogon of eq. (27) for S' and S'_n , one obtains:

$$\frac{\Delta f}{G_0 B_N} \sum_{n=n_1(k)}^{n_2(k)} \text{RMS}(S'_n)^2 \approx 2|c_k|^2 \quad (38)$$

This demonstrates how the Fourier series coefficients' magnitude of the “single period” signal S can be *recovered* from sums over EMI receiver readings of the RMS-average-detector if the filters' amplitude responses have a sufficient overlap and if the carriers C_k are sufficiently separated in frequency space.

⁴¹ Here, B_N , Δf and G_0 are assumed to be independent of n . As remarked in sec. 2.7.1, in CISPR-16-1-1 compliant measurements, $|H_n(f_c^{(n)})|$ and G_0 must equal 1.

CHAPTER 3

Physically-based IC-Package Models for EMC Predictions

3.1 Introduction

This section is concerned with electrical IC-package models for EMC-simulations. Today's automotive system ICs are packaged in dual- or quad-row surface mount packages. In these IC-packages, the die is glued and bonded to a lead-frame, and the package is usually sealed by plastic-molding.

There are multiple established approaches for the electrical modeling of IC-packages: Firstly, electromagnetic field simulation can be used (sec. 2.5.1). Here, ports are placed between the IC-pins and the ground plane, as well as between the bond pads and some IC-local reference conductor [201]. The resulting S-parameter dataset is included into transient simulations via reduced-order macromodeling (sec. 2.4.2). Secondly, parasitic-extraction techniques based on electro- and magnetostatic field solvers can be used (sec. 2.5.2). In this approach, the ground plane is often not included. Third, in some cases it is sufficient to use simplistic estimates for package inductances and capacitances. This approach only accounts for a small selected subset of inductive couplings.

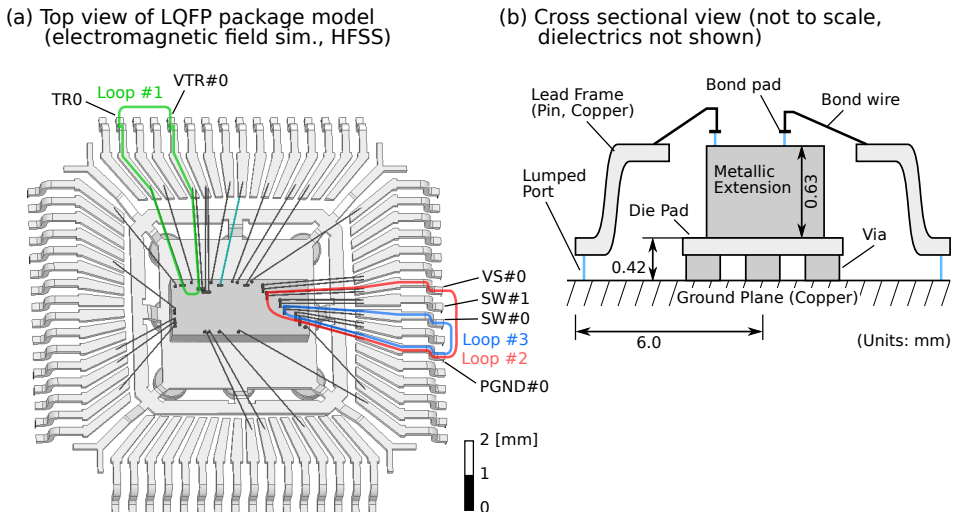


Figure 17: 3D CAD-drawing of an IC-package (LQFP-64, plastic molded, with exposed pad). It is used in electromagnetic field simulations based on lumped ports akin to fig. 12.

These approaches satisfy the requirements of functional verification use cases. However, they are often inappropriate for EMC-simulations because EMC-simulations pose far more stringent demands on the IC-package model. This will be elaborated in the following.

Fig. 17 (a) shows a 3D CAD-drawing of the IC-package used in the developed test-IC (chapter 6). Three pin-loops are highlighted in color: Loop #2 (red) and #3 (blue) conduct switching currents of a DC/DC-converter module, and loop #1 (green) spans the output pin of a transceiver module and its power supply (see sec. 2.1). Electromagnetic field simulation predicts a mutual inductance between loop #2 (red) and loop #1 (green) of $|L_{12;34}| = 5.4 \text{ pH}$ (sec. 3.2.3, table 2). Observe that this mutual pin-loop inductance is roughly three orders of magnitude below the typical pin-inductance (e.g. $L_{34;34}$ from table 2). Therefore, it can be neglected in functional verification. In contrast, in EMC-simulations, a high accuracy is required for small long-range mutual inductances because, e.g., $|L_{12;34}| = 5.4 \text{ pH}$ can already cause violations of the EMC requirements: The following calculation approximates the current spikes drawn from the DC/DC power supply as a Dirac comb (sec. 6.3.2, eq. (100)). Furthermore, it presumes that this AC-current flows mainly across loop #2 (red), and induces an AC-voltage across loop #1, onto which the 150-Ohm network acts as an ideal resistive voltage divider (sec. 6.7, eq. (104)). This yields the following expression¹ for the EMI-receiver readings:

$$V_{\text{RMS}}(f) = 2\pi f \sqrt{2} \frac{25}{145} Q_{\text{DC/DC, rise-pulse}} f_{\text{DC/DC}} L_{12;34} \quad (39)$$

where $f_{\text{DC/DC}} = 3 \text{ MHz}$ is the frequency of the DC/DC-converter, and where $Q_{\text{DC/DC, rise-pulse}} = 8.7 \text{ nC}$ is the area under the current spike at the rising clock edge (table 12). Eq. (39) yields $V_{\text{RMS}} = 21.6 \text{ uV}$ at $f = 100 \text{ MHz}$. This already violates the RF-emission limits (150 Ohm method) for LIN-transceivers, which is either 10 uV or 20 uV at 100 MHz, depending on the external circuitry [10]².

Moreover, observe that there is a large number of small long-range mutual pin-inductances. Since it is often difficult to rate their relevance for the EMC a-priori, they must be all included with high accuracy.

¹ Clearly this is a very simplistic calculation: For example, the neglect of the charge spike shape is only accurate between roughly 12 MHz and 60 MHz (sec. 6.3.2). Moreover, in practice, substrate-couplings cause RF-emissions of even higher magnitude at 100 MHz (Tr. #0 ON, sec. 6.5.1). The simplification of the integrated circuitry and the neglect of clock jitter further limit the generality of this formula.

² Specifically, if external capacitors of up to $3 \times 68 \text{ pF}$ are present at the bus line, the limit is 10 uV. If no additional capacitors are present, the limit is 20 uV [10].

The mutual pin-loop inductance $L_{12;34}$ can be approximated by regarding the loops #2 and #1 as two ideal magnetic dipoles that are oriented in z -direction and separated by a distance of d_{xy} . The presence of a perfectly conducting and infinite ground plane at $z = -d_z$ is accounted for by the method of images:

$$L_{12;34} = \frac{\mu_0 A_1 A_2}{4\pi(d_{xy}^2 + 4d_z^2)^{3/2}} \left(\left(1 + 4\frac{d_z^2}{d_{xy}^2} \right)^{3/2} - 1 + \frac{12}{d_{xy}^2/d_z^2 + 4} \right) \quad (40)$$

where A_1 and A_2 are the loop areas of the dipoles. The details of the derivation are left as an exercise to the reader. Using $A_1 = 5.7 \text{ mm}^2$, $A_2 = 7.7 \text{ mm}^2$, $d_{xy} = 7.3 \text{ mm}$ and $d_z = 1.1 \text{ mm}$, values which are taken from fig. 17³, one obtains $L_{12;34} = 3.6 \text{ pH}$. This estimate deviates from electromagnetic field simulation by only 44%. However, if the ground plane is neglected, e.g. as in some magnetostatic field simulations, the following loop inductance is computed:

$$L'_{12;34} := \lim_{d_z \rightarrow \infty} L_{12;34} = \frac{\mu_0 A_1 A_2}{4\pi d_{xy}^3} \quad (41)$$

This formula evaluates to $L'_{12;34} = 11.3 \text{ pH}$, which is by a factor of roughly 3 larger than $L_{12;34}$ from eq. (40). In a more precise computation, an even larger quotient of $L'_{12;34}/L_{12;34} = 8.6$ was found (sec. 3.3.4)⁴. This shows that the ground plane significantly shields long-range mutual inductances, which *must be accounted for* in package-models for EMC-simulations.

In many ICs, the package features an exposed pad, the main function of which is heat removal (sec. 2.2). However, AC-currents leave the IC through the die-backside and the exposed pad, which may not be neglected in EMC-simulations. This will be demonstrated experimentally in sec. 6.5.2. Therefore, the IC-package model must also pose a realistic impedance to a non-zero total current that enters the IC-pins and leaves via the exposed pad.

³ d_{xy} was calculated as the distance between the loop areas' center-of-mass.

⁴ Eqs. (40, 41) might underestimate the impact of neglecting the ground plane because they assume closed current paths. This is not the case in parasitic extraction without ground plane.

3.2 Black-Box Models based on Electromagnetic Field Simulation

This section analyzes the realization of the IC-package model as a black-box S-parameter dataset, as mentioned in sec. 3.1. The S-parameter dataset is obtained using electromagnetic field simulations based on lumped ports. As shown in fig. 17 (b), the IC-local reference conductor, which is called *metallic extension*, is galvanically connected to the die-pad. The necessity of this construction will be elaborated, and alternatives will be discussed. To enable transient simulations, reduced-order macromodels (sec. 2.4.2) were constructed using the IDEM-software [31]. This caused errors in the long-range mutual pin-loop inductances, which are analyzed in detail.

3.2.1 Methods

The 3D electromagnetic field simulation was performed using HFSS and includes the PCB ground plane, the entire lead frame, and most bond-pads and -wires. The bond wires electrically connect the bond pads to the lead-frame. Moreover, the simulation includes the PCB's FR-4 layer and the package mold compound, which are dielectrics. The silicon die, the die-attach glue, and dielectric and metallic layers of the IC-metallization are *omitted*. As shown in fig. 17 (b), for each IC-pin, a lumped port that refers to the PCB ground plane was introduced. Moreover, for each bond-pad, a lumped port, which refers to the so-called *metallic extension*, is added. This metallic extension is an IC-local reference conductor and an artificial object, the shape of which roughly coincides with the geometry of the silicon die. It is electrically connected to the die-pad. This construction differs from conventional IC-package models, which instead electrically separate the IC-local reference conductor from the die-pad. As will be shown, the proposed construction allows to account for die-backside currents in a simple manner, while the accuracy of small mutual inductances is still excellent. Note that, alternatively, one might remove the metallic extension entirely, and instead directly use the die-pad as reference conductor. However, this would result in lengthy lumped ports, which might adversely affect the model's passivity and causality as well as the accuracy of small mutual inductances. The IC-package and ground-plane were placed in a considerably larger vacuum box.

The obtained S-parameters were imported into IDEM [31]. The data successfully passed checks for passivity and causality, and no visible artifacts were seen in a review of the curves. Then, the vector fitting was performed in the complete frequency range from 1 MHz to 1 GHz. It was attempted to fit the parameters in S- and Y-parameter form, as well as in a certain H-parameter

representation that will be defined in sec. 3.2.2. A minimum order of 2, an order increment of 2 and a maximum order of 200 was used. The initial target accuracy was 0.001 and the initial guaranteed accuracy was 0.1, which are IDEM's default settings. A sequence of fits was performed, in which the target accuracy and the guaranteed accuracy were simultaneously decreased in steps of one order of magnitude. Two different reduced-order macromodels were exported for each fit: The first one is the unmodified vector fit, whereas in the second one, in addition, passivity enforcement was applied.

3.2.2 H-Parameters and (Mutual) Ground-Return Inductances

In the following, a certain hybrid-parameter representation (see sec. 2.4.1) of the package model is introduced. This is illustrated in fig. 18: Here, all lumped ports between IC-pins and the PCB-ground plane described as Z-ports, whereas all lumped ports between bond pads and the metallic extension are described as Y-ports. To distinguish them from the terminal-based H-parameters in parasitic extraction (sec. 2.5.2), they will be called *port-based H-parameters*. They exhibit the following block structure:

$$H = \left(\begin{array}{c|c} H_{ee} & H_{ei} \\ \hline H_{ie} & H_{ii} \end{array} \right) = \left(\begin{array}{c|c} i\omega L + R & - \\ \hline - & i\omega C + G \end{array} \right) \quad (42)$$

where the Z-block H_{ee} is decomposed into the ground-return inductance matrix L and the resistance matrix R . Moreover, the Y-block H_{ii} is decomposed into the pin-capacitance matrix C and the pin shunt-conductance matrix G .

The components of L , which are called (*mutual*) *ground-return inductances* $L_{m,n}$, can be alternatively defined using the test-circuit in fig. 19 (a): Hence,

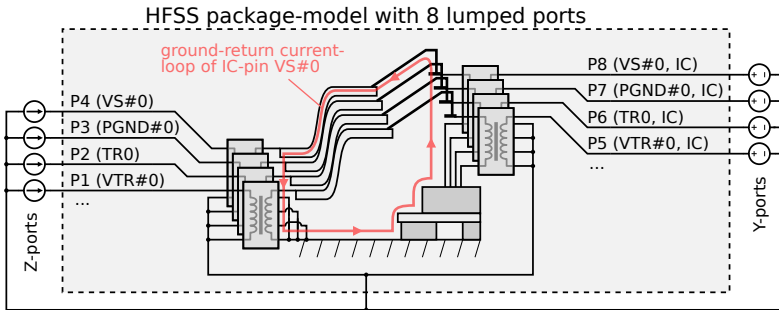


Figure 18: Port-based H-parameters obtained by converting the raw HFSS S-parameters. For clarity, only four IC-pins are depicted. The ports P1–P4 correspond to IC-pins and the ports P5–P8 correspond to bond-pads. The ideal transformers depict the semantics of the lumped ports, akin to fig. 12.

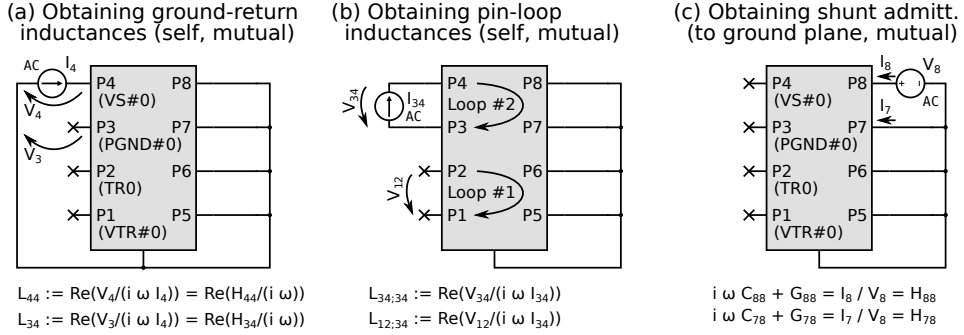


Figure 19: The test circuits used to obtain (mutual) ground-return inductances, (mutual) pin-loop inductances and the pin shunt-admittance. They are applied to the raw HFSS S-parameters as well as to the reduced-order macromodels. The package model port numbers P1-P8 are consistent with fig. 18.

$L_{m,n}$ are (mutual) loop inductances of the closed current paths illustrated by the orange line in fig. 18:⁵ This current flows across the pin's bond-wire and lead-frame parts, and is returned through the exposed pad and the PCB ground plane. Hence, it is trivial that IC-package models based on the metallic extension do support currents through the exposed pad, as required in sec. 3.1.

The main figure of merit used to evaluate the reduced-order macromodels vs. the raw HFSS-output are the (mutual) pin-loop inductances $L_{m,n;k,l}$. The (mutual) pin-loop inductances are defined as illustrated by fig. 19 (b). This test circuit measures the mutual inductances between loop #1 and loop #2 in fig. 17 (a), which is also called $L_{12;34}$. Alternatively the (mutual) pin-loop inductances can also be computed directly from the ground-return inductance matrix:

$$L_{m,n;k,l} = L_{n,k} - L_{n,l} - L_{m,k} + L_{m,l} \quad (43)$$

This follows by applying eq. (42) and the definition of H-parameters eq. (11) to fig. 19 (b).

The definition of the pin shunt-admittance, i.e. the components of $H_{ii} = i\omega C + G$, is also illustrated in fig. 19 (c). For example, using this kind of test-circuit, C_{66} , which is the sum over all capacitances at pin TR0, can be obtained. In the limit $\lim_{\omega \rightarrow 0} |i\omega C + G|$ should approach zero – violations thereof will be called *leakage artifacts*.

⁵ Note that, for frequencies approaching the pin self-resonances, this interpretation would be incorrect. Thus, only as long as the IC-package can be considered electrically small, the denotation of $L_{m,n}$ as (mutual) ground-return inductances is reasonable.

The port-based H-parameters defined above can be thought of as a canonical representation of IC-package models. In contrast to Y- and Z-parameters, the limit $f \rightarrow 0$ is full-rank (see sec. 2.4.2), and $\lim_{f \rightarrow 0} H$ separates the information about L and C into different components. Sec. 3.3.3 will show how this can be exploited to construct simple lumped-elements equivalent circuits. Moreover, in contrast to S-parameters, this representation does *not* introduce cancellation errors to (mutual) ground-return inductances $L_{m,n}$ at low frequencies (sec. 2.4.2). This explains why, in this section, it is also attempted to build reduced-order macromodels directly in this H-parameter representation. Recall that fitting $H_{ij}(f)$ to rational functions necessarily introduces fitting errors (sec. 2.4.2): A worst-case relativ error of $\pm\epsilon$, e.g. $\epsilon = 1\%$, will be assumed. Another neat property of vector fitting in this H-parameter-representation is that a simple tight upper bound for the relative error of $L_{m,n;k,l}$ can be given, which will be called ϵ' :

$$\epsilon' = \epsilon \frac{|L_{n,k}| + |L_{n,l}| + |L_{m,k}| + |L_{m,l}|}{|L_{n,k} - L_{n,l} - L_{m,k} + L_{m,l}|} \quad (44)$$

This follows trivially from eq. (43). If the mutual pin-loop inductance $L_{m,n;k,l}$ is much smaller than the absolute sum of the mutual ground-return inductances $L_{n,k}$, $L_{n,l}$, $L_{m,k}$ and $L_{m,l}$, then ϵ' is much larger than ϵ . Hence, reduced-order macromodeling may cause subtractive cancellation in the mutual pin-loop inductances⁶.

3.2.3 Results and Discussion

Table 2 shows exemplary quantities that were extracted from the raw HFSS S-parameters using the test circuits in fig. 19 at 10 MHz. The plausibility of $L_{12;34}$ in table 2 was already demonstrated in sec. 3.1 using eq. (40). The values for L_{14} , L_{13} , L_{24} , L_{23} and $L_{12;34}$ in table 2 can be used to test eq. (43). Eq. (44) yields a ratio of $\epsilon'/\epsilon \approx 14$ for $L_{12;34}$. This exemplifies the inherent susceptibility of mutual pin-loop inductances to subtractive cancellation in reduced-order macromodels quantitatively.

Table 3 lists the reduced-order macromodels that were generated using IDEM. The mutual inductance between loops #1 and #2, i.e. $L_{12;34}$, is very small yet critical for the EMC (see sec. 3.1) – hence, it represents a worst case scenario. In the following, it is demanded that the error in this mutual inductance is

⁶ Despite demonstrated on the example of port-based H-parameters, this problem is not limited to function-fitting in this particular representation. Rather, it is related to reduced-order macromodeling as such, and S-, Y- and Z-parameter-fits suffer from this effect as well.

Description	Symbol	Value
Mutual ground-return inductance (TR0, VS#0) *	L_{24}	19.6 pH
Mutual ground-return inductance (TR0, PGND#0) *	L_{23}	11.2 pH
Mutual ground-return inductance (VTR#0, VS#0) *	L_{14}	29.5 pH
Mutual ground-return inductance (VTR#0, PGND#0) *	L_{13}	15.7 pH
Mutual pin-loop inductance (VTR#0, TR0) ↔ (PGND#0, VS#0) †	$L_{12;34}$	−5.4 pH
Pin-loop inductance (PGND#0, VS#0) †	$L_{34;34}$	5.7 nH
Total pin-capacitance at TR0 **	C_{66}	0.58 pF
All quantities were obtained from the raw HFSS output at 10 MHz using the following test circuits: *: fig. 19 (a) †: fig. 19 (b) **: fig. 19 (c)		

Table 2: Selected (mutual) inductances and capacitances extracted from the HFSS-result.

Names *	Param.	Target Acc.	Guaranteed Acc.	Passivity Enforcement
H1	Hybrid	10^{-3}	10^{-1}	No (failed)
H2	Hybrid	10^{-4}	10^{-2}	No (failed)
H3	Hybrid	10^{-5}	10^{-3}	No (failed)
H4	Hybrid	10^{-6}	10^{-4}	No (failed)
S1, SIP	S	10^{-3}	10^{-1}	Yes (successful)
S2, S2P †	S	10^{-4}	10^{-2}	Yes (already passive)
S3, S3P †	S	10^{-5}	10^{-3}	Yes (successful)
S4, S4P	S	10^{-6}	10^{-4}	Yes (successful)
Y1, Y1P	Y	10^{-3}	10^{-1}	Yes (successful)
Y2, Y2P	Y	10^{-4}	10^{-2}	Yes (successful)
Y3, Y3P	Y	10^{-5}	10^{-3}	Yes (successful)
Y4, Y4P	Y	10^{-6}	10^{-4}	Yes (successful)
*: Names of passivity enforced macromodels are suffixed with a “P” †: The accuracy of $L_{12;34}$ was sufficient after passivity-enforcement and the leakage-artifacts were tolerable.				

Table 3: Attempts to obtain a passivity-enforced reduced-order macromodel using IDEM.

below $\pm 30\%$. In all H- and Y-parameter-fits, both before and after passivity enforcement, this mutual inductance is within the $\pm 30\%$ tolerance region. This can be seen in fig. 20 (a) and (c) on the example of the reduced-order

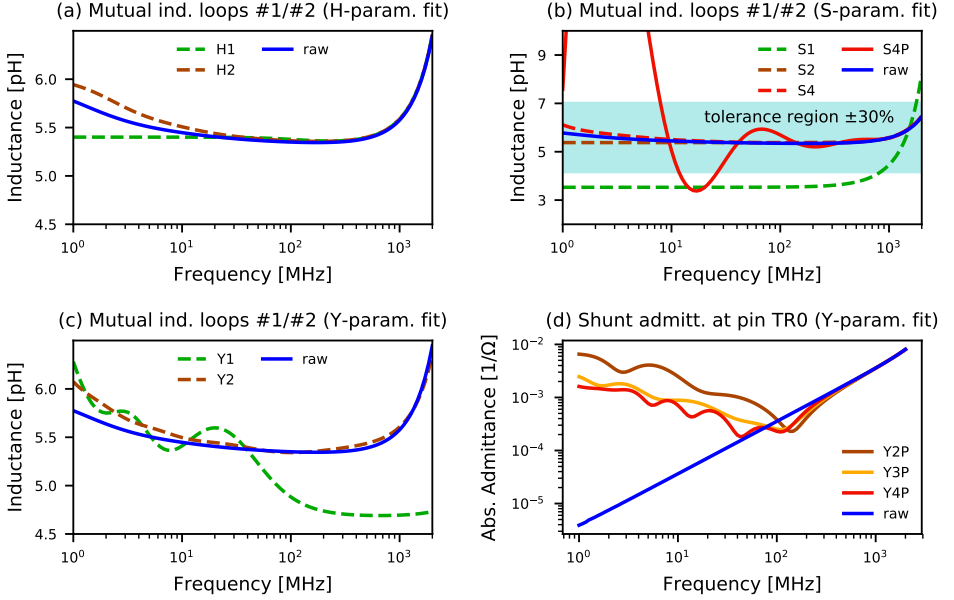


Figure 20: (a–c): Mutual inductance between loop #1 and loop #2 in the reduced-order macromodels, in comparison to the raw HFSS output. Reduced-order macromodels suffixed with a “P” are passivity-enforced. (d): Absolute total shunt-admittance $|i\omega C_{66} + G_{66}|$ in the passivity-enforced reduced-order macromodels based on Y-parameter-fits.

macromodels H1–2 and Y1–2 (table 3)⁷. In contrast, not all S-parameter-fits satisfy the $\pm 30\%$ error-bound on $L_{12;34}$ (blue shaded region in fig. 20 (b)): As shown in fig. 20 (b), even the initial fit with a target accuracy of 10^{-3} before passivity-enforcement, i.e. the reduced-order macromodel S1, is not sufficiently accurate. When the target- and guaranteed-accuracy settings are increased far beyond IDEM’s default (e.g. S2, S4 in fig. 20 (b)), the demands on accuracy could be met. However, this does not generally apply if passivity is enforced: For example, S4P (i.e. passivity-enforcement applied to S4) strongly violates the $5.4 \text{ pH} \pm 30\%$ tolerance region for frequencies below 30 MHz. This illustrates that the perturbations from passivity enforcement can lead to a catastrophic increase of the relative error of mutual pin-loop inductances like $L_{12;34}$: Firstly, passivity enforcement can apparently significantly worsen the relative error of a fit ϵ . Subsequently, ϵ is amplified by various subtractive cancellation effects, as discussed in sec. 3.2.2. This particular overshoot artifact is specific to high-order rational function fits of S-parameters: In the passivity-

⁷ The reduced-order macromodels H3, H4, Y3, Y4 as well as their passivity-enforced counterparts are not shown for clarity.

enforced moderate-order fits S2P and S3P (not shown for clarity) the artifacts were less pronounced, and the $\pm 30\%$ criterion for $L_{12;34}$ was met.

The reduced-order macromodels have also been tested for leakage artifacts, by examining the total shunt-admittance at pin TR0. All H- and S-parameter fits, both before and after passivity enforcement, have successfully passed this test. In contrast, all passivity-enforced Y-parameter-fits suffer from severe leakage artifacts: This is shown in fig. 20 (d): At 1 MHz, the total shunt-admittance at TR0 was at least $(1 \text{ k}\Omega)^{-1}$ for Y2P, Y3P and Y4P. This is explained by the discussion of the SMD-capacitor model in sec. 2.4.2. Interestingly, if passivity-enforcement was disabled, the leakage artifacts disappeared in some Y-parameter-fits. Thus, also in Y-parameters, the intrinsic numerical instabilities can remain hidden until triggered by passivity enforcement.

As shown in table 3, the passivity-enforcement implementation of IDEM failed for the port-based H-parameters. It is conjectured that the Hamiltonian passivity-enforcement algorithm, as implemented in [64], is not well-suited for broadband H-parameter-fits of electrically-small systems. This currently precludes the direct application of vector fitting to the port-based H-parameters.

3.2.4 Conclusion

Out of 12 passivity-enforced reduced-order macromodels, only two were suitable for EMC-simulations. This is shown by the †-symbol in table 3. Y-parameter-fitting may never be used for IC-package models, due to severe leakage-artifacts. The results of S-parameter-based vector fitting were only useful if the rational function order was within a certain bounded range. Thus, manual fine-tuning and extensive verifications of the fits are required. Recall that there is a large number of mutual pin-loop inductances, and it is difficult to decide a-priori which are most relevant for the EMC-simulations under consideration. Therefore, even after the extensive verifications of a reduced-order macromodel, some uncertainty about its quality remains.

The port-based H-parameter representation appears attractive because they avoid error amplification due to subtractive cancellation in the mutual ground-return inductances at low frequencies. Thus, it is conjectured that, in this case, the rational function order would not be limited from above, as it is de-facto in the S-parameter representation. However, in this representation, the state-of-the-art implementation of IDEM fails to enforce the passivity. This calls for further investigations and improvements in the Hamiltonian passivity-enforcement algorithm [64]. Also note that S-parameter-based macromodels are not very amenable to insightful alteration analyses (sec. 2.3.3) and root-cause studies (see sec. 6.7). This is different in H-parameter-based macromodels because its individual components have an intuitive interpretation in

terms of inductances and capacitances at low frequencies. In principle, in an alteration analysis, blocks circuit elements in the synthesized reduced-order macromodel that represent a component might be selectively disabled.

In addition to the difficulties discussed in this section, reduced-order macromodels may also cause other inaccuracies and instabilities in transient simulations (sec. 2.4.2 and 2.3.2). Due to the numerous non-trivial issues that arise from reduced-order macromodels in EMC-simulations, there is a strong motivation to find alternatives. Sec. 3.3 will demonstrate two feasible approaches that instead generate lumped-elements equivalent circuits.

3.2.5 Alternatives to the Metallic Extension on the Die-Pad

Above, the artificial “metallic extension” has been introduced, in order to obtain a reference conductor – in this case the die-pad – which is sufficiently close to the bond pads. As anticipated in sec. 3.2.1, an alternative is to introduce a IC-local *floating* reference conductor, e.g. thin and good conductor, roughly in the plane of the die’s top surface. The lumped ports of the bond-pads are then referred to this floating reference instead.

However, a naive implementation of this construction gives incorrect results when combined with a substrate model. Such a substrate model must model the die-backside as well, either as a short to the die-pad, or as a distributed backside capacitance to the die-pad (see sec. 6.3.1). By convention, the die-pad is represented by the simulator ground. Therefore, the voltage difference between bond-pads and the simulator ground in the SPICE simulation must reflect the voltage difference between bond-pads and the die-pad in the field simulation. However, since the lumped ports of the bond pads are now referred to the floating reference, the voltage difference between bond-pads and the simulator ground in the SPICE simulation is incorrect. Moreover, a non-zero total current entering via IC-pins would result in a charging of a non-physical capacitor between the floating reference and the die pad. Charging of this small non-physical capacitor, which will be called “CX”, rapidly elevates the voltage of the floating reference, and thereby effectively blocks currents through the die backside.

Fig. 21 shows how a floating reference is correctly realized. Firstly, a lumped port “F” between the die pad and the floating reference must be introduced. Field-simulation yields the S-parameter model shown by the gray box in fig. 21 (b). Then a transformation is applied which changes the reference of all bond-pads, e.g. of port P5, from the floating reference to the die pad. This can be understood as externally attaching transformers as shown in fig. 21 (b). The resulting network is equivalent to the electromagnetic model depicted by the gray box in fig. 21 (c). In the H-parameter representation (Y- and Z-ports in

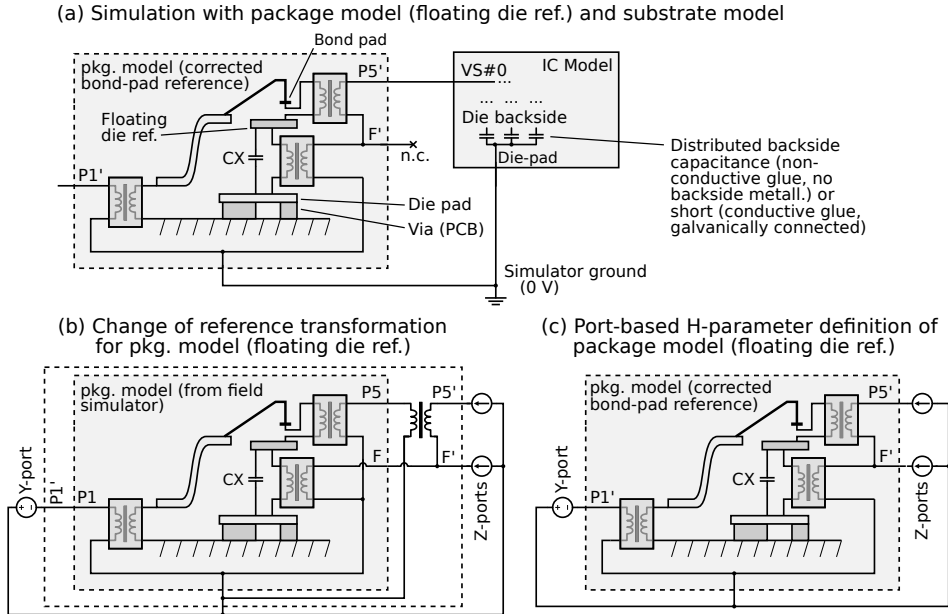


Figure 21: The raw network parameter data from an electromagnetic field solver corresponds to the gray box in (b). By externally adding certain transformers, and characterizing the network parameters, one obtains the gray box in (c). This is connected to an IC-model including the substrate as shown in (a).

fig. 21 (b) and (c)), this is simply achieved by superimposing two rows and two columns. After having corrected the reference of the bond-pad's lumped ports, the network from fig. 21 (c) can be connected to an IC-model including the substrate. This is shown in fig. 21 (a). It can be seen that the voltage difference between the two terminals of the IC-model (VS#0 and the die-pad) now reflects the voltage difference between the die-pad and the bond-pad in the field simulation. Furthermore, now, a current drawn across the IC-model, i.e. entering VS#0 and leaving the die pad, results in a current path across the bond-pad's lumped port as well as over the floating reference's lumped port. Therefore, no current flows across the non-physical capacitor "CX", and it is not charged.

Note that the terminal F' is left unconnected in fig. 21 (a). This is best realized by applying an additional transformation to the package model's network parameters: In the H-parameter representation, this merely amounts to the removal of a row and of a column from the matrix⁸. Observe that the semantics of the so-obtained port-based H-parameters is the same as in the previously-described metallic extension: That is, the imaginary part of the Z-

⁸ Note that this finally eliminates the non-physical capacitor "CX" from the dataset.

block equals the ground-return inductance matrix (eq. (42)). If the generation of a reduced-order macromodel is required, vector fitting should be applied to the S-parameters of the network that is transformed as described, rather than to the initial S-parameters⁹: Since the semantics of the network parameters are equivalent, the conclusions about the metallic-extension approach (sec. 3.2.4) are completely transferable to the floating reference approach.

One might naively try to introduce multiple ports between the floating reference and the die-pad, in order to distribute the die backside current more evenly. However, in the course of this thesis it was empirically found that connecting these ports in parallel ruins small long-range mutual pin-loop inductances like $L_{12,34}$. Therefore, this must not be done in EMC-simulations. This effect and the other considerations above emphasize how *extremely subtle* is the task of creating and combining physical IC-package models and substrate models for the purpose of EMC-simulations.

Note that in the LQFP-64 package in fig. 17, the height of the metallic extension is very small compared to the diameter of the IC-package, and thus negligible. The floating reference construction might be useful for ceramic IC-packages with a non-conductive die pad because here a comparatively thick metallic extension, which spans the distance between the die's top surface and the PCB-plane, would have to be introduced. This approach was successfully tested on a ceramic IC-package (sec. 6.5.5). However, for simplicity, the metallic extension should be preferred over the floating reference.

3.3 Lumped-Element Models Containing Ground-Return Inductances

This section presents two related methods for synthesizing lumped-element models of packages that are sufficiently accurate for EMC-simulations. This is an alternative to reduced-order macromodels, which allows for a more compact representation and is less prone to numerical issues. Furthermore, the parasitic inductors and inductive couplings in these lumped-element models have a useful physical interpretation as (mutual) ground-return inductances (see sec. 3.2.2). This allows for insightful alteration analyses (sec. 2.3.3) and root-cause studies (see sec. 6.7).

The first method employs parasitic extraction techniques (sec. 2.5.2) to obtain the lumped-element parameters. In the conventional approach using

⁹ The question must be raised, whether this might fail because passivity and causality of such a transformed dataset cannot be ensured. This is not the case: The transformer is causal and passive, and connections between causal and passive networks are necessarily causal and passive as well.

parasitic extraction, the ground plane either neglected (sec. 3.1) or simply introduced as a floating conductor. However, as will be shown, this conventional approach overestimates the mutual pin-loop inductance $L_{12;34}$ at least by a factor of 4.7. It will be shown that this can be fixed by adding terminals to the ground plane and then applying a certain reference transform of H-parameters (sec. 3.3.3). The second method converts electromagnetic field simulation data to the port-based H-parameter representation, as explained in sec. 3.2.2. Using this dataset, a similar lumped-elements model of the IC-package can be constructed as well.

However, the methods in this section are limited to electrically small IC-package models: Since the LQFP-64 package has a diagonal of about 17 mm (see fig. 17), its lumped-element model should not be used beyond 1 GHz (see sec. 2.5.2).

3.3.1 Ground Planes in Parasitic Extraction

Parasitic extraction tools (sec. 2.5.2) do not require a reference conductor, whereas a ground plane is strictly required by electromagnetic field simulation based on lumped ports. In sec. 3.1, it was already motivated that omitting the ground plane entirely causes large errors in long-range mutual inductances because magnetic shielding is neglected. However, less obvious is the fact that magnetic shielding is *also* strongly underestimated if the ground plane is added to the 3D package model as a floating conductor. Before this issue will be explained and resolved, some theoretical background about ground planes in parasitic extraction must be given.

As explained in sec. 2.5.1, field simulation of Maxwell's equation is based on port excitations, whereas parasitic extraction is based on terminal excitations that violate the continuity equation. The (mutual) inductances yielded by electromagnetic field simulation are summarized by the *ground-return inductance matrix* L (sec. 3.2.2), whereas parasitic extraction computes the *partial inductance matrix* $L^{(P)}$ (sec. 2.5.2). In the following, the relation between the (mutual) partial inductances $L_{ij}^{(P)}$ and the (mutual) ground-return inductances L_{ij} is studied on the example of two coupled transmission lines over a ground plane (fig. 22 (a)). These transmission lines have a height over the PCB ground plane of 0.56 mm, and are spaced 3 mm apart – this is comparable to bond-wires in LQFP-packages.

The AC currents on the surface of the ground plane in fig. 22 (b) arise when a current of I_1 is forced across port #1 and a current of $I_3 = -I_1$ is forced across port #3. Conversely, the ground plane currents in fig. 22 (c) are the eddy currents resulting from a current across transmission line #1 that is produced by creating charge carriers at terminal #1 and destroying them at terminal #2.

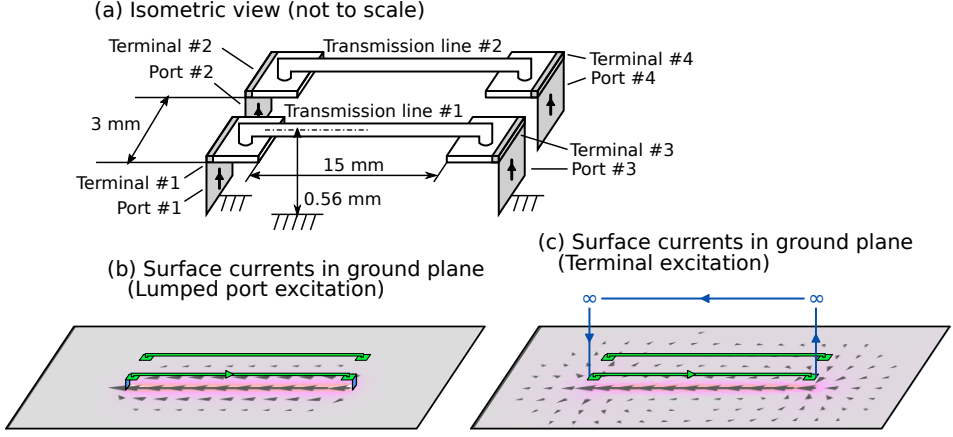


Figure 22: Two transmission lines over a large, highly conductive ground plane. Part (a) shows the definitions of the geometry, terminals and ports, and (b), (c) show solutions of the AC ground plane currents at 100 MHz with either terminal excitations or lumped port excitations. For their computation in (b) a simulation of Maxwell's equation (Ansys HFSS [82]) was used, and in (c) a quasi-magnetostatic solver (Ansys Q3D [84]) was used.

Alternatively, this could be intuitively understood as a current path closed at infinity [15], [92] as depicted in fig. 22 (c) by the blue line. It can be seen that the eddy currents in fig. 22 (c) are less localized than the return currents in fig. 22 (b). This illustrates that the mutual partial inductance between the two transmission lines can be much larger than the mutual ground-return inductance. In this example, they differ roughly by a factor of 19, as will be shown in sec. 3.3.2. Moreover, observe that the (mutual) partial inductances do *not* contain enough information to compute the (mutual) ground-return inductances if the terminals are defined as shown in fig. 22 (a): Since the quasi-magnetostatic solver never inject charge carriers into the ground plane, any superposition of the current fields in the ground plane divergence-free. This is opposed to the current-field in electromagnetic field solvers, in which current is drawn from the ground plane at the port excitations.

This deficit can be resolved by defining additional terminals on the surface of the ground plane as shown in fig. 23 (a). Note that, disregarding numerical and discretization errors, due to linearity of the PDEs, the parasitic extraction model allows to exactly compute the system's quasi-static response to an arbitrary current excitations vector. Therefore, the terminal voltages in fig. 23 (b) corresponds to the electric potential ϕ induced by currents I_1 and $-I_1$ forced across port #1 and port #3. Since differences of ϕ correspond to port voltages (sec. 2.5.2), one can equate V_1 and V_2 with voltages of port #1 and port #2 from fig. 22 (a). Hence, the (mutual) ground-return inductances

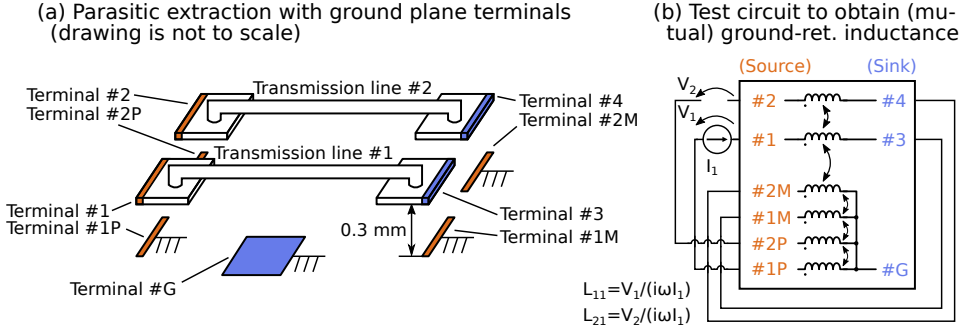


Figure 23: (a): A modification of fig. 22 (a) where source terminals are placed onto the ground plane underneath terminals #1–#4, and a sink terminal #G is arbitrarily placed onto the ground plane. (orange: source terminals, blue: sink terminals). (b): The test circuit used to obtain the (mutual) ground-return inductances from the (mutual) partial inductances.

L_{11} and L_{21} can be obtained from V_1 , V_2 as shown in fig. 23 (b). Note that the transformation performed by fig. 23 (b) is equivalent to:

$$L_{i,j} = (v^{(i)})^T \cdot L^{(P)} \cdot v^{(j)} \quad \text{with: } v_k^{(a)} := \delta_{k,a} - \delta_{k,aP} + \delta_{k,aM} \quad (45)$$

where $\star^T$ denotes the transpose and δ is the Kronecker delta. For example:

$$\begin{aligned} L_{12} = & +L_{1,2}^{(P)} - L_{1,2P}^{(P)} + L_{1,2M}^{(P)} - L_{1P,2}^{(P)} + L_{1P,2P}^{(P)} - L_{1P,2M}^{(P)} \\ & + L_{1M,2}^{(P)} - L_{1M,2P}^{(P)} + L_{1M,2M}^{(P)} \end{aligned}$$

Fig. 24 helps to understand the proposed process, which computes (mutual) ground-return inductances from (mutual) partial inductances, more intuitively: Part (a–c) visualize three distinct single-source solutions of the spatially discretized quasi-magnetostatic PDEs that appear while computing elements of $L^{(P)}$. Conversely, the solution in fig. 24 (d) is obtained as a superposition of (a–c), and it corresponds to the port-like excitations imposed by fig. 23 (b). Fig. 24 (d) is in good agreement with fig. 24 (e), which was computed using an electromagnetic field solver using the lumped port excitation from fig. 22 (a).

So far, the role of the inaccuracies due to spatial discretization and due to numerical errors in the linear solver have not yet been clarified. In the following, the error in the *computed (mutual) partial inductance* is quantified by two different means: Firstly, the relative deviation from the *exact, continuous solution* shall be called $\hat{\epsilon}^{(P)}$. Secondly, the relative deviation from the *exact solution of the spatially discretized equations* shall be called $\epsilon^{(P)}$. Furthermore, the analogous relative deviations in the (mutual) ground-return inductances are denoted by $\hat{\epsilon}$ or ϵ , respectively. Note that the discretization errors $\hat{\epsilon}^{(P)}$

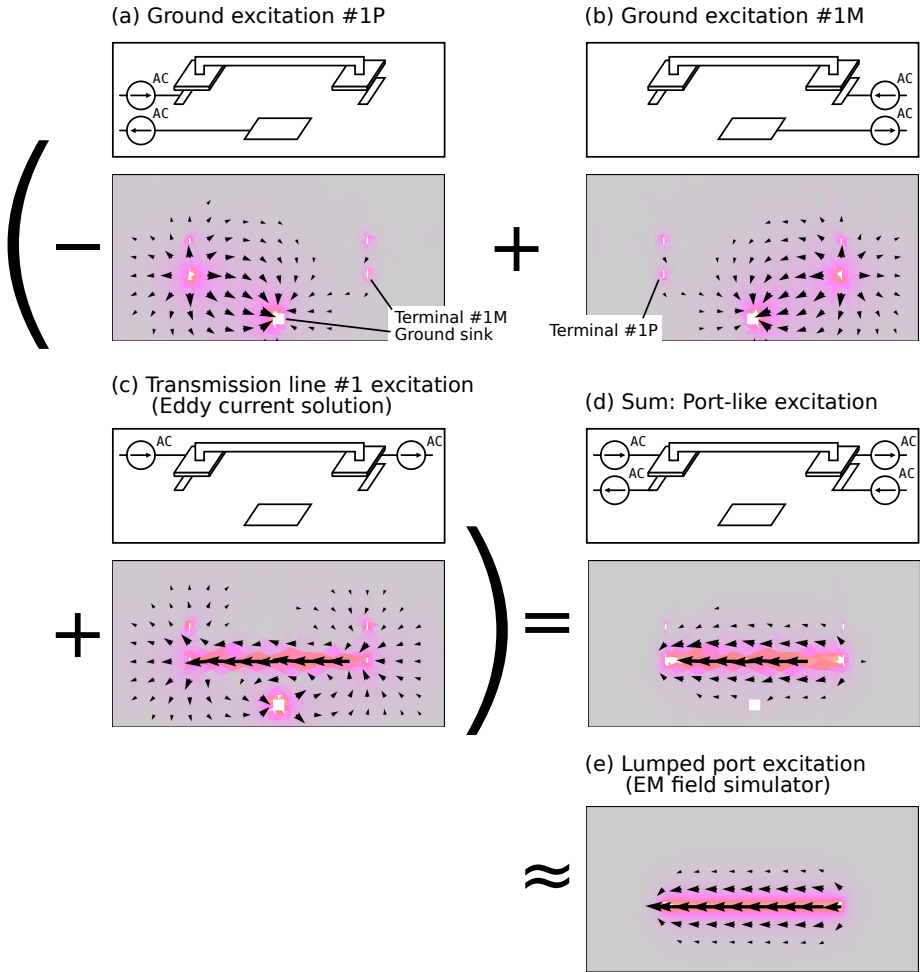


Figure 24: (a–d): AC currents in the ground plane which are solutions of spatially discretized quasi-magnetostatic PDEs with terminal excitations (Ansys Q3D). Part (e) shows the corresponding AC currents obtained by solving Maxwell's equations solver with lumped port excitations (Ansys HFSS) at 100 MHz. Note that the current field in part (c) equals fig. 22 (c), and in part (e) it equals fig. 22 (b).

and $\hat{\epsilon}$ are typically rather large, e.g. of the order of 1%–10%. In contrast, the numerical errors $\hat{\epsilon}^{(P)}$ and $\hat{\epsilon}$ are much smaller, and, in the case of direct linear solvers, they can be decreased arbitrarily by using a more wide floating point format.

Observe that the spatially discretized quasi-magnetostatic partial differential equations are linear as well. Therefore, if the numerical error $\hat{\epsilon}^{(P)}$ is neglected, the test circuit from fig. 23 (b) still computes the exact response of the *spatially discretized* system to a port excitation. Hence, the errors dis-

cretization $\hat{\epsilon}$ in L_{11} and L_{21} derived from fig. 23 (b) are *exactly the same as the discretization errors $\hat{\epsilon}$ of L_{11} and L_{21} derived by directly solving the discretized equations with lumped port excitations*, e.g. as it is done by electromagnetic field simulation. This property should be appreciated because it implies that the discretization error $\hat{\epsilon}^{(P)}$ is *not* amplified by subtractive cancellation in linear combinations of (mutual) partial inductances. This has some counterintuitive implications:

- With a discretization error of $\hat{\epsilon}^{(P)} \approx 10\%$, one might *naively* presume that no information is lost if the components of $L^{(P)}$ are printed in an ASCII-format with only two decimals. However, the introduced rounding errors are *uncorrelated errors* in the range of $1\% - -10\%$, which, unlike the discretization error $\hat{\epsilon}^{(P)}$, are amplified by subtractive cancellation. Therefore, this might ruin the accuracy of e.g. mutual pin-loop inductances derived from $L^{(P)}$.
- Some approaches might assemble a partial inductance matrix $L^{(P)}$ component by component from approximate analytic solutions or using look-up tables. Special care must be taken that the so-obtained numbers also have interpretations as exact solutions of a discretized, or otherwise simplified, complete system. Otherwise, the accuracy of e.g. derived mutual pin-loop inductances might be considerably worse, even if the (mutual) partial inductances themselves better approximate the continuum solution.

In the following, (mutual) partial inductances are called *matched* if linear combinations yield (mutual) ground-return and pin-loop inductances with errors smaller than expected from uncorrelated error propagation. This discussion has shown that components of $L^{(P)}$ obtained by repeatedly solving the quasi-magnetostatic PDEs *on the same mesh* are matched, and care must be taken not to spoil this matching.

In contrast, the relative numerical deviations $\dot{\epsilon}^{(P)}$ is amplified by subtractive cancellation: From eq. (45) follows that, in the worst case, the relative numerical errors $\dot{\epsilon}^{(P)}$ leads to a relative error in the (mutual) ground-return inductances $\dot{\epsilon}$ of¹⁰:

$$\frac{\dot{\epsilon}}{\dot{\epsilon}^{(P)}} = \frac{|(v^{(i)})^T| \cdot |L^{(P)}| \cdot |v^{(j)}|}{|(v^{(i)})^T \cdot L^{(P)} \cdot v^{(j)}|} \quad (46)$$

where here, $|\cdot|$ is read as a *component-wise* absolute value. A more pragmatic view is to regard the relative numerical errors as uncorrelated random variables,

¹⁰ Observe that eq. (44) can be put in the same form with some appropriate definition of $v^{(a)}$.

	Sym.	Test #1	Test #2	Test #3	Field-sim. †
Ground plane	–	yes	yes	yes	yes
Port excitations	–	yes	yes	no	yes
Frequency	–	∞ (q.s.) *	DC	∞ (q.s.) *	100 MHz
Partial inductance T.l. #1	$L_{11}^{(P)}$	17.5 nH	22.9 nH	18.0 nH	–
Mutual partial inductance T.l. #1 $\leftrightarrow$ T.l. #2	$L_{12}^{(P)}$	3.16 nH	4.98 nH	3.63 nH	–
Ground-return inductance T.l. #1 **	L_{11}	14.4 nH	18.8 nH	–	15.1 nH
Mutual ground-return inductance T.l. #1 $\leftrightarrow$ T.l. #2 **	L_{12}	0.187 nH	1.067 nH	–	0.204 nH
Tests #1–#3 correspond to quasi-magnetostatic solutions (Ansys Q3D), and the field simulation (†) is a solution of Maxwell's equations (Ansys HFSS). Tests #1 and #2 were obtained from the system depicted in fig. 23 (a), and tests #3 and #4 are based on fig. 22. Table cells in good agreement ($\pm 40\%$) with electromagnetic field simulations are colored in green. * quasi-magnetostatic inductances were computed under $\lim_{f \rightarrow \infty}$ ** results from fig. 23 (b) and eq. (45) were equal					

Table 4: Simulation results of the coupled transmission lines.

where $\dot{\epsilon}^{(P)}$ denotes the standard deviations. These stochastic errors propagate as follows ^{II}:

$$\frac{\dot{\epsilon}}{\dot{\epsilon}^{(P)}} = \frac{\sqrt{|(v^{(i)})^T|^2 \cdot |L^{(P)}|^2 \cdot |v^{(j)}|^2}}{|(v^{(i)})^T \cdot L^{(P)} \cdot v^{(j)}|} \quad (47)$$

where here, $|\cdot|^2$ is read as a *component-wise* absolute square. Amplification of numerical errors from the linear solver $\dot{\epsilon}^{(P)}$, as described by eqs. (46,47), may pose a limit to how far one may stretch the computation of (mutual) ground-return and pin-loop inductances from $L^{(P)}$.

3.3.2 Results of the Coupled Transmission Lines

The coupled transmission lines over a ground plane (sec. 3.3.1, fig. 22) have been simulated using a quasi-magnetostatic solver as well as using electromagnetic field simulation. The results are shown in table 4. In test #1, reference terminals are present on the ground plane, and the partial inductance matrix

^{II} This formula is, essentially, Gaussian error propagation.

$L^{(P)}$ was computed in the high-frequency limit (sec. 2.5.2). As indicated by the green highlighting in table 4, the (mutual) ground-return inductances L_{11} and L_{12} computed from $L^{(P)}$ in test #1 are in good agreement with electromagnetic field simulation. This shows the feasibility of the approach from sec. 3.3.1.

In test #2, the partial inductance matrix was computed at DC, which results in an L_{12} that is too large by roughly a factor of 5. This reflects the fact that DC-inductances are incapable of expressing magnetic shielding (see sec. 2.5.2). Test #3 in table 4 corresponds to the system from fig. 22, where the reference terminals are omitted. Observe that $L_{12}^{(P)}$ from test #3 is roughly 19 times larger than L_{12} from test #1. This confirms that the mutual partial inductance between two transmission lines over a ground plane can be much larger than the mutual ground-return inductances.

In the computation of L_{12} in test #1, relative numerical errors $\epsilon^{(P)}$ in $L^{(P)}$ are amplified by a factor of 71 in the worst case. This was calculated using eq. (46). Conversely, according to eq. (47), the standard deviation of uncorrelated random relative numerical errors are amplified by a factor of 28. These factors are representative of a ratio between the distance of the transmission lines and the height over the ground plane of roughly 5.4 : 1 (see fig. 22), and they are expected to increase with the distance. This again emphasizes the importance of ensuring and conserving the *matching* (sec. 3.3.1) among mutual partial inductances in the linear solver as well as in the storage format.

3.3.3 Converting Terminal-based H-Parameters into Lumped-Port-based H-Parameters and Generating the Equivalent Circuit

In addition to inductances and resistances, a package model also includes capacitances. As explained in sec. 2.5.2, the lumped-elements circuit created by parasitic extraction tools can be understood in terms of *terminal-based H-parameters* (sec. 2.5.2). These terminal-based H-parameters exhibit a block structure, in which the upper left block describes the partial inductance matrix $L^{(P)}$, and the lower right block contains information about the capacitances. In contrast, the *port-based H-parameters* from sec. 3.2.2 contain the (mutual) *ground-return* inductances in their upper left block. In the following, it will be shown how these different H-parameter representations can be converted into each other algorithmically. This can be understood as a generalization of the approach for computing individual (mutual) ground-return inductances from $L^{(P)}$ described in sec. 3.3.1.

The terminal-based H-parameters are referred to the “voltage at infinity”, as shown in fig. 14 (b). In the first step, the reference is changed to the ground sink (#G in fig. 23), and the “voltage at infinity” is then rendered floating.

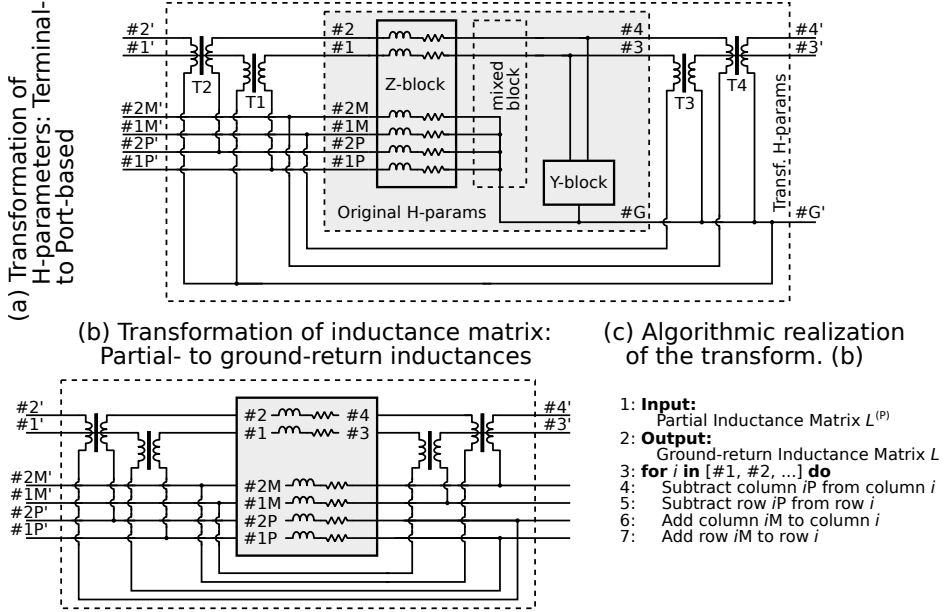


Figure 25: Part (a) shows how four transformers (T1–T4) applied to an electromagnetic model with terminal-excitation semantics (gray box, on the example of fig. 23 (a)) in order to convert it into a model with port-excitation semantics. Part (b) shows the same transformation merely applied to the Z-block, i.e. the subcircuit representing (mutual) partial inductances.

These transformations merely affect the Y-block, i.e. the capacitive subcircuit, and the mixed block in a quite trivial way. The gray box in fig. 25 (a) shows an equivalent circuit of the so-obtained H-parameters (see sec. 2.4.1).

Subsequently, the terminal excitations will be changed into port-like excitations. This is formally expressed by attaching multiple ideal transformers externally, as shown in fig. 25 (a). Now assume that the transformers T3 and T4 can be approximately exchanged with the Y-block, which represents the capacitors, as well as with the mixed block¹². Then the transformers T1–T4 and the Z-block form a proper subcircuit, which is depicted in fig. 25 (b). This can be understood as a transformation that maps the partial inductance matrix $L^{(P)}$ to the ground-return inductance matrix L . It is left to the reader to show that the algorithmic realization in fig. 25 (c) is exactly equivalent¹³. Finally,

¹² This can be justified as follows: Recall from sec. 2.5.2 that the distribution of these capacitances is merely heuristical, and may be changed arbitrarily. Therefore, the Y-block may be attached at nets #1, #2 and #1P instead. Subsequently T3 and T4 can be trivially exchanged with the mixed block.

¹³ If $L^{(P)}$ and L are regarded as the Gramian matrices of bilinear forms [19], then the transformation from $L^{(P)}$ to L is formally a change of basis, i.e. $L = B^T L^{(P)} B$, with a suitably-defined change-of-basis matrix B .

the rows and columns corresponding to #1P', #1M', #2P' and #2M' are deleted from the H-parameters, which is equivalent to leaving the corresponding terminals unconnected.

Assume that the port-based H-parameters are given. This can be either achieved using the transformation described above, or by using the output of an electromagnetic field simulation at a single frequency point (sec. 3.2.2). Then, an equivalent circuit can be generated using the constructions in fig. 8 and fig. 7 (a) and (b) from sec. 2.4.1. This equivalent circuit is an electrical model of the package, the terminals of which have lumped-port semantics (see sec. 2.5.1). If the H-parameters originate from an electromagnetic field simulation, at this point, their mixed part must be forced to a binary matrix. This approximation is similar to the approximations inherent to parasitic extraction (sec. 2.5.2). It is tolerable if the size of the current loop is significantly smaller than the wavelength.

3.3.4 Evaluation on the Example of the LQFP-64 Package

The parasitic extraction tool Q3D was applied to the IC-package shown in fig. 17 (a). In test #1 and #2, the obtained RLCK-circuit was converted to port-like excitations using the transformation from sec. 3.3.3. The results are shown in table 5. Similar to sec. 3.3.2, in test #1, the partial inductance matrix $L^{(P)}$ was computed in the high-frequency limit. In test #1, the agreement of the (mutual) pin-loop inductances $L_{12;34}$ and $L_{34;34}$ with electromagnetic field simulation is acceptable. Moreover, the total pin capacitance at TR0 (table 5) is predicted very accurately. Hence, the approach from sec. 3.3.3 was validated.

If the partial inductance matrix is instead computed at DC (test #2 in table 5), the mutual pin-loop inductance $L_{12;34}$ is overestimated by a factor of 10. This is in line with the results from sec. 3.3.2. In test #3, reference terminals on the ground plane were omitted, and in test #4, the entire ground plane was removed. Hence, in tests #3 and #4, the transformation from sec. 3.3.3 is not applicable. In test #3, the mutual pin-loop inductance $L_{12;34}$ is overestimated¹⁴ by a factor of 4.7, and in test #4, it is over-estimated by a factor of 8.6. Thus, if no reference terminals are implemented, the RF-emissions can be over-estimated by up to 13 dB. This follows from eq. (39). Moreover, if the entire ground plane is removed, the RF-emissions can be over-estimated by up to 19 dB.

Using eq. (46) it was calculated that the amplification factor of numerical errors in the mutual ground-return inductance L_{14} is 18 in the worst

¹⁴ The corresponding (mutual) pin-loop inductances in table 5 are formally computed using fig. 19 (b) as well. However here, the characterized subcircuit is the raw-output of Ansys Q3D, which does not have lumped-port semantics. The current path is thus not fully closed.

	Sym.	Test #1	Test #2	Test #3	Test #4	EM field §
Ground plane	–	yes	yes	yes	no	yes
Port excitations	–	yes	yes	no	no	yes
Frequency	–	∞ (q.s.)	DC	∞ (q.s.)	∞ (q.s.)	100 MHz
Mutual ground-return inductance (TRO, VS#0) *	L_{24}	24.3 pH	–74.8 pH	48.6 pH	–61.1 pH	19.6 pH
Mutual pin-loop inductance (VTR#0, TRO)↔ (PGND#0, VS#0) †	$L_{12;34}$	–3.4 pH	–33.5 pH	–16.0 pH	–29.1 pH	–5.4 pH
Pin-loop inductance (PGND#0, VS#0) †	$L_{34;34}$	5.1 nH	6.6 nH	5.1 nH	5.6 nH	5.7 nH
Total pin-cap. at TRO **	C_{66}	0.63 pF	0.63 pF	0.63 pF	0.63 pF	0.58 pF
Tests #1–#4 are based on an RLCK-circuit obtained using a parasitic extraction tool (Ansys Q3D). In tests #1 and #2 the transformation described in fig. 25 was applied, whereas in tests #3 and #4 the RLCK-circuit was not modified. Table cells in good agreement ($\pm 40\%$) with electromagnetic field simulations are colored in green. § electromagnetic field simulation data was taken over from table 2. The shown quantities were obtained using the following test circuits at $f = 10$ MHz: *: fig. 19 (a) †: fig. 19 (b) **: fig. 19 (c)						

Table 5: Circuit parameters of a LQFP-64 package model obtained using parasitic extraction.

case. Assuming uncorrelated random numerical errors, the amplification of the standard deviation is by a factor of 7.8, which follows from eq. (47). By combining the 4-term formula eq. (43) and the 9-term formula eq. (45), the mutual pin-loop inductances can be calculated directly from the mutual partial inductances:

$$L_{m,n;l,k} = (v^{(m,n)})^T \cdot L^{(P)} \cdot v^{(l,k)}$$

with: $v_k^{(a,b)} := \delta_{k,a} - \delta_{k,aP} + \delta_{k,aM} - \delta_{k,b} + \delta_{k,bP} - \delta_{k,bM}$ (48)

Written out in full, this formula would be a sum over 36 terms. By substituting the Kronecker delta vectors $v^{(m,n)}$ and $v^{(l,k)}$ into eqs. (43, 44), the numerical error in the mutual pin-loop inductances can be estimated. The error in $L_{12;34}$ was amplified by a factor of 444 in the worst case, and its standard deviation was amplified by 104. Since $L_{12;34}$ is rather small and close to the RF-emission limits (sec. 3.1), these numbers can be understood as worst case figures.

3.3.5 Conclusion

It was shown that using the conventional approach, which either uses a floating ground-plane or no ground plane at all, can lead to large errors in EMC-simulations. In sec. 3.3.4, it was shown that the error can be up to 19 dB if no ground plane is present, and up to 13 dB if a floating ground plane is used. Sec. 6.5.5 will confirm that these estimates are quite accurate. This issue could be resolved by converting the terminal-based H-parameters to port-based H-parameters, which requires additional reference terminals. The so-obtained lumped inductances and inductive couplings correspond to (mutual) ground-return inductances instead of (mutual) partial inductances. This is the main difference between the method proposed in this section and the conventional approach using parasitic extraction.

For brevity, in the following, the linear solver that is invoked by the quasi-magnetostatic solver will be simply be denoted by *linear solver*. In the following, a tolerance region of $\pm 40\%$ is assumed for the mutual pin-loop inductances $L_{12,34}$. Since the statistical error amplification factor is 104 (sec. 3.3.4), if the linear solver's relative numerical error is above 0.37%, the predicted RF-emissions at the pin TRO are expected to be inaccurate. Moreover, since the relative numerical error is amplified 444 in the worst case (sec. 3.3.4), it would be even desirable to have the linear solver's relative numerical error bounded by 10^{-4} . This illustrates that EMC-simulations pose quite stringent demands on the quasi-magnetostatic solver. In direct linear solvers, this error is related to the bit count of the floating point format. However, in iterative linear solvers, the numerical error is usually considerably larger, and depends on its configuration. Therefore, it is desirable to characterize unknown proprietary quasi-magnetostatic solvers. To this end, the coupled transmission lines from sec. 3.3.2 can be used as a stress test: Their distance should be increased up to point of numerical failure, which is indicated by a non-physical cusp in the mutual inductance. The statistical error amplification factor at this point, which is calculated using eq. (47), is an estimate of the linear solver's relative numerical error.

It was shown that deviations of the discretized solution from the continuous solution are correlated. This is a kind of *matching* among (mutual) partial inductances. If this matching is lost, the mutual pin-loop inductances cannot be predicted accurately. Therefore, (mutual) partial inductances should be specified with at least 3 additional decimals. Also the (mutual) ground-return inductances are matched, albeit here, this effect is considerably less critical: This is found by comparing the worst-case error amplification when computing $L_{12,34}$ from mutual partial inductances, which is 444, to the error amplification factor from sec. 3.2.3, which is 14. Nevertheless, when exporting the final

lumped-elements circuit to an ASCII format, at least 2 additional decimals should be used.

Because only data from a single frequency point is used, subtle frequency-dependencies of the resistance and inductance due to the skin effect (see sec. 2.5.2) are lost. However, this thesis proposes that frequency-dependent resistances could be heuristically reintroduced as follows: Firstly, in the Z-block in fig. 25, the real component is taken from the DC solution instead. Then, certain heuristical ladder circuits that approximate the skin effect [102] are placed in series with each source terminal of the Z-block. It is presumed that the skin effect losses are primarily in the bond wires. Thus, if the bond wire diameters are supplied in tabular form, quite accurate latter circuits can be generated. Observe that this construction only modifies the diagonal of L , and note that the mutual pin-loop inductances only depends on off-diagonal components of L – see eq. (43). This proves that the delicate matching between the inductive couplings is not impaired.

3.4 Summary

- Mutual mutual pin-loop inductance of only 5.4 *pico*-Henries, i.e. roughly three orders of magnitude below the typical pin-inductance, between transceivers and DC/DC-converters can cause violations of the RF-emission limits.
- Package-models for EMC-simulations are required to (1) accurately represent these very small long-range mutual inductances, (2) exhaustively include all kinds of long- and short-range couplings (3) account for the magnetic shielding of bond-wire and lead-frame parts caused by the PCB-ground plane and (4) pose a realistic impedance to a non-zero total current that enters the IC-pins and leaves via the exposed pad.
- In IC-package models based on electromagnetic field simulation, an artificial metallic extension on the die-pad was proposed. This is an effective technique to describe AC-currents through the exposed pad, and the difficulties associated with the floating reference are avoided. A canonical representation are the port-based H-parameters. Their Z-block contains the (mutual) ground-return inductances whereas their Y-block contains the pin-capacitances.
- Reduced-order macromodels in the S-parameter representation are prone to characteristic cancellation errors in the mutual ground-return inductances and mutual pin-loop inductances at low frequencies. This can be avoided by applying vector fitting to the port-based H-parameter representation. However, in this representation, the Hamiltonian passivity enforcement algorithm fails. Independent of the macromodel's parameter format, the small long-range mutual pin-loop inductances, which are important in EMC-simulations, suffer from another kind of cancellation artifact.
- Synthesizing lumped-element models containing ground-return inductances are an alternative to reduced-order macromodels – they allow for a more compact representation and are less prone to numerical issues. Furthermore, it allows for insightful alteration analyses and root-cause studies. The contained lumped inductances and inductive couplings correspond to (mutual) ground-return inductances instead of (mutual) partial inductances. This is different from some conventional approaches.
- In the conventional approach using quasi-magnetostatic solvers, the ground plane either neglected or simply introduced as a floating conductor. It was shown that the error can be up to 19 dB if no ground plane is present, and up to 13 dB if a floating ground plane is used. This can be resolved by introducing terminals to the ground plane, and by converting the terminal-based H-parameters to port-based H-parameters.
- EMC-simulations pose quite stringent demands on the quasi-magnetostatic solver: From the requirements posed by EMC-simulations, it was deduced that the quasi-magnetostatic solver's linear solver's relative numerical error should be bounded by 10^{-4} . In this respect, proprietary quasi-magnetostatic solvers can be characterized using two coupled transmission lines.

CHAPTER 4

Investigation of Inductances and RF-Losses in On-Die Power Routing

4.1 Introduction

In order to estimate the partial inductance of on-die power routing, a crude rule of thumb is to assume 1 nH/mm [92]. Ground or supply nets that are connected via multiple pins, e.g. the battery supply or a pre-regulated supply, can exhibit ground-return inductances as low as 3 nH (e.g., see sec. 6.7). Thus, it is plausible that, in an IC with a die-area of e.g. 10 mm², the on-die power/ground routing in series with the pins significantly contributes to the total inductance.

Since the partial inductance matrix in RLCK-extraction cannot be sparsified easily (sec. 2.6.1), it is important to apply this technique very selectively. For example, assume that weak inductive couplings between power routing and sensitive signals are *not* a concern: Then, the power-routing in the lower four metal layers can usually be neglected for frequencies below 1 GHz. This is due to the fact that the self-inductance vanishes in the series resistance.¹ Furthermore, in numerous other cases, the self-inductance of on-die routing is negligible as well: Firstly, wherever possible, bond pads are placed directly on top of the connected power transistors (sec. 2.2). Secondly, supply- or ground-pins shared among multiple modules are often routed using rather wide metal plates, which also reduces the parasitic inductance. Third, the seal-ring and the system ground usually meet at a star point (sec. 2.1), which is directly connected to the bond pad. Hence, the AC-voltage of the seal-ring, which is highly relevant for substrate-coupled RF-emissions (see sec. 6.7), is largely unaffected by the on-die routing inductance.

On the other hand, in RF-immunity testing, in addition, weak on-die inductive couplings might be implicated [169]. This requires to include sensitive nets in the RLCK-extraction as well. For example, this might be long-distance routing of the bandgap-voltage, provided that it is not low-pass filtered (sec. 2.1), or the inputs of an OTA. Moreover, also more high-ohmic power-routing that can carry a high AC-current in RF-immunity testing should be include in the RLCK-extraction in simulations of the IC's susceptibility. This is because these nets may act as an aggressor. The question arises how precise RLCK-extraction

¹ The exact corner frequency is a function of the trace width, and can be estimated using the 1 nH/mm rule of thumb.

tools can predict weak inductive couplings in BCD-technologies across large distances.

The characteristics of the internal low-voltage power domains vary strongly among different implementations. In the following it is assumed that, for $f > 100$ MHz, the output impedance is dominated by the internal bypass-capacitor of 70 pF. Furthermore, assume the internal regulator supplies an analog module via the power-metallization, with a total loop inductance of 3 nH. The analog module shall have a capacitance of 10 pF. In this scenario, the power impedance at the analog module is dominated by the routing inductance above 350 MHz. If the dynamic voltage drop above e.g. 350 MHz is a concern for the EMC, it is recommended to include these interconnects in the RLCK-parasitic extraction. Moreover, this power domain has a resonance near 900 MHz if the quality factor is sufficiently high. Especially in future high-frequency extensions of DPI-testing, such resonances might be excited. While the frequency of these resonances are easily calculated, their quality factor is very difficult to predict because numerous effects contribute to high-frequency losses. For example, in most BCD-technologies, the ESR of on-chip capacitors are layout-dependent and not thoroughly characterized. Contributions to the high-frequency losses are also found in the power distribution network. This raises the question how well these losses can be predicted using conventional RLCK-extraction techniques.

For example, in RFIC-design it is known that magnetically-induced eddy currents in the substrate [120] or in the metal plates [53] may substantially alter the interconnect resistance and inductance [71] at high frequencies. However, the construction of circuit models for substrate eddy currents is highly involved [155], [179], and traditional extraction tools typically neglect this: In the classical framework of parasitic extraction (see sec. 2.5.2), this effect cannot be properly represented because the partial inductance and resistance matrices are frequency dependent.

4.2 Test Wafers and Test Structures

In the course of this thesis, test wafers were developed, in order to experimentally study on-die inductive effects. The aims of these experiments are twofold: Firstly, a better understanding of the on-die power supply network's high-frequency physics is sought. The second aim is to provide a prototype for testing of RLCK parasitic extraction tools for EMC simulation applications: A meaningful tool qualification must expose both the algorithmic *strengths and weaknesses*, in order gain an understanding of the tool's "trust-region".

Most of the developed test structures consist of low-ohmic power metal only (sec. 2.2), and some of the test structures are multiple millimeters in

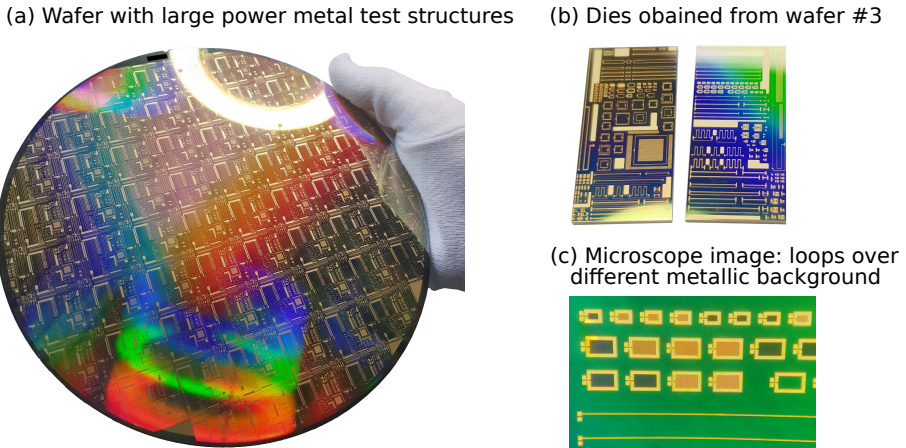
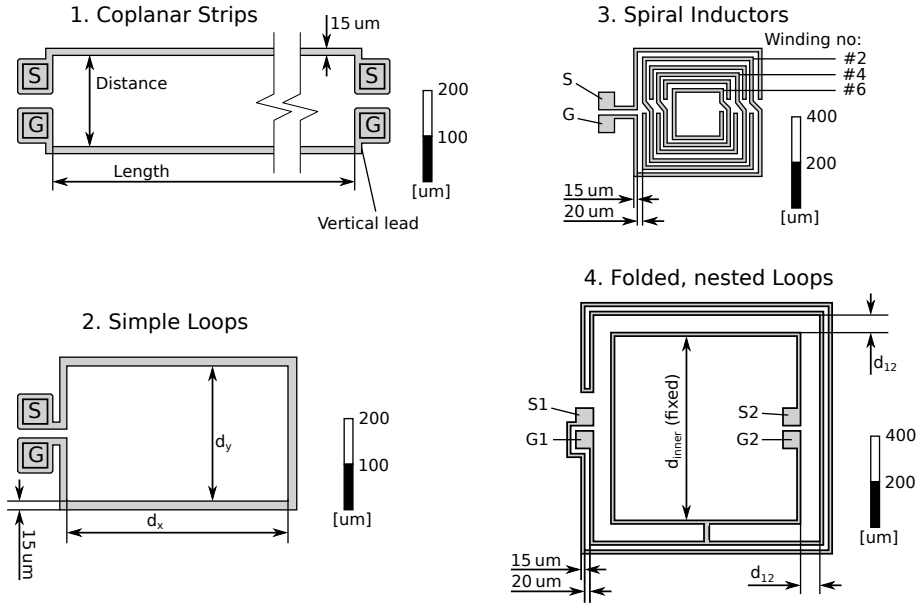


Figure 26: (a) Wafer #1 from the split lot, where a simplified BCD-process was implemented. Wafer #3 was diced, as shown in (b). Part (c) shows multiple variants of power metal loops, as well as two transmission lines.

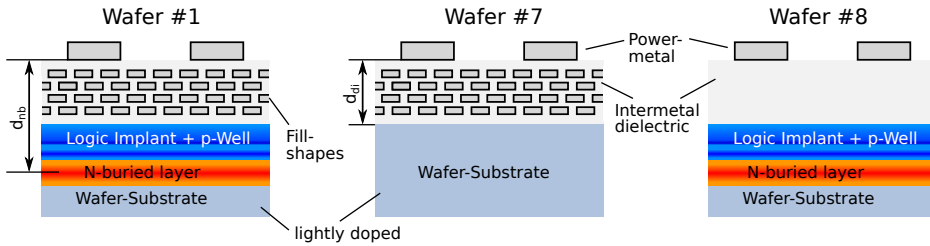
length. Consequently, their size is in the same order of magnitude as the power routing of an integrated circuit, and therefore it is presumed that they cover the spectrum of physical effects relevant for power routing. These test structures are characterized by means of 1- and 2-port on-wafer measurements using a vector network analyzer (sec. 2.4.3) up to 8.5 GHz. Because many geometry variations are realized for each type of test structure, a series of test structures requires a sizeable amount of silicon area. Therefore, production with a complete set of photomasks using shared reticles would still be very expensive. Instead, a strongly reduced set of photomasks and process steps were defined in close collaboration with Infineon's semiconductor fabrication plants. This simplified process implements a homogeneous and unstructured doping profile, and allows to pattern multiple metal layers using a single, inexpensive reticle. Most via layers and the deep trenches were omitted in order to simplify the manufacturing process. Hence, the substrate, the n-epitaxial layer and all wells are electrically floating and the n-epitaxial layer is not segmented. A split lot of eight wafers were produced using this process. Images of a wafer and some test structures are found in fig. 26.

In wafer #1, the doping profile emulates an LV/MV-pocket of the Infineon BCD-technology (see sec. 2.2) that served as a template for this process. Moreover, in wafer #1, fill- and cheese-shapes (see sec. 2.2) are present in the metallization and are dimensioned as in this BCD-technology. The wafers in the split lot are processed with different parameters: As shown in fig. 27 (b), in wafer #7, the epitaxial layer growth and all implant steps were omitted, whereas, in all other respects, it is identical to wafer #1. The processing steps of

(a) Four different kinds of test structures that we will discuss in detail



(b) Cross sections of wafers on the example of the coplanar strip



(c) Test structure variants with metallic background on the example of wafer #1

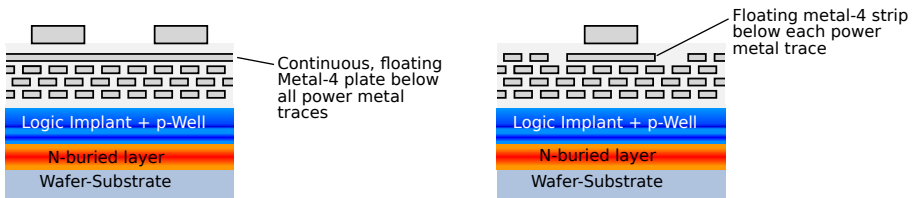


Figure 27: Illustrations of the kinds of test structures, semiconductor processing variants and structural variants in the patterning of the lower metal layers, which will be discussed in this section. Cheese-shapes are present in the metal plates and strips in (c), but were not shown for clarity. The distance d_{nb} measures the distance from the bottom of the power metal layer to the dopant concentration peak of the n-buried layer.

wafer #8 are also derived from wafer #1. Here, a process modification removes the four fine-pitch metal layers. Thereby, the fill-shapes are completely omitted. The height of the intermetal dielectric in wafer #8 is roughly matched to the height of the complete metal stack in the standard process (i.e. wafers #1 and #7), which is denoted by d_{di} . By default, the background of the power metal test structures is a dense fill-pattern, i.e. as in fig. 27 (b) for wafer #1 and #7. Some structure variants of the test structures in which the top-most lower metal layer is replaced by a continuous, floating plate or strip were manufactured. This is depicted in fig. 27 (c).

Fig. 27 (a) shows four kinds of test structures, which are of particular importance. Coplanar strips with large strip distances of up to roughly 0.4 mm and lengths up to 7.44 mm were created from power metal. In this chapter, these structures represent the primary means of probing the high-frequency physics of the on-die power supply network. Due to their simplicity, they allow for precise testing of the theory and of RLCK-extraction tools. These coplanar strips will be addressed in sec. 4.5. The simple loops, the spiral inductors [14] and the folded, nested loops shown in fig. 27 (a) lack translation symmetry and exhibit currents flowing in both x- and y-direction. Thereby, they allow to evaluate RLCK-extraction tools with respect to the treatment of true 3D structures. Also, the ability to assemble a composite circuit from the capacitance matrix and the partial inductance matrix can be tested. The result of this evaluation is presented in sec. 4.6.

4.3 Electromagnetic Field Simulation and Parasitic Extraction

To provide additional validation, 3D EM-field simulations of all measured test structures were performed using Ansys HFSS. Each simulation contains one complete test structure, including the pads that are used for contacting it by the wafer probers. In these simulations, the excitations are lumped ports that are placed differentially between the source and ground pad. The three-dimensional geometry of conductors was obtained by importing GDS-II files and extruding these 2D polygons to the thickness of the respective metal layer. The microscopic fill- and cheese-shapes were not included because the size of the mesh would otherwise exceed reasonable bounds. The HFSS simulation model also contains the intermetal dielectric as well as an elaborate model of the substrate. This is illustrated by the cross section in fig. 28. To describe the substrate, multiple layers of different resistivity ρ that mimic the doping profile are added. In each layer, the resistivity ρ is homogeneous, i.e. constant in (x, y, z) . The p-n-junctions between the logic implant, the

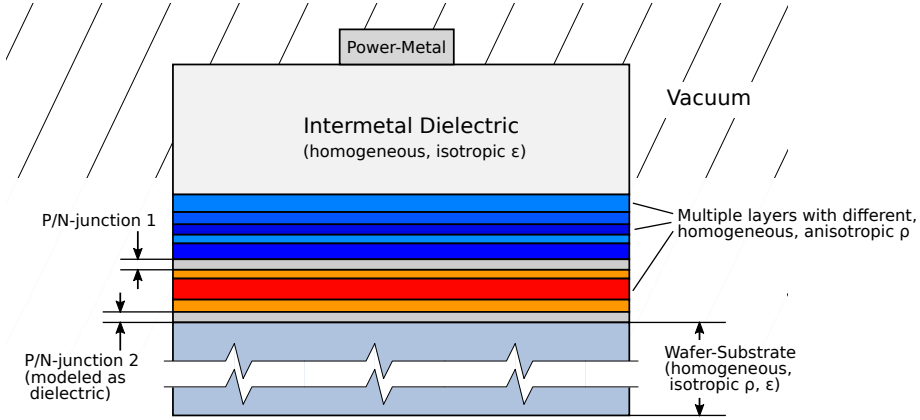


Figure 28: Example cross section of a HFSS simulation model of a power metal test structure, including the substrate. This system is surrounded on all sides by a considerably larger vacuum box. The number of substrate layers shown here are different from the actual simulations, and the dimensioning and coloring in this figure does not reflect the actual doping profile used. All dimensions are not to scale.

n-epitaxial layer and the wafer-substrate were emulated using thin dielectric layers. The thickness of these dielectric layers roughly equals the size of the p-n-junctions' depletion regions, and the dielectric constant was adjusted such that their capacitances match the p-n-junctions' capacitances at a bias of 0 V. Since the wafer-substrate is a poor conductor, in addition to a resistivity ρ , it is parameterized by a dielectric constant ϵ as well.

In the substrate, the resistivity ρ is z-dependent and is related to the concentration of n-carriers n_0 , the concentration of p-carriers p_0 and their mobilities μ_n, μ_p as follows:

$$\rho(z)^{-1} = n_0(z)\mu_n(z) + p_0(z)\mu_p(z) \quad (49)$$

The carrier concentrations n_0, p_0 can be computed from the concentration of donor and acceptor dopants N_D and N_A using standard text-book formulas [12], [49]. In order to compute the mobilities of majority and minority carriers, the formulas from [33] and [3] were used. They contain correction terms for high acceptor or donor concentrations. These correction terms were found to be necessary, in order to obtain the correct sheet resistances. Each substrate layer in fig. 28, which spans the z-interval $[z_0, z_1]$, is associated with two

Name	Extraction type	Inductance Model	Fracture length
frac500u	rlck_coupled	-peec_model	500 um
frac200u	rlck_coupled	-peec_model	200 um
frac50u	rlck_coupled	-peec_model	50 um
laddernets	rlck_coupled	-peec_model -wide_band_model	200 um
Remarks: The version 18r01 of QRC was used, and parasitic reduction was disabled. The option -substrate_profile was not used. The -filter_size equals 0.5 um.			

Table 6: Specification of three different settings used to test Quantus QRC.

different resistivities ρ_z and ρ_{xy} , which are defined as different kinds of averages over the z -dependent resistivity ρ :

$$\rho_z = \frac{1}{z_1 - z_0} \int_{z_0}^{z_1} \rho(z) dz \quad \rho_{xy} = \left(\frac{1}{z_1 - z_0} \int_{z_0}^{z_1} \rho(z)^{-1} dz \right)^{-1} \quad (50)$$

It is demanded that the stack of substrate layers has a correct resistance with regard to vertical as well as lateral currents. It is left to the reader to show that this is only exactly satisfied ² if each substrate layer is assigned an *anisotropic resistivity* with a resistivity tensor of $\text{diag}(\rho_{xy}, \rho_{xy}, \rho_z)$.

The RLCK-extraction was performed using Quantus QRC [30] with a modified runset. The tested configurations are specified in table 6. In the evaluations of RLCK-extraction, a layout containing multiple test structures was extracted, and the resulting netlist was simulated using S-parameter analysis (see sec. 2.3.3). The so-obtained many-port S-parameter dataset was split into multiple, smaller 1-, 2- or 4-port datasets. Like the electromagnetic field simulation described above, this parasitic netlists also includes the pads.

4.4 RLCG Parameters of the Coplanar Strips

The test wafer contains an array of coplanar strips as shown in fig. 27 (a). The distance is varied in five steps, and for each distance, there exist four length variants, namely, 0.44 mm, 2.44 mm, 4.94 mm and 7.44 mm. The raw measurement and simulation results of the coplanar strips are in the form of two-port S-parameters. In the experiments, GS- and SG-wafer-probers were used, and the VNA was calibrated up to the prober tips using SOLT-calibration, as described in sec. 2.4.3. This network data is embedded in

² Clearly, in the limit $|z_1 - z_0| \rightarrow 0$ the averages ρ_z and ρ_{xy} converge, and an isotropic ρ is sufficient. However, with the layer thicknesses used here, this limit is not a good approximation.

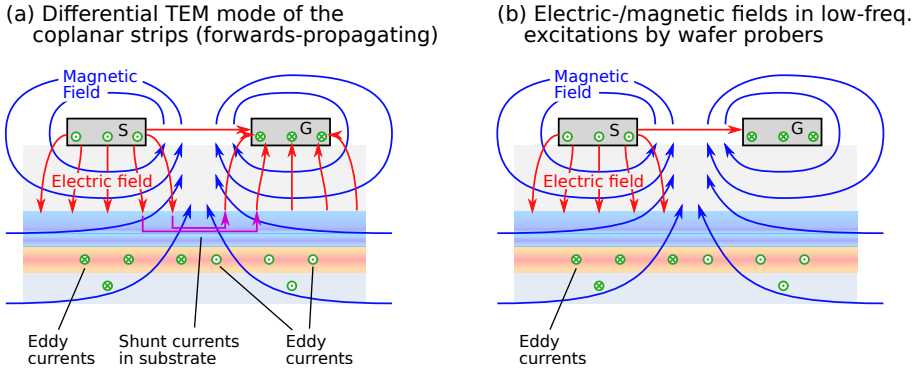


Figure 29: Part (a) shows the TEM-mode created by a differential excitation, such as in the HFSS simulations or for $f > 2$ GHz. Part (b) shows the postulated E - and B -fields in measurement for $f < 400$ MHz. This is a superposition of a forwards-propagating differential mode, and a forwards- and a backwards-propagating common mode.

the capacitances of the pads, which may be large in comparison to the total capacitance of these transmission lines. Moreover, the data is embedded in the inductances of the vertical leads. In order to remove these unwanted parasitics, a variant of the THRU-de-embedding [124] was used: For each distance step, the shortest coplanar strips, which is of length 0.44 mm, is used as de-embedding structure. From its ABCD-parameter representation (see sec. 2.4.2), a frequency-dependent series impedance $a_{12}/2$ and shunt impedance $a_{21}/2$ is obtained. These are then removed from the left and right port of all coplanar strips by appropriately-ordered inverse cascading operations. This reduces the effective lengths of the remaining coplanar strips to 2.0 mm, 4.5 mm and 7.0 mm.

In a transmission line, i.e. a structure whose cross-section is independent of the z -coordinate, any solution the time-harmonic Maxwell's equations can be written as a superposition of forwards- and backwards-propagating modal solutions, which have a simple sinusoidal dependence on z [182]. Below the cutoff frequencies of TE- and TM-modes³, only the TEM-modes (transverse electromagnetic modes) are relevant. In each TEM modal solution, the field lines of the E and B -field are parallel to the xy -plane. The coplanar strips exhibit two TEM-modes: A common mode, in which the substrate acts as a return conductor, as well as a differential mode.

Fig. 29 (a) illustrates the differential TEM-mode that is characterized. Here, the left conductor, which is contacted by the wafer prober's signal pin, carries a current in $-z$ -direction. Conversely, the right conductor (contacted by the wafer prober's ground pin) carries the return current. As will be shown

³ These cutoff frequencies are well beyond the frequency range considered here.

experimentally in sec. 4.5.1, magnetic field lines penetrate deeply into the substrate. Due to the comparatively large distance, the electric field lines predominantly terminate on the substrate. Now, consider the case where the wafer probes couple to this differential TEM-mode only. Then, elementary transmission line theory [182] may be applied. It can be shown that the two-port ABCD-parameters of a lossy, 1-conductor transmission line are related to its RLCG parameters as follows [135]:

$$a = \begin{pmatrix} \cosh(l\sqrt{Z_{\text{series}}Y_{\text{shunt}}}) & \sqrt{\frac{Z_{\text{series}}}{Y_{\text{shunt}}}} \sinh(l\sqrt{Z_{\text{series}}Y_{\text{shunt}}}) \\ \sqrt{\frac{Y_{\text{shunt}}}{Z_{\text{series}}}} \sinh(l\sqrt{Z_{\text{series}}Y_{\text{shunt}}}) & \cosh(l\sqrt{Z_{\text{series}}Y_{\text{shunt}}}) \end{pmatrix}$$

with: $Z_{\text{series}} := R + i\omega L$ $Y_{\text{shunt}} := G + i\omega C$ (51)

where R , L , G and C are the series resistance-, series inductance-, shunt conductance-, and shunt capacitance per length, respectively, and l is the length of the transmission line. Different methods have been proposed for inverting eq. (51), in order to obtain R , L , G and C from a : Some methods use only products and quotients of a_{12} and a_{21} [41], while others exploit a_{21} and a_{22} instead [162]. However, such methods suffer from a singularity at multiples of $\lambda/2$, and might have large numerical errors at very low frequencies. In the following, a novel method, which is based on the insight that eq. (51) may be rewritten as a matrix exponential, is proposed ⁴:

$$a = \exp \left(l \begin{pmatrix} 0 & Z_{\text{series}} \\ Y_{\text{shunt}} & 0 \end{pmatrix} \right) \quad (52)$$

Then, the RLCG-parameters are obtained by inverting eq. (52) using the matrix logarithm, which acts as a complex logarithm on all eigenvalues ⁵. Care must be taken to use the continuation of the complex logarithm on the associated Riemann surface ⁶, such that the branch cut at $n\lambda/2$ is treated correctly. Since Z_{series} and Y_{shunt} are the ABCD-parameters of an infinitesimal segment, it is clear that R summarizes the DC series resistance of the power metal conductor, the skin effect losses and the eddy current losses in the substrate.

⁴ The equivalence between eq. (52) and eq. (51) can be shown arithmetically. An alternative derivation is also found in [1].

⁵ Note that this method is easily generalized for multi-conductor transmission lines, using the $2n$ -port ABCD-parameters described in sec. (2.4).

⁶ A frequency-dependent eigen-decomposition that is continuous in f must be computed, which requires that eigenvalues are properly re-ordered. Then, a suitable branch of the Riemann surface should be selected for each frequency point and for each eigenvalue, such that the so-computed, new eigenvalues are continuous in f as well.

Conversely, G summarizes the losses due to the shunt currents in the substrate (fig. 29 (a)), and due to the loss angle in the intermetal dielectric. Note that the de-embedding and the matrix logarithm is applied to measurement, field simulation and RLCK extraction simulation data in the same way.

4.4.1 Error Calculation and Artifacts at Low Frequencies

The continuous curves in fig. 30 (a) show $\text{Im}(a_{12})$ of the three coplanar strips for distance $d = 0.385$ mm obtained from measurement and after de-embedding. The dashed curves ($\text{Im}(\log(a)_{12}) = \omega l L$) are obtained by means of applying the matrix logarithm as explained above. It can be seen that $\log(a)_{12}$ coincides with a_{12} for $\lambda \ll 2l$, and it can be seen that $\log(a)_{12}$ does *not* appear singular at $l = \lambda/2$. By dividing the curves in fig. 30 (a) by ωl , the curve $L(f)$, which is shown in (b), is obtained. The data from $l = 2.0$ mm, 4.5 mm and 7.0 mm are in excellent agreement. As exemplified by the dots in fig. 30 (b), these curves will be read at fixed frequencies, and an error bar can be defined by their minimum and maximum. Likewise, from $\log(a)_{21}$ the capacitance $C(f)$, which is shown in fig. 30 (c), is obtained.

However, for $f < 400$ MHz, the measured capacitance differs from the HFSS prediction roughly by a factor of two. The following interpretation is proposed: For $f > 2$ GHz, the wafer probers approximately only couple to the differential TEM-mode, as desired. This is reinforced by the good agreement

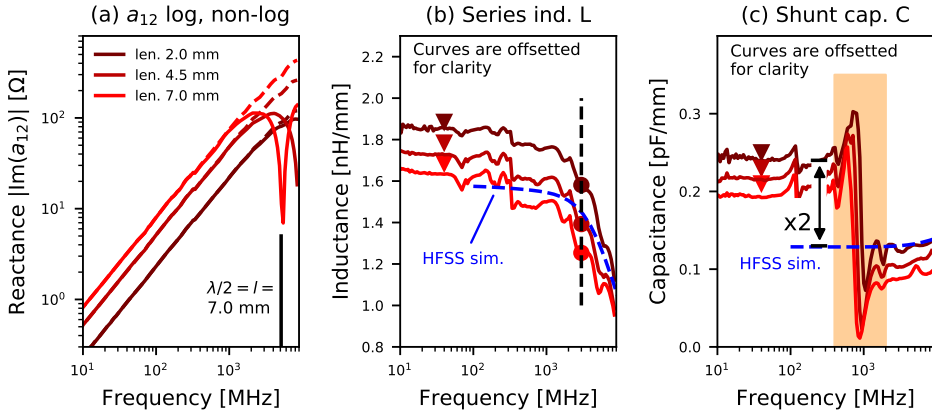


Figure 30: Visualization of the data evaluation method of the coplanar strips with distance $d = 0.385$ mm in wafer #1. The solid lines in (a) show $|\text{Im}(a_{12})|$, and the dashed lines show $\text{Im}(\log(a)_{12})$. Curves for $l = 4.5$ mm and $l = 7.0$ mm in (b) and (c) were offset for clarity, as indicated by the triangular markers. The shaded area in (c) marks the transition region $[0.4 \text{ GHz}, 2 \text{ GHz}]$ towards the differential TEM-mode.

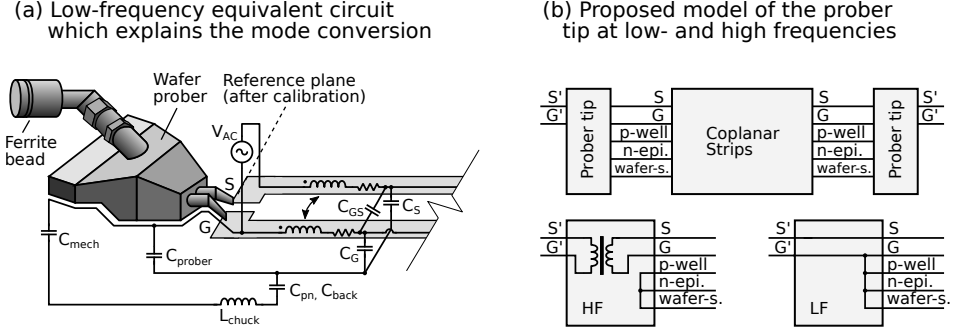


Figure 31: Part (a) shows a low-frequency equivalent circuit of the probe, wafer and the coplanar strips using partial inductances. After calibration, the AC-excitation V_{AC} is effectively located at the calibration plane. The ferrite bead is unable to blocking the “common mode” interference currents over C_{prober} and C_{mech} . Part (b) shows how a multi-mode coplanar strip transmission line model is embedded in models of the probe tips. All substrate layers (p-well, n-epi., wafer-s.) are thought to be effectively shorted at the probe tips at LF and HF, because of the wafer’s enormous total capacitance.

between HFSS-simulation and measurement for $L(f)$ and $C(f)$ for all lengths in the range $f > 2$ GHz (see fig. 30 (b), (c)). Formally, this is expressed by the HF probe tip model in fig. 31 (b), which couples the probe tips S' and G' to the pads S and G using an ideal transformer. In contrast, for $f < 400$ MHz, the coupling of the probe tips are instead represented by the LF probe tip model in fig. 31 (b). Here, the ground tip is effectively shorted to, both, the ground pad and the substrate. In the low-frequency limit, this is explained by the equivalent circuit in fig. 31 (a). The capacitance between the probe and the substrate C_{prober} was estimated to be much larger than C_G and C_S .⁷ Therefore, C_G can be neglected, and the potential of the substrate, which is given by the voltage divider between C_S and C_{prober} , is strongly tied to the ground tip. The capacitance of the differential TEM-mode is given by a series connection of C_G and C_S , whereas in the low-frequency limit, instead the capacitance C_S is measured. C_S is larger by roughly a factor of two if $C_{GS} \ll C_S$ and if $C_S = C_G$.⁸

It is well known that balanced transmission lines, such as the coplanar strips, should actually not be directly connected to an unbalanced measurement

⁷ The capacitive path over the wafer backside to the wafer chuck C_{back} and across the mechanical manipulator C_{mech} might further decrease the impedance between the ground tip and the substrate.

⁸ Further confirmation was provided by the following experiment: An unbalanced transmission line, in which the ground conductor was placed below the signal conductor, was measured as well. Here, the discussed artifacts were not observed because the signal conductor is shielded from the substrate.

equipment as it is done here [152]: An theoretical but impractical solution would be to interface the balanced transmission line with two baluns. Another solution is to perform an unbalanced 4-port measurement instead, for example by using the n-buried layer as a reference conductor. Alternatively, the coplanar strips might be discarded in favor of some balanced transmission line, in which the second power metal strip is connected to the substrate at regular intervals. However, these two solutions require additional, expensive photomasks for fine vias, contacts, n-sinkers, n-wells, diffusion and possibly deep trenches, which motivates why this was not implemented.

In the following, it is argued that the data for $L(f)$ below 400 MHz can still be interpreted as the inductance per length of the differential TEM-mode. Firstly, observe that all coplanar strips are electrically small below 400 MHz. Therefore, the E - and B -fields in cross sections at any z -coordinates are approximately equal, and one may approximate $\log(a)$ by $a - 1$. In order to predict the magnetic field lines, it must be known whether the current is returned via the power metal, or via the substrate. A simple estimation has shown that the resistance of a current return path over the substrate would be much larger than the impedance of the power metallization. Therefore, the majority of the return current flows in the power metallization. Hence, the magnetic field lines, which are shown in fig. 29 (b), are roughly equal to the magnetic field lines in the differential mode. The measured inductance per length is equal to the differential TEM-mode as well. Note that fig. 29 (b) is formally a superposition of the common and differential mode, and hence this may be termed a *mode conversion*.

This argumentation is confirmed by the observation that there is *no* discontinuity in fig. 30 (b) in the transition region [400 MHz, 2 GHz]. In fact, the visible artifacts appear smaller than 0.1 nH/mm.

4.5 Results and Discussion of the Coplanar Strips

This section discusses the measurement and simulation results of the coplanar strips defined in fig. 27 (a).

4.5.1 Distance- and Frequency-Dependence of the Inductance

Fig. 32 (a) shows the measurement results of the distance- and frequency-dependent L . The fact that all error bars in fig. 32 (a) are below 10% creates confidence in the correctness of the used data evaluation procedure. In wafer #1, the metallization below the power metal is a dense fill-pattern, whereas in

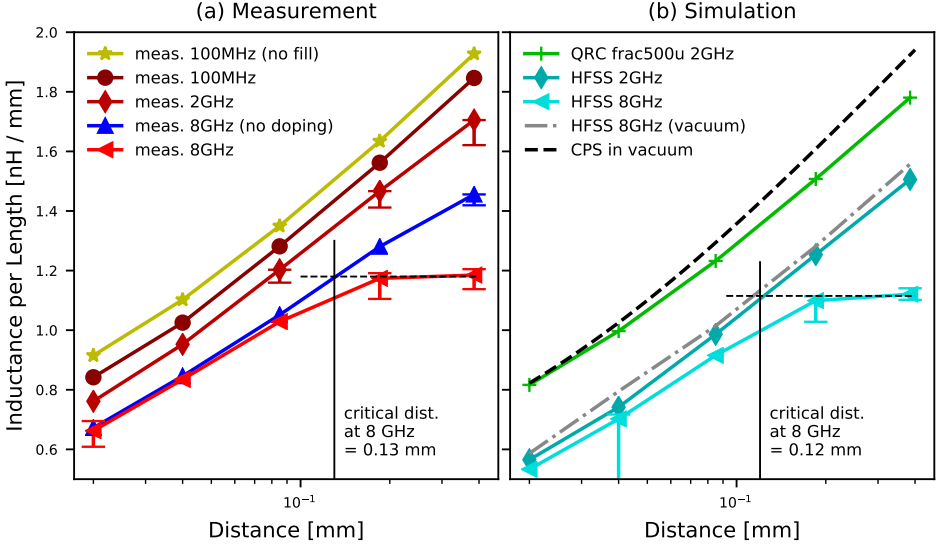


Figure 32: Inductance per length of the coplanar strips as a function of the distance. The data points show $l = 2$ mm, and the error bars are the minimum and maximum over $l = 2$ mm, 4.5 mm and 7 mm (see sec. 4.4.1). The yellow curve and the blue curve in (a) corresponds to wafer #8 and wafer #7, respectively, whereas the red curves correspond to wafer #1.

wafer #8, this fill-pattern is left out⁹. For each distance, coplanar strips of three different lengths have been measured and simulated, and the so-obtained intervals are shown as error bars. By comparing the yellow curve (wafer #8) in fig. 32 (a) to the red curve (wafer #1), it can be seen that fill-shapes have no impact on the inductance at 100 MHz. This also holds for the corresponding curves at 2 GHz and 8 GHz (this data was omitted from fig. 32 (a) for the sake of clarity). This was expected because the magnetic moment created by eddy currents which flow in these microscopic fill-shapes is very small.

In fig. 32 (a), it can be seen that above a certain *critical distance* of roughly 0.13 mm, the inductance at 8 GHz (red curve, wafer #1) saturates at roughly 1.2 nH/mm. This shows that the two power metal conductors become inductively decoupled at 8 GHz for $d > 0.13$ mm. An indication about the origin of this effect is provided by a comparison to the data from wafer #7 (blue curve): The saturation characteristic disappears if the n-epitaxial layer, the logic implant and the p-well are omitted. This leads to the hypothesis that the coplanar strips decouple into two microstrip-like transmission lines, in which

⁹ Recall that the HFSS-simulations never include the fill-pattern.

the n-buried layer carries the return current¹⁰. This will be further refined in sec. 4.5.3. To precisely characterize the critical distance, the apparent supremum (dashed black curve) is intersected with the measured inductance over the bare wafer-substrate (blue curve). Note that, in the investigated distance range, this saturation characteristic is not observed for $f \leq 2$ GHz. In fact, for $d < 0.385$ mm and $f \leq 2$ GHz, a comparison between wafer #1 and wafer #7 showed only small deviations (curves are not shown for clarity). Thus, at 2 GHz and below, the critical distance is certainly larger than 0.385 mm, but it cannot be determined precisely by the conducted experiments.

Fig. 32 (b) shows simulation results of $L(f)$. A systematic offset error of 0.2 nH/mm is observed between the HFSS-simulation at 2 GHz and the measurement data. Apart from this offset, the alignment is excellent¹¹. By comparing the HFSS simulation results for 2 GHz and 8 GHz it can be seen that these simulations predict the critical distance reasonably well (0.12 mm). This reinforces that the observed saturation is not a measurement artifact. Moreover, HFSS simulations were performed, in which all substrate layers and the intermetal dielectric (see fig. 28) were replaced by vacuum. As shown by the dashed gray curve, in this case the saturation disappeared, which further supports the hypothesis that the substrate is responsible for this effect. For $f \leq 2$ GHz, the difference between the HFSS simulations with and without substrate were very small (curves not shown for clarity). This impressively shows that for $f \leq 2$ GHz and $d \leq 0.385$ mm, the magnetic field lines are negligibly affected by the substrate. Such transmission lines, in which the B -field penetrates deeply into the substrate but the E -field does not, are also known as *metal-insulator-semiconductor (MIS) slow wave*¹² transmission lines in literature [71].

In the following, a simple closed-form expression for the inductance per length of the coplanar strips on the wafer is derived: Formulas for the characteristics of coplanar strips in vacuum are found in literature [178]:

$$v = c \quad Z_0 = 120\pi \frac{K(k')}{K(\sqrt{1-k'^2})} \quad k' := \frac{d}{d+2w} \quad (53)$$

where v is the propagation speed, c is the speed of light in vacuum, Z_0 is the characteristic impedance, K is the complete elliptic integral of the first kind,

¹⁰ The p-well and the logic implant are thought to carry only a negligible fraction of the return current because their combined sheet resistance is larger by orders of magnitude.

¹¹ The reason for this offset is speculated to be related to the erroneous mode conversion (sec. 4.4.1), or due to an insufficient mesh size.

¹² Using the capacitance and inductance data from fig. 30 at 3 GHz one obtains a wave propagation speed of only $v = 0.24 c$.

d is the distance between the coplanar strips (edge to edge) and w is their width¹³. The inductance per length is calculated using $L = Z_0/v$. Clearly, the investigated slow-wave coplanar strips are very different from coplanar strips in vacuum, but the inductance per length is the same because the magnetic field lines are equal. The inductance predicted using these formulas, which is visualized by the dashed black line in fig. 32 (b), is a reasonable agreement with measurement.

It is further observed that the data obtained from QRC-based circuit simulations at 2 GHz in fig. 32 (b), where the “frac500u” settings were used, is in good agreement with this model. This validates QRC, and shows that, if configured as specified in table 6, QRC assumes that magnetic field lines penetrate freely into the substrate. The inductance from QRC at 100 MHz and 4 GHz (not shown for clarity) almost perfectly overlapped the QRC results for 2 GHz, even at $l = 7$ mm. This impressive fact proves that RLCK extraction tools like QRC are excellently capable of describing the wave propagation of this differential TEM-mode. It was observed that, with the “frac50u”-settings (a mode where the resulting netlist size is much increased!) the precision of $L(f)$ was very similar (data not shown for clarity). This is in line with the understanding that a fracturing size of $\lambda/20$ is by far sufficient for transmission lines.

When increasing the frequency, the measured inductance decreases significantly, as can be seen in the red curves in fig. 32 (a). For distances below 0.1 mm, the difference of the inductance between 100 MHz and 8 GHz is between 0.2 nH/mm and 0.3 nH/mm. It is well known that the inductance of a cylindrical wire differs by $\mu_0/(8\pi) = 0.05$ nH/mm between DC and the high-frequency limit due to the skin effect [76], [92]. This raises the question whether the observed decrease in $L(f)$ for $d < 0.1$ mm might be fully explained by the vanishing of the metal strips’ internal inductances. As demonstrated in [76], the internal inductance of wire with a rectangular cross section and a ratio of $t/w = 0.3$ is only $L_{\text{int.}} \approx 0.035$ nH/mm. Since the predicted change in the inductance of coplanar strips of $2L_{\text{int.}} \approx 0.070$ nH/mm is much smaller than the decrease observed in measurement, it is concluded that this is *not* a feasible explanation. In HFSS simulations, for distances below 0.1 mm, the alignment between the inductance at 100 MHz (not shown) and 8 GHz was much better. It might be that the decrease in measurement might be merely an artifact due to the mode conversion issues explained in sec. 4.4.1.

¹³ This model is based on the simplifying assumption of an infinitesimal conductor thickness.

4.5.2 Eddy Current Losses in the Substrate

Fig. 33 (a) shows the equivalent series resistance R , calculated according to $\text{Re}(\log(a)_{12})/l$, as a function of frequency for $d = 0.385$ mm. Alternatively, the series losses can be expressed as the *series loss tangent* $\tan \delta_{\text{series}}$:¹⁴

$$\tan \delta_{\text{series}} = \frac{R}{\omega L} \quad (54)$$

The series loss tangent is plotted in fig. 33 (b) as a function of the distance for $f = 4$ GHz. In resonances formed from metal interconnect and on-chip capacitors, $1/\tan \delta_{\text{series}}$ is an upper bound on the quality factor.

The main difficulty in calculating R or $\tan \delta_{\text{series}}$ from network parameters is the fact that R is typically much smaller than the series reactance $\text{Im}(\log(a)_{12})/l$, which is depicted by the black curve: Since even small phase errors in $\log(a)_{12}$ can add a large error to R , it must be carefully worked out

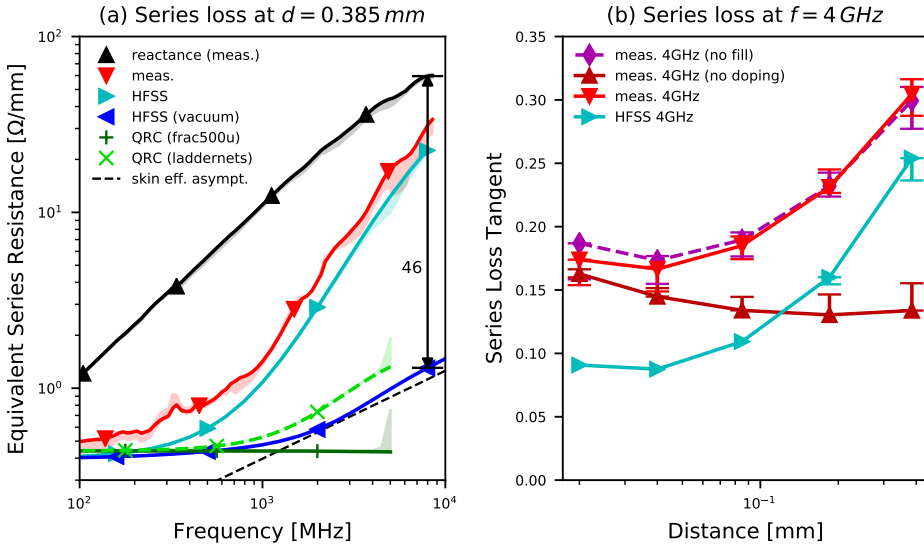


Figure 33: Series losses of the coplanar strips as (a) the equivalent series resistance per length for a fixed distance or (b) the series loss tangent for a fixed frequency. The data points show $l = 2$ mm. The shaded areas in (a) and the error bars in (b) show the minimum and maximum over $l = 2$ mm, 4.5 mm and 7 mm (see sec. 4.4.1). The magenta, brown and red curves in (b) correspond to wafer #8, wafer #7 and wafer #1, respectively.

¹⁴ This term has been chosen merely as an analogy: Note that this is unrelated to the loss angle of the intermetal dielectric [178], which is instead a part to the *shunt* loss tangent $\tan \delta_{\text{shunt}} := 1/(G\omega C)$.

whether the measured R may be interpreted as series losses. The blue curve¹⁵ in fig. 33 (a) summarizes the result from the HFSS simulations, in which the substrate and the intermetal dielectric were replaced by vacuum. Here, the only series losses should be due to the skin effect, and, in fact, the blue curve is in good agreement with a theory prediction of the skin effect losses (black, dashed curve). Observe that, in these HFSS-simulations without substrate, at 8 GHz, R is roughly by a factor of 46 smaller than the reactance ωL . This demonstrates that the used data evaluation methodology as such, i.e. the de-embedding and application of the matrix logarithm to the ABCD-parameters, is capable of quantifying δ_{series} with an error $\ll 1^\circ$.

In fig. 33 (a), it can be seen that, when the substrate is added to the HFSS simulation (cyan curve), R increases markedly. This already suggests that the cyan curve reflects eddy-current losses in the substrate (see sec. 4.4). This will be proven subsequently by a direct computation of the TEM modal solution using FEM-analysis in sec. 4.5.3. Observe that the measurement data in fig. 33 (a) (red curve) is in reasonably good agreement with the HFSS simulation. This suggests that, for $d = 0.385$ mm, the measured phase in $\log(a)_{12}$ can indeed be interpreted as δ_{series} , and it is *not* dominated by phase errors. However, by comparing the red and the cyan curve in fig. 33 (b), it is observed that the agreement with simulation is not good for all distances at 4 GHz. It appears that the measured $\tan \delta_{\text{series}}$ is shifted by about $+0.05$ to $+0.08$, or alternatively, δ_{series} is shifted by $+3^\circ$ to $+5^\circ$. The origin of this phase offset, which was highly reproducible, also across different wafers, could not yet be conclusively explained. It might be a systematic bias due to the erroneous mode conversion (sec. 4.4.1), or it might be a dissipative effect that is not present in the HFSS model, and which is not yet understood.

By comparing the measurement data between wafer #1 (red curve) and wafer #7 (brown curve) in fig. 33 (b), it is revealed that the n-buried layer is a major contributor to the eddy current losses at 4 GHz¹⁶. This is in line with the understanding of the saturation of the inductance that was developed in sec. 4.5.1: At high frequencies, adding the n-buried layer leads to strong eddy currents: On the one hand, these eddy currents are responsible for increased losses. On the other hand, they can alternatively be understood as return currents of two microstrip-alike transmission lines, which leads to their magnetic decoupling. This is further clarified in sec. 4.5.3. Moreover note that the measurement data in fig. 33 (b) from wafer #8 (dashed, magenta

¹⁵ The coincidence of curves for $l = 2$ mm and 4 mm were found to overlap almost perfectly.

¹⁶ It is clear that the contribution from the p-well and the logic implant is comparably small because their combined sheet resistance is larger by orders of magnitude.

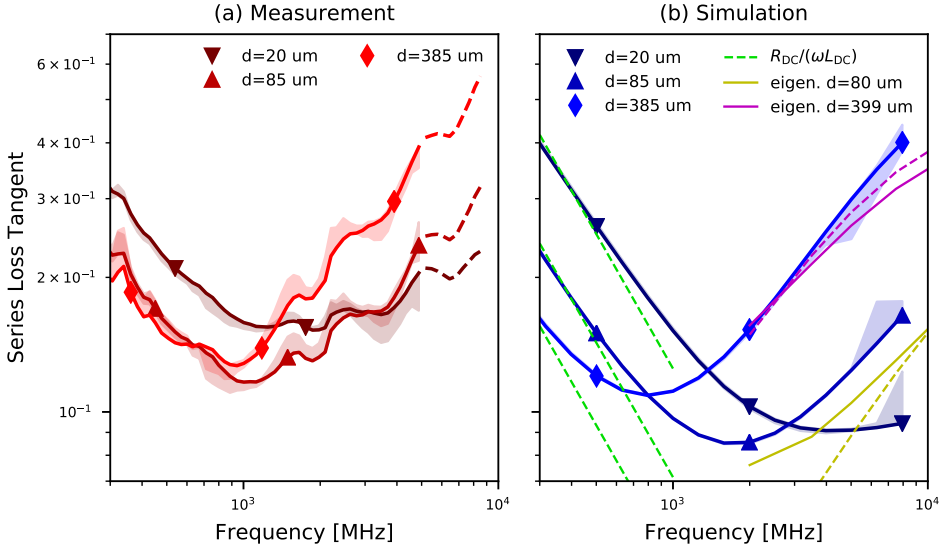


Figure 34: Series loss tangent $\tan \delta_{\text{series}}$ of the coplanar strips. Part (a) shows data from measurements of wafer #1. The blue curves in (b) were obtained from the HFSS-simulations including the substrate. The red and blue curves correspond $l = 2 \text{ mm}$. The shaded areas show the minimum and maximum over $l = 2 \text{ mm}$, 4.5 mm and 7 mm (see sec. 4.4.1).

curve) is well aligned with the data from wafer #1 (red curve). This shows that the presence of metal fill-shapes does *not* affect the series loss tangent.

In fig. 33 (a), it can be seen that the results of QRC-based circuit simulations exhibit a frequency-independent R equal to the DC resistance if the “wide_band_model” is disabled. With the “laddernets” settings (see table 6), depicted by the light green curve, heuristic skin effect models [92] correctly describe the skin effect losses, but the more important eddy current losses are still not accounted for. QRC features a mode in which also eddy current losses are introduced, but, according to the documentation, this is mutually exclusive with the extraction of inductive couplings. However, this mode was not investigated in this thesis.

Fig. 34 summarizes this section’s results of the series losses in the coplanar strips. This figure provides sufficient information to estimate $\tan \delta_{\text{series}}$ over a wide range of distances and frequencies. The low-frequency asymptote is given by $R_{DC}/(\omega L_{DC})$ – this is shown by the green dashed lines in fig. 34 (b). The dashed yellow and magenta curves in fig. 34 (b) show the part of the series loss tangent that corresponds to eddy-current losses in the n-buried layer. Details on how this was computed using the FEM-eigenanalysis are found in sec. 4.5.3. This coincides with the high-frequency asymptote of the blue

curves in fig. 34 (b), which represent $\tan \delta_{\text{series}}$ obtained from the 3D HFSS-simulations. The minima in fig. 34 (b) arise at the frequency where these low- and high-frequency asymptotes join. The dashed, red lines in fig. 34 (a) show the measurement data for $l = 2$ mm beyond 5 GHz. In this frequency range, the error bars were typically $> 50\%$ (not shown for clarity), and thus, this data should be used with caution. Moreover, the data for $d = 20$ μm above 1 GHz in fig. 34 (a) might overestimate the actual losses by factor of 2, due to the phase offset discussed above. The ripple in the measurement data might be due to a calibration drift. This illustrates that quantifying these very small series losses beyond 1 GHz stretches the used measurement setup to the limit.

4.5.3 FEM-Eigenanalysis – Eddy Currents in the n-Buried Layer

The 3D EM-field simulations (sec. 4.3), the results of which were discussed previously, replicate the measurement environment in many aspects. This is both a strength and a weakness: For example, on the one hand, the fact that metal-pads are excited using lumped ports allowed to evaluate the precision of the used data evaluation methodology, as shown in sec. 4.5.2. On the other hand, the necessity to apply de-embedding to these 3D simulation results hampers the accessibility of higher frequencies and larger distances. Moreover, the 3D simulations are not well suited to investigate the EM-field of the theorized differential TEM-mode, and to separate the different RF-loss effects.

Therefore, another kind of field simulation, which directly computes the modal solution of the coplanar strips above the substrate, was set up. More specifically, the source-free solutions of Maxwell's equations in an infinite cylindrical structure [182] are solved using the FEM. This is an eigenvector problem on a 2D mesh, and thus the term *FEM-eigenanalysis* will be used in the following. As numerical engine, the “DrivenModal”-analysis of HFSS [82] was employed. It is applied to a thin slab of the analyzed coplanar strips, where wave ports are created at its front and back surfaces. The wave ports must be considerably larger than the distance between the metal traces in both x- and y-direction, in order to reduce boundary effects. This thin slab is equivalent to a cross-section of the 3D model (sec. 4.3), and thus, these 2D simulations describe the substrate with the same level of detail. The eigenvector problem yields an infinite number of modal solutions, of which only the two solutions with the lowest eigenvalues correspond to the TEM-modes of interest. However, because the differential and the common TEM-mode are almost degenerate at large distances, for numerical reasons, it was also necessary to enforce a perfect-E symmetry boundary condition [82] at the

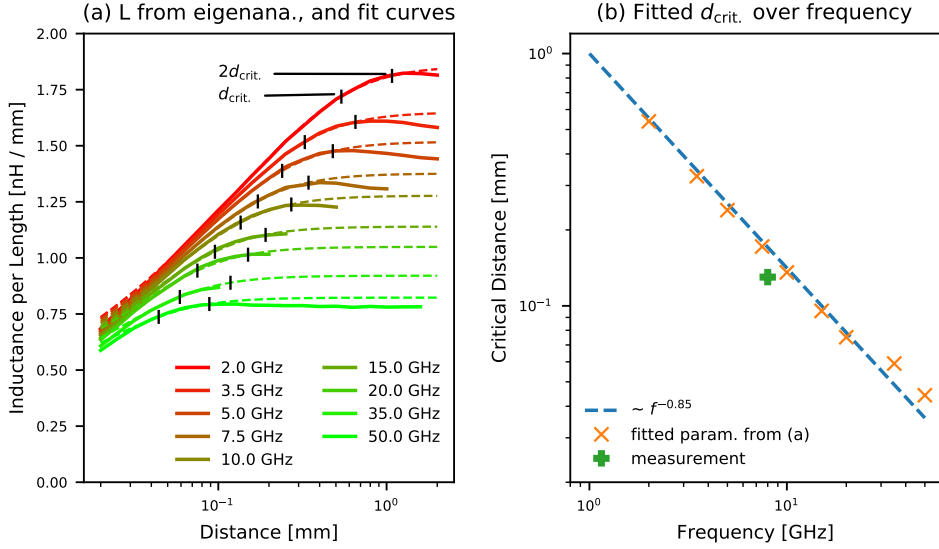


Figure 35: Part (a): The inductance per length of the coplanar strips for frequencies up to 50 GHz. The solid curves shows the result from the FEM-eigenanalysis, whereas the dashed curves are the fitted empirical functions. Part (b): The so-obtained frequency-dependent $d_{\text{crit.}}$ is roughly proportional to $f^{-0.85}$.

symmetry plane. This eliminates the common mode but retains the differential mode.

From the resulting eigenvalues and -vectors, HFSS directly computes the complex-valued propagation constant γ as well as the complex-valued characteristic impedance Z_0 . To compute Z_0 , the Z_{pv} -convention [82] was used with an integration path from the power metal conductor towards the symmetry plane.¹⁷ Using elementary transmission-line theory [182] it can be derived that:

$$R + i\omega L = \gamma Z_0 \quad G + i\omega C = \gamma / Z_0 \quad (55)$$

The solid curves in fig. 35 (a) show the so-obtained curves $L(d)$ for various frequencies. These curves appear clipped because, at some frequencies, for $d \gtrsim 3d_{\text{crit.}}$, the FEM-eigenanalysis did not converge properly. In order to compute $d_{\text{crit.}}$ as a function of the frequency, each curve was fitted to an empirical function. This is constructed by substituting $d \rightarrow d / \sqrt{1 + (d/d_{\text{crit.}})^2}$ into eq. (53). Thereby, the limit under $d \rightarrow \infty$ of the empirical inductance function equals the inductance in vacuum at $d = d_{\text{crit.}}$, which coincides with the

¹⁷ The presence of a perfect-E symmetry plane requires that the impedance multiplier option in HFSS is set to 2 [82].

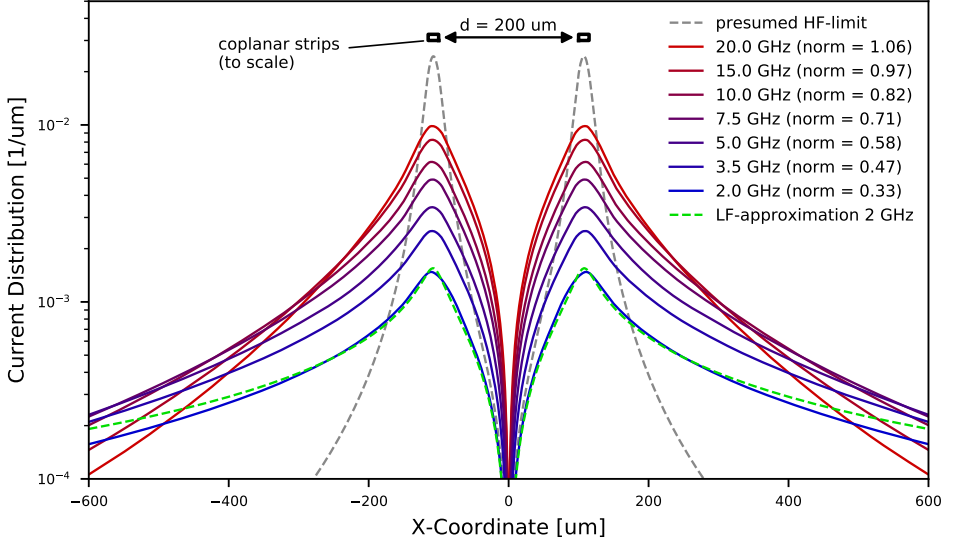


Figure 36: The absolute value of the current distribution in the n-buried layer $|D_{I,n-b.}(x)|$ underneath coplanar strips centered at $x = \pm(d/2 + w/2)$. The red/magenta/blues curves represent the differential TEM-mode computed using FEM-eigenanalysis. The dashed gray and green curves visualize eq. (58) and eq. (59), respectively.

definition of $d_{\text{crit.}}$ introduced in sec. 4.5.1. In addition, the curve is uniformly scaled by another empirical fit-parameter $C_{L,\text{fac.}}$. The empirical function then reads:

$$L = C_{L,\text{fac.}} \frac{120\pi K(k')}{c K(\sqrt{1-k'^2})} \quad k' := \frac{1}{1 + 2w\sqrt{d^{-2} + d_{\text{crit.}}^{-2}}} \quad (56)$$

The dashed curves in fig. 35 (a) show the fitted curves. Note that they were only fitted in a range up to roughly $2d_{\text{crit.}}$ (solid black bars in fig. 35 (a)). Beyond $2.5d_{\text{crit.}}$, the computed $L(d)$ even slightly decreases – an effect that is not captured by the empirical functions. The orange crosses in fig. 35 (b) show the fitted $d_{\text{crit.}}$ as a function of the frequency. As shown by the dashed blue line, $d_{\text{crit.}}$ is approximately proportional to $f^{-0.85}$. This data is in good agreement with $d_{\text{crit.}}$ obtained from measurement (sec. 4.5.1), which is shown by the green plus.

In order to further clarify the involvement of the n-buried layer, the current density field $J(x, z)$ of the forwards-propagating differential TEM-mode was exported. Subsequently, $J(x, z)$ was integrated over a z-span $[z_0, z_1]$, which ranges from the p-n-junction below to the p-n-junction above the n-epitaxial

layer. The result $\hat{f}(x)$ is then normalized to the total current that flows in y -direction in each power metal strip. This yields the current distribution of the n-buried layer, which will be termed $D_{I,n-b.}(x)$.¹⁸ The “norm” of this distribution is defined as follows:

$$N_{I,n-b.} = \left| \int_0^\infty dx D_{I,n-b.}(x) \right| \quad (57)$$

This formula applies in a coordinate-system where the two power metal strips are symmetrically centered at $x = \pm(d/2 + w/2)$. The norm $N_{I,n-b.}$ is equal to 1 if and only if the current in each power metal strip is completely returned in the n-buried layer. Fig. 36 visualizes the magnitude of the current distribution $|D_{I,n-b.}(x)|$ for a distance of $d = 200 \text{ } \mu\text{m}$. The legend of fig. 36 also states the norm $N_{I,n-b.}$ for each depicted frequency. Note that, in the FEM-eigenanalysis, $200 \text{ } \mu\text{m}$ equals the critical distance at roughly 7 GHz (see fig. 35 (b)). Thus, $f_{\text{crit.}} = 7 \text{ GHz}$ is termed the *critical frequency* at $200 \text{ } \mu\text{m}$. Fig. 36 reveals that, below $f_{\text{crit.}}$, the total current in the n-buried layer is significantly less than the current flowing in the metallization. Moreover here, the shape of the distribution is largely frequency-independent. In contrast, above $f_{\text{crit.}}$, the norm $N_{I,n-b.}$ approaches 1, while simultaneously the current distribution becomes increasingly concentrated beneath the power metal strips.

An analytic solution of the current distribution in the ground plane below a microstrip-line can be found in literature [75]¹⁹. Using the superposition principle, this is easily generalized to the differential mode of two weakly coupled microstrip lines centered at $x = \pm(d/2 + w/2)$:

$$D_{I,c.-ms.}(x) = \frac{1}{w\pi} \left(-\tan^{-1} \frac{+2x-d}{2h} + \tan^{-1} \frac{+2x-d-2w}{2h} + \tan^{-1} \frac{-2x-d}{2h} - \tan^{-1} \frac{-2x-d-2w}{2h} \right) \quad (58)$$

where w is the strip width, h is the height over the ground plane. In the following, h will be equated with the height of the power metallization over the dopant maximum in the n-buried layer, i.e. d_{nb} from fig. 27 (b). The dashed gray curve in fig. 36 visualizes eq. (58), which is presumably the HF-limit. However, at 20 GHz, the current distribution at $d = 200 \text{ } \mu\text{m}$ obtained from the FEM-eigenanalysis is still far less concentrated than the dashed curve. This shows that, even at $d = 2.7d_{\text{crit.}}$, the coplanar strips *cannot* be

¹⁸ Note that $D_{I,n-b.}(x)$ is complex-valued. The complex argument encodes the current's phase in the n-buried layer relative to the current in the metal strips.

¹⁹ In this analytic solution, the current in the metal strip is assumed to be homogeneous, and its height is zero. Moreover, the metal strip and the ground plane are perfect conductors.

described as two coupled microstrip-lines, with the n-buried layer being a ground plane. Rather, the n-buried layer acts as a very poor ground plane that is still penetrated by the magnetic field in the immediate surrounding of the metal strips. Nevertheless, the n-buried layer almost completely carries the return current and thereby magnetically shields the two metal strips *from each other*. This justifies the introduction of the term *microstrip-alike* transmission lines in sec. 4.5.1.

For $d \ll d_{\text{crit}}$, the n-buried layer can be assumed to have a negligible impact on the magnetic field, and it carries only weak eddy currents. By superimposing the well-known two solutions of the magnetic vector potential for an infinite thin wire, an LF-approximation for $\vec{A}$ can be obtained. Then, using $\vec{E} = -i\omega\vec{A}$ and $\hat{J}(x) = R_{\text{nepi}}^{-1}\vec{E} \cdot \vec{e}_z$, the following formula is obtained for $D_{\text{I,n-b.}}(x) = \hat{J}/I$:

$$D_{\text{I,n-b.}}(x) = 1.5 \frac{i\omega\mu_0}{4\pi R_{\text{nepi}}^{-1}} \log \frac{(x + d/2 + w/2)^2 + h^2}{(x - d/2 - w/2)^2 + h^2} \quad (59)$$

The additional factor of 1.5 in eq. (59) is an empirical correction to improve the agreement with the FEM-eigenanalysis result. The green dashed curve in fig. 36 visualizes the weak eddy currents from eq. (59) at $f = 2 \text{ GHz}$. It is approximates the current distribution from the FEM-eigenanalysis very well.

An approximate closed-form solution of the eigenvector problem that is valid both below and above f_{crit} , would be desirable. This solution would generalize eq. (59) and eq. (58), and it would allow to derive a non-empirical formula for $L(d, f)$ as well as $d_{\text{crit}}(f)$. An analytic solution might be constructed by solving the diffusion equation of the vector potential in a multi-layered substrate, e.g. using complex image theory [155]. For example, Weisshaar et al. use complex image theory to compute closed-form expressions for R , L , G and C over a homogeneous wafer-substrate [194]. However, a closed-form expression readily applicable to the discussed coplanar strips over the n-buried layer could not be found in literature.

It is easily shown that the power dissipated in the n-buried layer $P_{\text{I,n-b.}}$ per length l can be computed from the current distribution $D_{\text{I,n-b.}}(x)$ as follows:

$$\frac{P_{\text{I,n-b.}}}{l} = I_{\text{RMS}}^2 R_{\text{eff.,n-b.}} \quad R_{\text{eff.,n-b.}} := R_{\text{nepi}} \int_{-\infty}^{\infty} dx |D_{\text{I,n-b.}}(x)|^2 \quad (60)$$

where I_{RMS} is the RMS-current in the power metal strips. Therefore, the part of the loss-tangent caused by eddy-currents in the n-buried layer equals $R_{\text{eff.,n-b.}} / \text{Im}(\gamma Z_0)$, and this formula is evaluated using $D_{\text{I,n-b.}}(x)$, γ and Z_0 from the FEM-eigenanalysis. This was depicted by the *dashed* yellow and magenta curves in fig. 34 (b). Note that, by inserting the approximate

eq. (59) into eq. (60), it is derived that, below the critical distance, this contribution to $\tan \delta_{\text{series}}$ is roughly proportional to the frequency. The solid yellow and magenta lines in fig. 34 (b) show the complete series loss tangent $\text{Re}(\gamma Z_0) / \text{Im}(\gamma Z_0)$, which also includes the DC resistance of the power metallization. The good agreement with the blue curves again confirms the correctness of this data.

4.5.4 Eddy Current Losses in the Metallization

It is clear that eddy currents can also occur in the metallization if the structuring allows them to flow unhindered. So far, this has not yet been addressed. An extreme case²⁰ is a continuous metal-4 plate beneath the coplanar strips. Measurements and simulations were performed on coplanar strips above a continuous floating metal plate with the minimum distance of $d = 20 \mu\text{m}$. In one case, the metal plate was located in metal-4, as shown in fig. 27 (c),

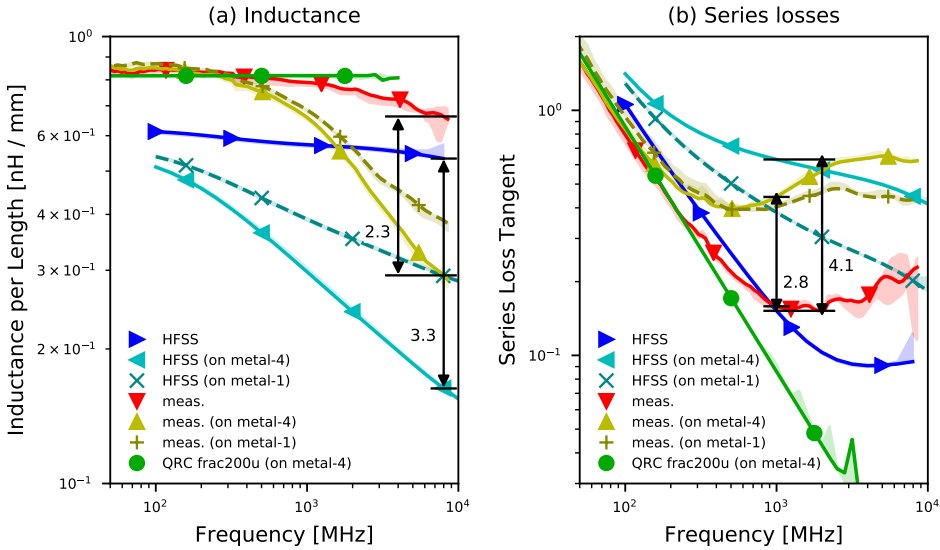


Figure 37: Impact of a metallic background (continuous, floating metal-1 or metal-4 plate, see fig. 27 (c)) on the physics of the coplanar strips with distance $d = 20 \mu\text{m}$. The measurement data was obtained from wafer #1 and from another wafer that has been processed essentially identically. The data points show $l = 2 \text{ mm}$. The shaded areas show the minimum and maximum over $l = 2 \text{ mm}$, 4.5 mm and 7 mm (see sec. 4.4.1).

²⁰ The worst case deviation of the inductance in the high-frequency limit would be attained for a completely filled metal stack. Other criteria, e.g. an extremal loss tangents at a certain frequency, lead to a different worst case – for example, a single metal plane with a matched sheet resistance.

and in the other case, the metal plate was located in the bottom-most metal layer, i.e. metal-1. The blue and red curves in fig. 37 (a) correspond to coplanar strips *without* a metal plate in simulation and measurement, respectively²¹. By comparing the red to the yellow curve in fig. 37 (a) it is found that, at 8 GHz, the presence of a metal-4 plate can reduce the inductance roughly by a factor of 2.3. Conversely, the HFSS simulations predict a decrease by a factor of 3.3. This prediction is sufficiently accurate. The measurement data in fig. 37 (b) shows that, already at 1 GHz, eddy currents in the metal-4 plate increase the series losses by a factor of 2.8. Conversely, the HFSS simulations predict an increase by a factor of 4.1 at 1 GHz. The reason for the discrepancies between measurement and HFSS simulations is probably that the conducted simulations neglect cheese-shapes, and thus underestimate the sheet resistance in metal-4. This might be improved by using an effective, increased resistivity.

The green curves in fig. 37 show that QRC is unable²² to describe to eddy currents in a continuous metal plate. This is consistent with the hypothesis that QRC's RLCK-extraction algorithm is similar to eq. (19). However, it is very important to understand that the inability to predict these eddy currents is merely due to the fact that the metal plate is two-dimensional. Instead, as will be shown in sec. 4.6, *eddy currents in line-like metal segments can be excellently predicted* by QRC or by other tools based on eq. (19). In purely digital ICs, the power distribution network typically does *not* feature extended ground-planes [92], but in Automotive System ICs, extended metal plates may occur. A simple workaround to simulate the eddy-currents in such metal plates is proposed: For simulation, the continuous metal plate should be slotted in a way that it breaks apart into eddy-current carrying line-like segments and a floating cutoff piece.

4.6 Results and Discussion of the Loops and Inductors

The coplanar strips discussed in sec. 4.5 are 2D structures, in the sense that they can be described by 2D field equations – see also fig. 29. Albeit coplanar strips are suitable for high-precision tests, they are blind to issues that only occur in true 3D structures, where currents flow in both x- and y-direction. This section compares the simulation- to the measurement-results of the simple loops, the spiral inductors and the folded, nested loops from fig. 27 (a).

²¹ The discrepancies between these curves, which represent simulation and measurement, respectively, were already discussed above.

²² It was double-checked that the resulting netlist contains mutual inductances between the power metal and the fractured metal plate below. This requires special settings because the metal plate is not connected.

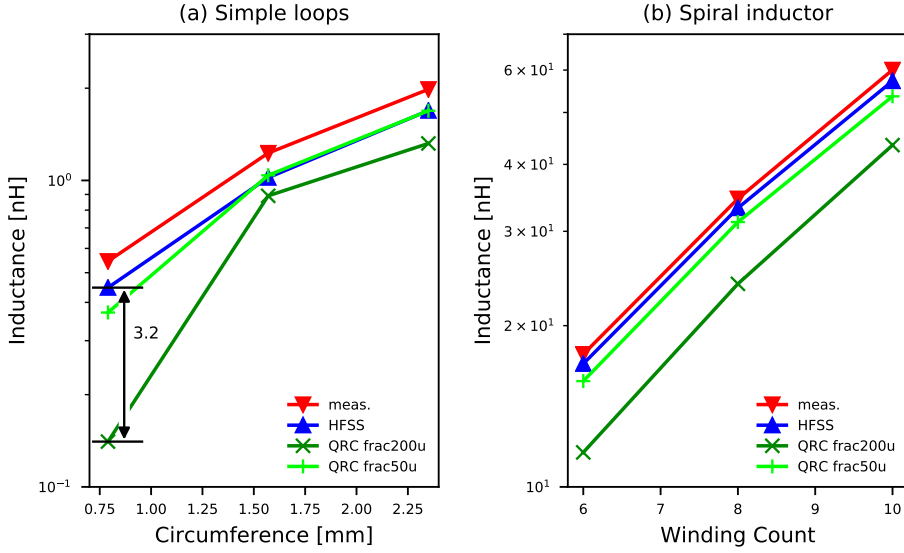


Figure 38: The inductance, defined as the imaginary part of the 1-port Z-parameters at 100 MHz, of (a) the simple loops and (b) spiral inductors in simulation and measurement (wafer #1). The circumference in (a) corresponds to $2d_x + 2d_y$ in fig. 27 (a).

Here, de-embedding and other additional post-processing was *not* performed – rather, the depicted data is directly computed from raw S-parameter datasets.

Fig. 38 summarizes the results of the simple loops and the spiral inductors, which are defined in fig. 27 (a). For very small fracture sizes of only 50 μm , the QRC-based prediction aligns almost perfectly with the HFSS-simulations. However, remarkably, the QRC-based prediction in fig. 38 (a) with a fracture size of 200 μm is off by a factor of up to 3.2, despite this fracture size is smaller than $\lambda/20$. Based on similar observations, some QRC users have speculated in the past that a criterion for the fracture size based solely on the wavelength is not sufficient. However, this is in contradiction to the results of coplanar strips (sec. 4.5.1). It is also in contradiction to the theoretical understanding in sec. 2.6.1 and sec. 2.5.2: The accuracy of the computed inductances should be *independent* of the fracture size, as should be the accuracy of the capacitances. It has meanwhile been clarified that this deviation is due to the fact that the used version of QRC simply cannot handle angled segments properly. Decreasing the fracture size reduces the size of the angled fractures, and hence this error is decreased. A proper workaround was provided but not yet thoroughly tested. It is important to understand that the only applicable solution for this issue is this *proper workaround*, whereas strongly decreasing the fracture size is *extremely expensive* and must not be recommended: This is

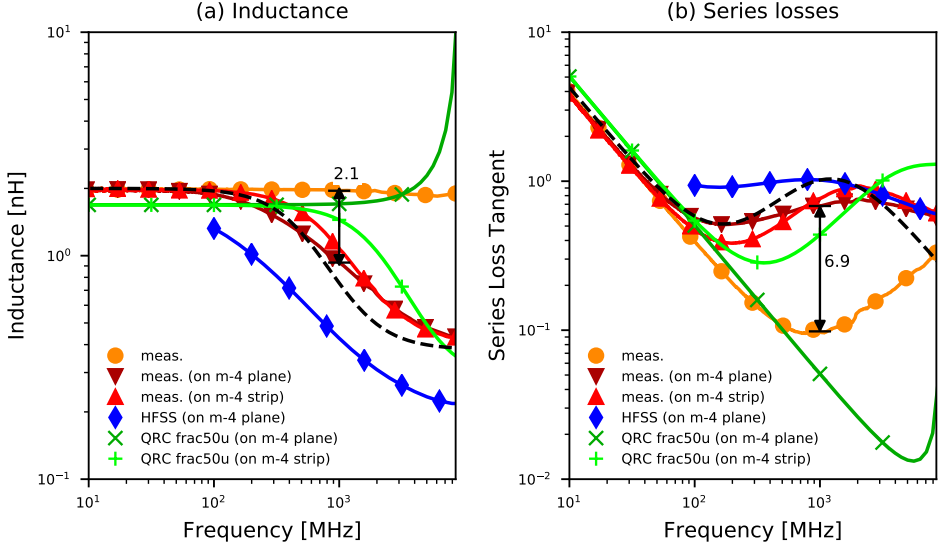


Figure 39: Impact of a metallic background on the behavior of the simple loops defined in fig. 27 (a) on wafer #1. The circumference is $2d_x + 2d_y = 2.41$ mm. In the brown, blue and dark green curves, a continuous, floating metal-4 plate that covers the complete loop area and the pads was present. Conversely, in the red and light green curves, a closed, ring-shaped, floating metal-4 strip lies below the power metal trace. (see fig. 27 (c)) The dashed black curve corresponds to the circuit model from fig. 40.

because, if RLCK-extraction is used, the linear solver run time asymptotically grows with the *third power* in the fracture count²³. For example, if the partial inductances pose a bottleneck to the linear solver, decreasing the fracture from 500 μm to 50 μm would increase the simulation run time, e.g., from one day to almost three years.

When a continuous metal-4 plate is added, at 1 GHz, the inductance of a loop of circumference 2.41 mm is reduced by a factor of 2.1, and the series loss tangent is 6.9-fold increased. This is shown by the measurement data (dark red and orange curves) in fig. 39 (a) and (b). This effect, which is a consequence of the eddy currents in the metallization (see sec. 4.5.4), is correctly predicted by the HFSS-simulation (blue curve)²⁴. Now suppose a

²³ The partial inductance matrix is necessarily dense (see sec. 2.6.1), and dense Gaussian elimination has an asymptotic run time of $\mathcal{O}(N^3)$.

²⁴ The small deviations are probably due to the neglect of cheese-shapes, which introduces an error to the sheet resistance – see sec. 4.5.4.

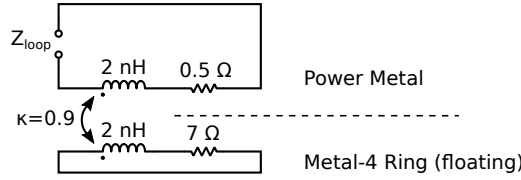


Figure 40: Circuit model of the simple loop with circumference $2d_x + 2d_y = 2.41$ mm above a ring-shaped metal-4 strip. The resistances were computed from the geometry of the metal strips. The inductances and their coupling coefficient were obtained from low- and high-frequency asymptotes of the light red curve in fig. 39 (a).

hole is cut out in the middle of the metal-4 plate, such that only a closed²⁵ ring-shaped strip beneath the power metal trace remains (see fig. 27 (c)). This results in the light red curve. By comparing the light red to the dark red curves fig. 39 (a) and (b), it can be seen that this hole *only minimally* affects the inductance and the series loss tangent. This is explained by the presumption that, in the frequency range where eddy currents have a significant impact, they are necessarily sharply concentrated underneath the power metal trace. This insight is used to construct a very simple circuit model of the simple loops above a metal-4 plate or strip (fig. 40). The dashed black curves in fig. 39 (a) and (b) are obtained from the impedance seen at Z_{loop} in fig. 40. Recall that eq. (19) cannot properly treat two-dimensional conductors (see sec. 2.6.1). Thus, for RLCK-extraction tools based on this equation, one should expect an *incorrect prediction* of the eddy currents for the metal-4 plate but a *good prediction* for the metal-4 strip. This is exactly consistent with the behavior of QRC, as shown by the green curves in fig. 39.

Fig. 41 shows the impedance of a spiral inductor up to 8.5 GHz. The HFSS-simulation is in excellent agreement with the measurement. Above 2 GHz, the response of the QRC-based circuit model appears slightly frequency-shifted by a factor of about 1.3. This might be due to small errors in the extracted capacitances. Moreover, the resonances are more sharp, which is probably related to the neglect of eddy current losses in the substrate. This data indicates that the assembly of the capacitance and the partial inductance matrix into a composite circuit model by tools like QRC works sufficiently well.

The folded, nested loops in fig. 27 (a) test the induction caused by differential AC currents: Since currents in the two outer loops are of the same magnitude but of opposite direction, their magnetic fields almost cancel out. Hence, the small voltage induced in the inner pickup loop is only correctly

²⁵ The metal-4 strip would not be connected to itself at the pads, the measurement, HFSS-simulation and QRC-simulation data would not show any eddy current losses. This should be clear to the reader.

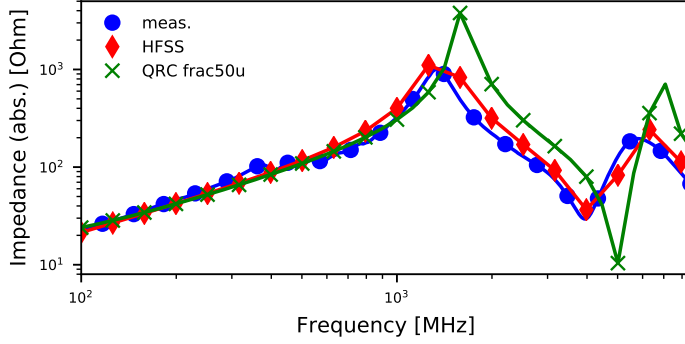


Figure 41: Absolute value of the 1-port Z-parameters of the spiral inductor defined in fig. 27 (a) with 8 windings in simulation and measurement (wafer #1).

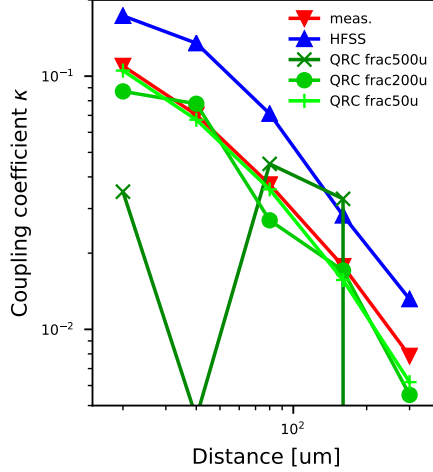


Figure 42: The inductive coupling coefficient κ in the folded, nested loops defined in fig. 27 (a). From two-port measurement- or simulation data at 100 MHz, κ was computed as $-\text{Im}(Z_{21}) / \sqrt{\text{Im}(Z_{11}) \text{Im}(Z_{22})}$.

predicted by RLCK extraction if the mutual partial inductances are matched sufficiently well (see also sec. 3.3.1). By comparing the light green curve to the red curve in fig. 42, it is observed that QRC achieves correct predictions even for κ below 1%. However, as shown by the dark green curve, this ability diminishes for larger fracture size, which is likely due to the inability to handle angled segments, as described above. Whether the provided workaround is suitable for these test structures as well is still under investigation.

4.7 Conclusions and Outlook

The presented analysis of the coplanar strips have improved the understanding of the high-frequency physics of the power and ground network in Automotive System ICs. It was shown experimentally that the coplanar strips form a MIS slow wave transmission line, in which, below a critical distance $d_{\text{crit.}}$, the magnetic field lines penetrate freely into the substrate. Conversely, above the critical distance, strong eddy currents arise in the n-buried layer, which decouple the two metal strips magnetically. This effect might be relevant for the pre-silicon analysis of the RF-immunity beyond 1 GHz, assuming that inductive couplings between the power network and sensitive analog signals is a limiting factor. At 8 GHz, the critical distance in measurement was 0.13 mm, and an extrapolation of simulation data has shown that $d_{\text{crit.}}$ at 1 GHz is roughly 1 mm. The FEM-eigenanalysis has shown that the critical distance is roughly proportional to $f^{-0.85}$.

Series losses due to eddy currents in the metallization can significantly dampen resonances in the power distribution network. If power and ground are routed over the same, continuous metal-4 plate, the series loss tangent is greater than 0.4 for the complete frequency range from DC to 8.5 GHz, and probably beyond ²⁶. This already rules out resonances with a quality factor greater than 2.5, while not introducing any low frequency losses. For example, assume the IC-internal voltage regulator from sec. 4.1, and assume that it supplies the analog module via coplanar strips of $l = 1.5$ mm and $d = 0.385$ mm. Using technology data it could be estimated that the ESR of the module's 10 pF capacitance might be 5 Ω or lower. If no additional losses are present, the resonance is rather sharp with a quality factor of 3.2, but the addition of a continuous metal-4 plate would reduce the quality factor to about 1.3. It was demonstrated that a continuous plane is not necessary, but rather a circular, unconnected strip ²⁷ is sufficient as well. This strip mediates between the power and the ground trace, and the routing of the power and ground does not have to be altered. With the aid of simple circuit diagrams, e.g. fig. 40, the dimensions of this circular strip can be engineered such that the loss tangent is roughly 1 at the resonance frequency, whereby the resonance is damped to a Q-factor less than one ²⁸.

²⁶ Strictly speaking this was only shown for $d = 20$ μm , but this property is thought to apply for larger distances as well.

²⁷ It should not be floating but rather it should be connected to ground. It is important to connect it at most at a single point!

²⁸ For example, according to the measurement data in fig. 39, the loop above a metal-4 strip achieves about $\tan \delta_{\text{series}} \approx 0.9$ at 2 GHz. For a resonance frequency different than 2 GHz, the 7 Ω resistor in fig. 40 should be tuned accordingly.

The eddy current losses in the substrate have also been quantified. Based on this data, it is thought that they don't make significant contributions to the sharpness of resonances in the power distribution network because they are too small²⁹. Note that skin effect losses are even smaller, and they are negligible in comparison to the eddy current losses in the substrate. Furthermore, it has been shown that the fill-shapes had a negligible impact on, both, the inductance and the series losses in all measurements. This holds up to $f \leq 8.5$ GHz, and probably far beyond.

The discussed test structures allow for a meaningful characterization of the abilities and limitations of RLCK-extraction tools, which is important for establishing a "trust-region" of the tool. The behavior of QRC was found to be consistent with eq. (19). The practically-relevant properties of RLCK-extraction tools based on eq. (19) are summarized in the following:

- A useful criterion for determining the fracture size for power routing is based on an effective wavelength λ , e.g. the wavelength of a MIS slow wave transmission line in case of power-routing without metallic background³⁰. Additional fracturing is not required and must be avoided because the linear solver run time grows to the *third power* in the number of parasitic inductors.
- The substrate is neglected when computing the partial inductance matrix using eq. (19). The RLCK-circuit generated by such tools is highly accurate if and only if the magnetic field lines penetrate deeply into the substrate. This can be assumed below the critical distance. These models can precisely describe the wave propagation in the coplanar strips as well as multiple self-resonances in spiral inductors.
- In principle, if the mutual partial inductances are matched sufficiently well, the induction caused by differential AC currents is described correctly. The tested version of QRC was accurate down to $\kappa = 1\%$.
- Eddy currents in the lower metallization are correctly described if and only if these structures are line-like or if the metal plates are slotted such that the eddy-current carrying metal segments are line-like.

In the future, the proposed approach of dampening of resonances in the power distribution network by exploiting eddy currents in a circular metal

²⁹ Specifically, a range of plausible resonator parameters were tried out for $d \leq 0.385$, but in each instance the quality factor was not significantly changes by adding substrate eddy-current losses.

³⁰ Note that for the lower metallization, the effective λ is usually much smaller than for the investigated coplanar strips, because of an increased capacitance per length.

strip should be tested using a test chip. Furthermore, it is recommended to experimentally investigate the implications of the magnetic decoupling due to eddy currents in the n-buried layer on RF-immunity tests. Future theoretical investigations into these eddy currents could attempt find a closed-form solution of the differential TEM-mode, e.g., using complex image theory. In practice, the n-buried layer is structured, which was not considered in this section. An open question is how the presence of a large number of deep trenches affects the eddy currents in the n-buried layer. It should be noted that the die-pad below the die certainly also results in a magnetic decoupling at distances larger than the die thickness. This effect, which might be relevant for very thin dies, is easily described using the method of images [128]. However, to the current understanding, the RLCK-extraction tool QRC do not support this natively.

The developed test structures could be used as a blue print for meaningful tool and runset regression testing. It is very important to qualify RLCK-extraction tools with true 3D test-structures as well, i.e. the simple loops, the spiral inductors and the folded, nested loops. It was exemplified that weaknesses of these tools, of which any user must be well aware, may otherwise remain hidden. Also the tool's capability to correctly account for the current distribution in a wire should be addressed. A neglect of the current cross section might cause mispredictions in the inductive coupling coefficient between the power-metal and metal-4 (e.g. the errors in the light green curve in fig. 39 (b)). The observed weakness in the tested QRC version regarding angled segments and the provided workarounds must be further investigated. It is recommended to evaluate and compare of other RLCK-extraction tools with respect to their abilities in predicting the magnetic decoupling due to eddy currents in the n-buried layer, and due to eddy-currents in the die-pad.

4.8 Summary

- If a supply- or ground-pin is shared among multiple modules, the additional on-die resistance and inductance may become a concern. In RF-immunity testing, weak on-die inductive couplings might be implicated. In future high-frequency extensions of DPI-testing, resonances in low-voltage internal power domains might be excited.
- A novel approach for the extraction of RLCK-parameters of transmission lines was developed, which uses the matrix-logarithm of ABCD-parameters. In addition, de-embedding was performed, and the errors arising thereof were estimated by comparing four different length variants.
- Above a certain critical distance, the coplanar strips appear to decouple into two microstrip-alike transmission lines, in which the n-buried layer carries the return current. At 8 GHz, the measured critical distance was 0.13 mm, and at 1 GHz, simulations yield an expectation of 1 mm. The FEM-eigenanalysis has shown that the critical distance is roughly proportional to $f^{-0.85}$.
- The eddy current losses in the substrate have also been quantified. It was argued that they don't make significant contributions to the sharpness of resonances in the power distribution network because they are too small. Nevertheless, they far outweigh the skin effect losses.
- The metal fill-shapes are completely negligible, both for the self and mutual inductances, as well as in the eddy current losses. This holds up to 8.5 GHz, and probably far beyond.
- To describe the quality factor of resonances in low-voltage internal power domains, numerous high-frequency losses must be accounted for. A grounded or floating single-turn metal loop, which mediates between the power and the ground conductors, might be engineered to dampen resonances over a broad frequency range.
- Below the critical distance, the differential TEM mode of the metal-insulator-semiconductor (MIS) slow wave transmission lines is excellently described by RLCK-extraction tools such as QRC. Moreover, eddy currents in the lower metallization are correctly described if and only if these structures are line-like or if the metal plates are slotted such that the eddy-current carrying metal segments are line-like.
- Regarding tool-qualification, it is important to also consider true 3D test-structures, i.e. the simple loops, the spiral inductors and the folded, nested loops. Otherwise, weaknesses of these tools, of which any user must be well aware, may remain hidden. It is recommended to evaluate and compare of other RLCK-extraction tools with respect to their abilities in predicting the magnetic decoupling due to eddy currents in the n-buried layer, and due to eddy-currents in the die-pad.

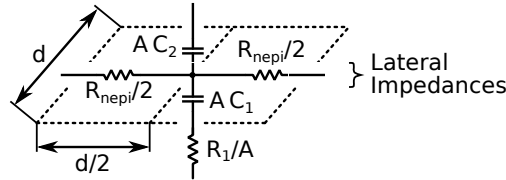
CHAPTER 5

Accurate and Efficient Simulation of Substrate Couplings

5.1 Low-Dimensional Models of the Wafer-Substrate

As pointed out in sec. 2.6.2, a major challenge in setting up substrate extraction or substrate noise analysis tools is picking a suitable level of abstraction. This section discusses approaches that approximate large areas of the n-buried layer as equipotential, which provides a rather high level of abstraction. The presented theory has multiple applications, ranging from substrate extraction runset development, e.g. for QRC (sec. 2.6.2), the determination of the boundary conditions in field simulators (sec. 5.2.1), to obtaining accurate equivalent circuits that are amenable to pencil-and-paper calculations (sec. 6.7). This section also presents the results of [44].

In state-of-the-art BCD-technologies, the n-buried layer, which resides on the wafer-substrate, is highly doped and thus has a low sheet resistance R_{nepi} (see sec. 2.2). Consider a sheet of the n-buried layer with of area $A = d^2$, which is connected to the wafer-substrate by a capacitance of AC_1 and to the overlying wells by AC_2 :



The resistance R_1/A represents the resistance of the wafer-substrate, and will be equated with the resistance to the die-backside, for simplicity. In the following, the *critical area* A_c is defined as the area A at which the sheet conductance R_{nepi}^{-1} equals the absolute total vertical admittance:

$$\frac{1}{R_{\text{nepi}}} = A_c \left| 2\pi i f C_2 + \left(\frac{1}{2\pi i f C_1} + R_1 \right)^{-1} \right| \quad (61)$$

Due to the low R_{nepi} , this critical area at $f = 1$ GHz is typically rather large (exact numbers may not be stated in order to protect the IP). The square root of the critical area $\sqrt{A_c}$ is an upper limit to the resolution of the voltage field in the n-buried layer. Moreover, in some cases, even areas of the N-buried layer that are much larger than A_c can be described as a single net: Firstly,

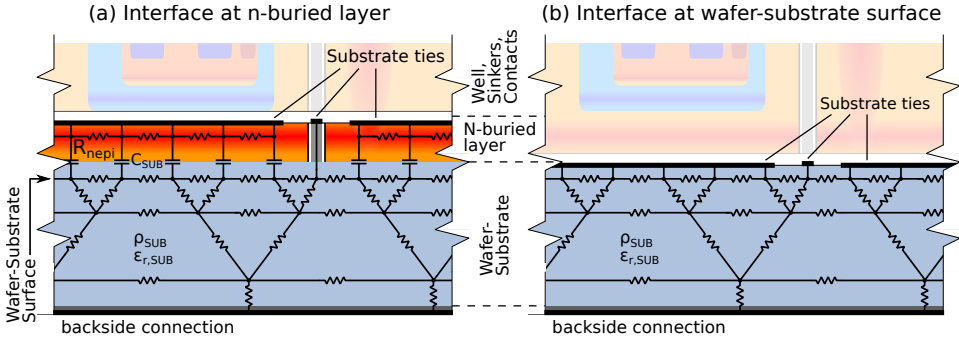


Figure 43: Two different approaches for defining the electrical interface between SPICE device models (above the substrate ties) and a low-dimensional field model of the substrate (below the substrate ties). The substrate ties, each of which covers a large area, are either (a) placed above the p-n-junction between the n-buried layer, or (b) they are placed below it.

assume that the wells are connected to the same electrical net as the n-buried layer, e.g. in an intermediate region between analog modules (see sec. 6.3.1). Here, currents across C_2 can be neglected, and assigning $C_2 := 0$ increases A_c to multiple square millimeters. Secondly, consider a HV-device where the spacing of the individual transistor fingers is much smaller than $\sqrt{A_c}$. The voltage field in the n-buried layer cannot resolve these individual fingers, and it can thus be considered location-independent. However, it must be kept in mind that counter-examples can be constructed as well: For example, a noisy, well-contacted N-well that is in the order of A_c .

If the voltage in the n-buried layer is roughly location-independent, the n-buried layer in each pocket can be described using only one electrical node each. The experimental results from sec. 6.5.3 confirm that this assumption can lead to very accurate models. For substrate modeling, this assumption is *very useful* because it can be exploited to reduce the model complexity enormously: Equating R_{epi} with zero allows to exactly decompose the substrate into two parts: Firstly, a field model of the wafer-substrate, and secondly, a model of the overlying wells. The field model of the wafer-substrate has comparatively few terminals, and is therefore called *low-dimensional*. Moreover, the overlying wells are usually easily parameterized by lumped-element models.

Fig. 43 (a) illustrates this approach: The wells, sinkers and contacts above the n-buried layer are described by parameterized SPICE device models, whereas a field model is used to describe the n-buried layer, the wafer-substrate and the p-n-junction in-between. Their electrical interface is realized via *substrate ties*. From an electrical point of view, the substrate ties are terminals of the field model, whereas from a field-simulation perspective they impose boundary conditions on the electric field (see sec. 2.5.1). Assuming that the boundary

conditions are of the *prescribed voltage* type, the sheet resistance of the n-buried layer R_{nepi} is shorted-out, and thus it can be removed from fig. 43 (a). In this approach, there is only a single substrate tie for each n-epitaxial pocket, no matter its area.

However, in practice, approximations are made that go beyond fig. 43 (a): The interface between SPICE device models and the field model is often placed at the wafer-substrate surface, as shown in fig. 43 (b). This is attractive because:

1. This moves the diode below the n-buried layer into the device model, which allows for a precise description of its bias-dependent capacitance. Moreover, little modification to existing SPICE device models is required.
2. In substrate extraction tools which construct an equivalent circuit using an FEM/FDM mesh (sec. 2.6.2): The field model is frequency independent, and no RC-constants must be considered regarding the meshing. Moreover, depending on the tool, the resulting mesh might be more coarse by default.
3. If PCV (prescribed, constant voltage) boundary conditions are used, the Y-parameter representation of fig. 43 (b) can be interpreted as wafer-substrate resistances between large-area n-epitaxial pockets. This allows to draw simple circuit models that facilitate even pencil-and-paper calculations. In contrast, the Y-parameter representation of fig. 43 (a) is complex-valued and does not distinguish between substrate capacitances and resistances.

However, the approach of placing the interface below the p-n-junction of the n-buried layer (fig. 43 (b)) introduces additional approximations, the consequences of which are often poorly understood: In this case, the choice of the boundary conditions has a large effect, but this is rarely mentioned in literature [77], [78]. An approach frequently found in literature treats the wafer-substrate and the buried layer as a single resistive continuum [61], [168], [180], but this is limited to p-doped buried layers that do *not* form a p-n-junction with the wafer-substrate. In the following, the term *PCV-based substrate extraction* denotes the imposition of *prescribed voltage* boundary conditions directly onto the wafer-substrate surface, e.g. as in QRC runsets based on fig. 43 (b). Note that this effectively introduces a perfectly conductive plane beneath n-epitaxial pocket. The consequences of this artifact will be quantified in sec. 5.1.1. Resorting to a complex FEM/FDM representation that captures fig. 43 (a) is not the only solution: Sec. 5.1.2 explains how one can obtain accurate circuit models of the wafer-substrate which are nevertheless amenable to pencil-and-paper calculations.

5.1.1 The Impact of the Boundary Conditions

This section studies the approach of defining the interface at the wafer-substrate surface, i.e. fig. 43 (b), and it experiments with three different boundary conditions. For this purpose, a simple toy model with four substrate ties (A, B, C and T) and a backside connection is constructed. It is shown in fig. 44 (a). This is a two-dimensional system in which the wafer-substrate is assigned a sheet resistance of $R_{\text{sheet}} = \rho_{\text{SUB}}/d_z$ (see also table 1). Thus, it can be understood as a slice of thickness d_z with an isolating or periodic boundary at $z = \pm d_z/2$. Due to the fact that the studied system is two-dimensional, the intrinsic longitudinal trench resistance is necessarily neglected in the following, despite it exhibits a certain practical relevance (sec. 6.5.3). Since the dielectric constant $\epsilon_{r,\text{SUB}}$ and magnetic fields in the wafer-substrate can be neglected (see sec. 5.2.1), the current flow is governed by Laplace's equation:

$$\nabla\phi(\vec{x}) = 0 \quad (62)$$

where $\phi(\vec{x})$ is the electric potential and $\vec{J} := -R_{\text{sheet}}^{-1} \nabla\phi$ is the current density. The boundaries at the terminals “T” and “backside” both have prescribed, constant voltages. Therefore, this is representative of a die with a low-ohmic backside metallization (see sec. 2.2). In the following, the voltage at terminal k is called V_k , the current entering terminal k is denoted by I_k , and its associated part of the boundary is called χ_k . The conducted computer experiments vary the boundary conditions applied at “A”, “B” and “C” in fig. 44:

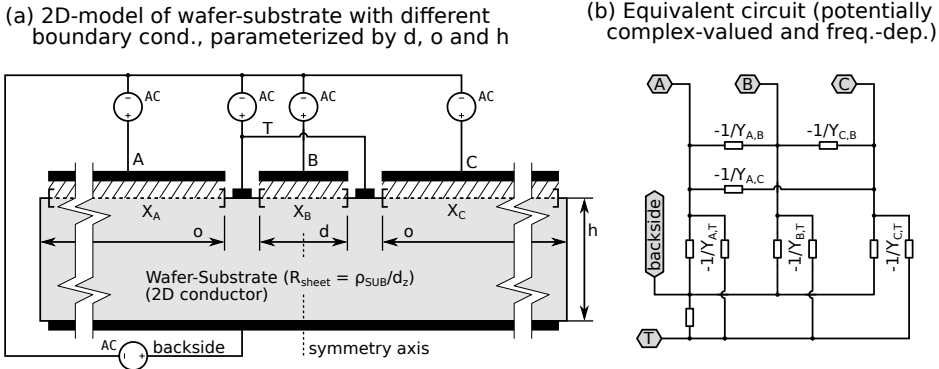


Figure 44: Part (a): 2D toy model of the wafer-substrate. The trenches T and the backside have PCV boundary conditions, whereas the coupling from A, B and C to χ_A , χ_B and χ_C , respectively, is realized by either PCV, PCCD or CLI boundary conditions (hatched area). The generalized π -equivalent of the toy model's Y-parameters is shown in (b). They are complex-valued and frequency-dependent only if the CLI boundary condition is used.

1. *Prescribed, constant voltage* (PCV) boundary condition: The terminal voltage V_k is imposed at every point of the associated surface χ_k and the terminal current I_k equals the total current through χ_k :

$$\phi(\vec{x}) = V_k \quad (\forall \vec{x} \in \chi_k) \quad I_k = - \int_{\chi_k} \vec{J}(\vec{x}) \cdot \vec{n} \, dA \quad (63)$$

where $\vec{n}$ is the normalized normal vector pointing outwards and dA is the area differential.

2. *Prescribed, constant current density* (PCCD) boundary condition: The terminal current I_k is evenly distributed over the associated surface χ_k , and the terminal voltage V_k represents the average electric potential over χ_k :

$$\vec{J}(\vec{x}) = -\vec{n} \frac{I_k}{|\chi_k|} \quad (\forall \vec{x} \in \chi_k) \quad V_k = \frac{1}{|\chi_k|} \int_{\chi_k} \phi(\vec{x}) \, dA \quad (64)$$

where $|\chi_k|$ denotes the area of χ_k .

3. *Capacitive-layer impedance* (CLI) boundary condition: A linear combination of the boundary current and voltage is constrained as follows:

$$\phi(\vec{x}) - \frac{1}{i\omega C_{\text{lay}}} \vec{J}(\vec{x}) \cdot \vec{n} = V_k + \frac{I_k}{i\omega C_{\text{lay}} |\chi_k|} \quad (\forall \vec{x} \in \chi_k) \quad (65)$$

where $C_{\text{lay}} := C_{\text{SUB}} d_z$ is a capacitance per unit length. Moreover, the terminal current I_k is defined as the total current through χ_k :

$$I_k = - \int_{\chi_k} \vec{J}(\vec{x}) \cdot \vec{n} \, dA \quad (66)$$

The PCV and PCCD boundary conditions are also commonly known as *Dirichlet* and *Neumann boundary conditions*, respectively [46]. The CLI boundary condition defined in eq. (65) is a kind of *Robin or impedance boundary condition* [46], [191] with a complex-valued, frequency-dependent coefficient. It has a special property which is very interesting for the extraction of wafer-substrate resistors in the presence of an n-buried layer, as will be explained in the following.

The dashed box in fig. 45 shows a subcircuit, which, as will be shown in the following, is equivalent to a wafer-substrate with the CLI boundary condition: Eqs. (67–69) in fig. 45 express the relations between circuit and field quantities. By means of eqs. (67–69), the AC current-voltage relations of $C_B^{(n)}$ and the

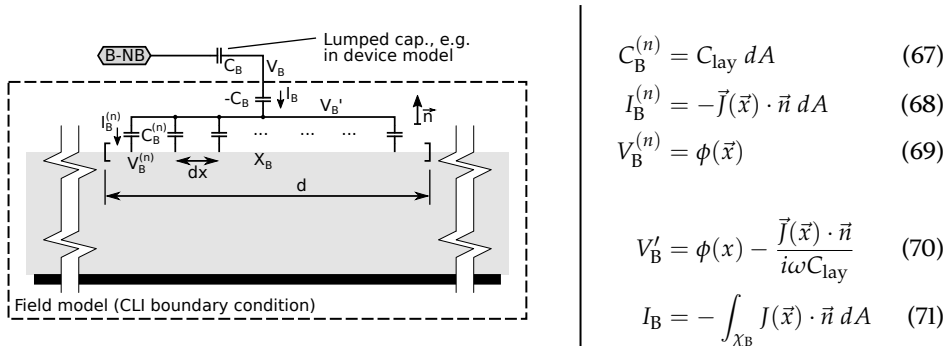


Figure 45: A field model of the wafer-substrate using CLI boundary conditions (dashed box) is connected to a lumped capacitor $C_B = |\chi_B|C_{\text{lay}}$. The CLI boundary condition can be interpreted as a capacitive layer, here shown as a large number of small capacitors $C_B^{(0)}, C_B^{(1)}, \dots$, connected in series with a lumped negative capacitor $-C_B$. From the terminal “B-NB”, the composite system appears as capacitive layer on top of a resistive sheet.

Kirchhoff's current law at V'_B are transformed into eqs. (70–71). Note that eq. (71) is equivalent to eq. (66). Furthermore, by substituting the AC current-voltage relation of $-C_B$ into eq. (70), the Robin boundary condition eq. (65) is obtained.

Assume a lumped capacitor $+C_B = |\chi_B|C_{\text{lay}}$, e.g. the p-n-junction capacitance from a SPICE device models, is externally attached to this field model, as shown in fig. 45. This positive lumped capacitor exactly compensates the negative lumped capacitor $-C_B$ inside the field model. This proves that embedding a field model with CLI boundary conditions in lumped capacitors results in a field model where the n-buried layer was included, i.e. it realizes fig. 43 (a). And hence:

Fig. 44 with PCV b.c. ... mimics PCV-based substrate extraction

Fig. 44 with CLI b.c., ... mimics substrate extraction with an embedded in lumped cap. interface at the n-buried layer

With the exhaustive, common-reference ports definitions, which is depicted in fig. 44 (a), an equivalent circuit can be obtained as shown in fig. 44 (b) ¹. This construction is based on the generalized π -equivalent (see sec. 2.4.1). In

¹ Note that a field model of the wafer-substrate with the CLI boundary condition does *not* contain the capacitance of the n-buried layer: Rather, it's Y-parameters only represent wafer-substrate resistors, much like the PCV boundary condition. However, it is different in the sense that the boundary current distribution was altered such that it correctly reflects the current density that is capacitively injected by the n-buried layer.

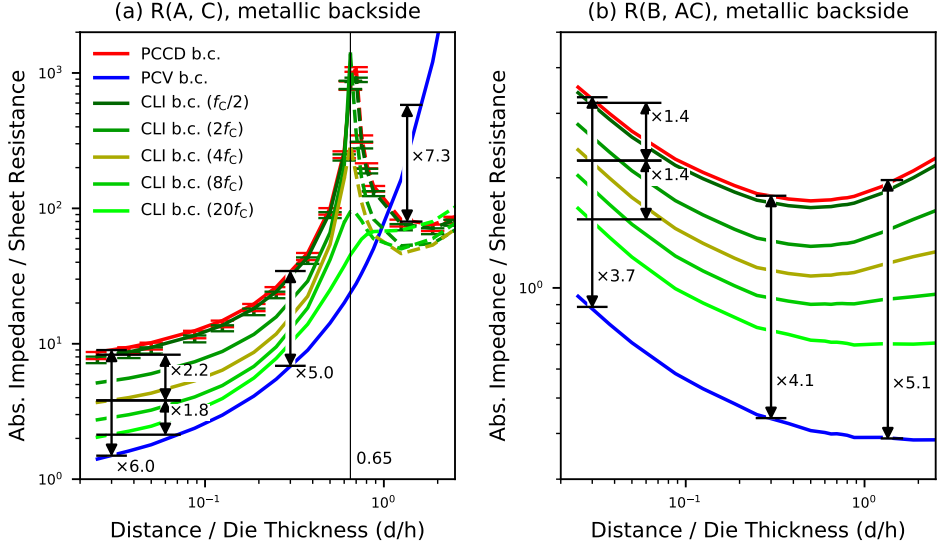


Figure 46: Absolute impedances between n-epitaxial pockets ($R(A, C) := |-1/Y_{A,C}|$ and $R(B, AC) := |-Y_{A,B} - Y_{B,C}|^{-1}$) as a function of the distance d for $o = 25h \approx \infty$. Error bars depict the maximum deviation from $o = 5h$ and $12.5h$. Dashed lines indicate a negative sign of $\text{Re}(-Y_{A,C})$ and $\text{Re}(-Y_{A,B} - Y_{B,C})$, respectively.

the following, the wafer-substrate impedances in this equivalent circuit are discussed. Since a commercial FEM software that supports the CLI boundary condition could not be found, in the course of this thesis, a custom 2D Laplace FEM-solver was implemented based on “triangle” [160], [172] and a general-purpose circuit simulator. The shown data was obtained using this tool flow, and in the limit of $o \rightarrow \infty$ (with o defined in fig. 44).

Fig. 46 (a) plots the absolute impedance between pocket A and pocket C, i.e. $R(A, C) := |-1/Y_{A,C}|$, over their distance d (see fig. 44). The coupling between two large-area pockets has a singularity roughly at $d = 0.65h$ in the PCCD and CLI boundary conditions but not with PCV boundary conditions, which is demonstrated by fig. 46 (a). A simplistic intuitive understanding of this effect will be suggested in sec. 5.1.3. Primarily, the impedances below the singularity are considered. They are positive, short-range and presumably far more relevant.

It can be shown that scaling R_{sheet} is a symmetry transform which does not change the system’s reaction, except for a proportional frequency shift and a proportional scaling of the Y-parameters. Moreover, scaling the die thickness h is approximately a symmetry transform², which only causes a

² That is, a slight scaling of the deep trenches can be neglected.

proportional frequency shift and a scaling of d . Therefore, in the following, the simulation results are generalized by normalizing the absolute impedance and the distance d to the sheet resistance R_{sheet} and to the die thickness h , respectively. The following *critical frequency* is defined:

$$f_C := \frac{1}{2\pi h R_{\text{sheet}} C_{\text{lay}}} = \frac{1}{2\pi h \rho_{\text{SUB}} C_{\text{SUB}}} \quad (72)$$

Due to the symmetries described above it is appropriate to express the frequency in units of f_C .

In fig. 46, it appears that, in the limit $f \rightarrow 0$, the CLI converges to the PCCD boundary condition. Conversely, in the limit $f \rightarrow \infty$, it apparently converges to the PCV boundary condition³. In the BCD-technology used in the test-IC from chapter 6⁴, if certain typical average values are substituted for h and C_{SUB} in eq. (72), the frequencies $f_C/2$ and $20f_C$ approximately correspond to 30 MHz and 1 GHz, respectively. It is remarkable that the CLI-result at $f = f_C/2$ is already very close to the PCCD-limit, whereas the CLI-result at $20f_C$ is still at a sizeable distance from the PCV-limit in fig. 46 (b). Thus, a PCV-based substrate extraction approach is not very accurate even at rather high frequencies like 1 GHz. Observe that for distances $d = 0.02h$ to $d = 0.3h$, the PCV-limit for $R(A, C)$ in fig. 46 (a) is smaller by a factor of 5 to 6 than the PCCD-limit. Therefore, it can be concluded that PCV-based substrate extraction *overestimates the coupling between two close, large-area pockets* by a factor of about 5 to 6 at 30 MHz and below. With a slight abuse of notation, $R(B, AC)$ shall refer to $(R(B, A)^{-1} + R(B, C)^{-1})^{-1}$, which is equal to $R(B, A)/2$ due to the symmetry axis in fig. 44. This is interpreted as the substrate coupling of a pocket of length d to its immediate surroundings. It can be seen that the PCV-limit for $R(B, AC)$ is smaller by a factor of 5.1 to 3.7 than the PCCD-limit. This holds at large distances, e.g. $d = 1.5h$, as well as at small distances, e.g. $d = 0.02h$. Therefore, a PCV-based substrate extraction approach *overestimates the coupling of a pocket to its immediate surroundings regardless of its size* by a factor of 5.1 to 3.7 at 30 MHz and below.

Above the singularity, i.e. for $d > 0.65h$, with CLI boundary conditions, the sign of the real part of $Y_{A,C}$ changes (indicated by dashed lines in fig. 46 (a)), and the CLI-data rapidly diverges from the PCV-data. At a distance of only $d = 1.5h$ they already differ by a factor of > 7.3 , regardless of the frequency. It is concluded that PCV-based substrate extraction *cannot* predict direct

³ This can be proven mathematically by means of eq. (65), and interpreting I_k as the total current (eq. (66)) and V_k as the average electric potential (eq. (74)).

⁴ The critical frequency depends on C_{SUB} and ρ_{SUB} , and the plotted curves depend on the deep trench width. Be aware that these parameters might be different in other technologies.

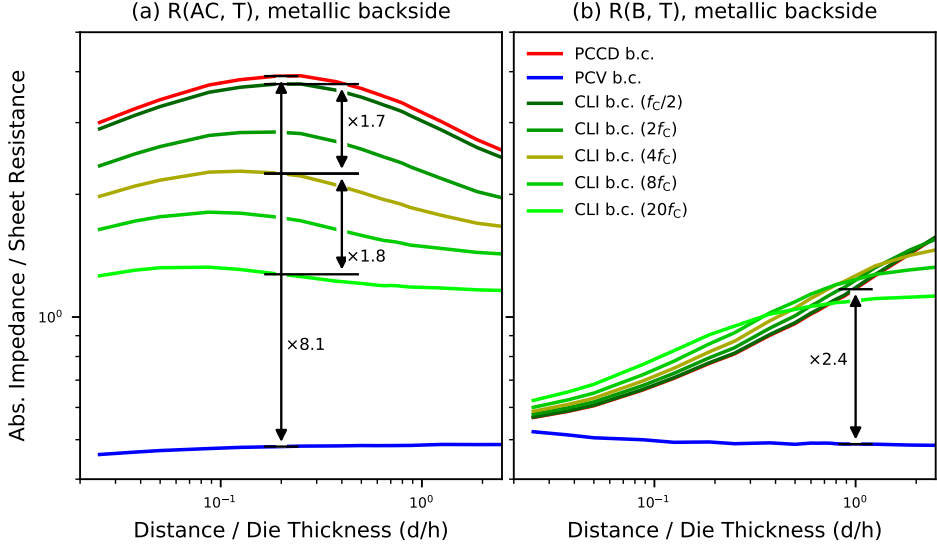


Figure 47: Absolute impedances from n-epitaxial pockets to trenches ($R(AC, T) := | -Y_{A,T} - Y_{C,T} |^{-1}$ and $R(B, T) := | -1/Y_{B,T} |$) as a function of the distance d for $o = 25h \approx \infty$. Error bars depict the maximum deviation from $o = 5h$ and $12.5h$.

couplings between two pockets A and C that are separated by a large-area pocket B with $d > 1.5h$ very well. However, this might *not* be very relevant, as will be elaborated in sec. 5.1.3.

Fig. 47 shows the absolute impedances from the pockets A, B and C, respectively, to the trenches T that delimit the pocket B (see fig. 44). Again abusing notation, $R(AC, T)$ is defined as $(R(A, T)^{-1} + R(C, T)^{-1})^{-1}$ which equals $R(A, T)/2$ by mirror symmetry. The PCV-limit underestimates the resistance between large-area pockets and trenches $R(AC, T)$ by a factor of up to 8.1. Conversely, as shown in fig. 47 (b), the resistance of a pocket with $d = h$ is underestimated by a factor of “only” 2.4. Moreover, in the limit of $d \rightarrow 0$, the PCV-limit becomes increasingly accurate in estimating the resistance between B and its trenches.

The results presented above only apply to the connected metallic backside, due to the backside terminal with a PCV boundary condition in fig. 44 (a). If the backside terminal is dropped from the simulation, one obtains data that is representative of a non-metallized backside with a negligible backside capacitance. Figs. 48 and 49 show the results for such an unconnected backside. Importantly, by comparing results for different o , it is observed that the PCCD-curves apparently did not properly converge in the limit $o \rightarrow \infty$, and they are therefore not shown. It is concluded that, for an unconnected backside, the

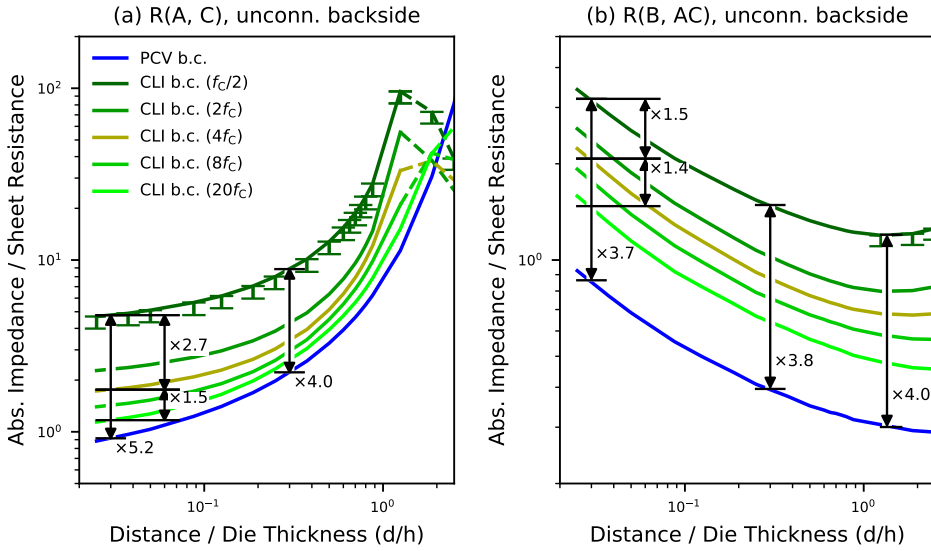


Figure 48: Absolute impedances between n-epitaxial pockets in the case of a non-metallized backside with a negligible backside capacitance. In contrast to fig. 46, here the backside terminal was removed from the toy model (fig. 44 (a)).

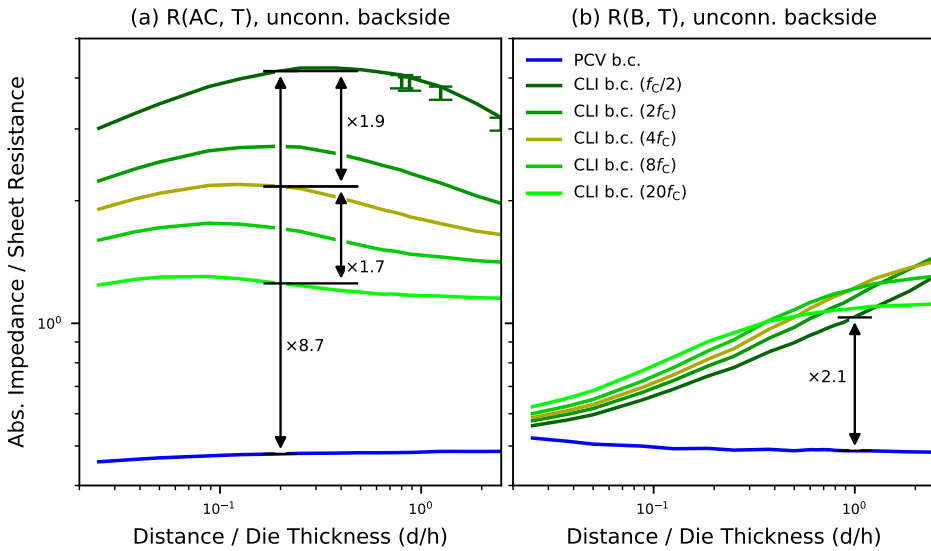


Figure 49: Absolute impedances from n-epitaxial pockets to trenches in the case of a non-metallized backside with a negligible backside capacitance. In contrast to fig. 47, here the backside terminal was removed from the toy model (fig. 44 (a)).

PCCD boundary condition is not representative of the CLI boundary condition at low frequencies. The PCCD boundary condition is thus not recommended in dies with an unconnected backside.

5.1.2 Equivalent Circuits Amenable to Pencil-and-Paper Calculations

A model of the substrate that facilitates pencil-and-paper calculations must:

1. consist of a small number of macroscopic circuit elements⁵ which
2. have a clear physical interpretation and in which
3. nodal voltages and branch currents have a clear physical interpretation.

Clearly, (1.) rules out FEM/FDM representations. Y-parameter representations from PCV-based substrate extraction satisfy all of (1.–3.), but they are not particularly precise, as argued in sec. 5.1.1. This section describes how to compute more accurate equivalent circuits, which are suitable for both AC and transient simulations, using field simulation with CLI boundary conditions in practice. Moreover, it provides a physical interpretation of nodal voltages and branch currents in the so-obtained circuit models.

Commercial field simulators or substrate extraction tools that directly support the CLI boundary condition could not be found. However, it can be emulated easily using the construction from fig. 45: In each pocket, a thin, dielectric layer, which has a carefully controlled sheet capacitance C_{SUB} , is placed above the wafer-substrate. Furthermore, sufficiently good electrical conductors contact the dielectric layer from above, and they are tied to terminals with PCV boundary conditions. This is visualized by fig. 13 in sec. 2.5.1. This three-dimensional AC-conduction problem is solved numerically for a suitable frequency range⁶. Subsequently capacitances C_k are de-embedded from the resulting network parameters, i.e. negative *lumped* capacitors are put in series. Special care must be taken regarding the following aspects:

- The de-embedded capacitors C_k must be very precisely matched to the total capacitance of the dielectric layers because small mismatches were observed to cause sizeable errors. Y-parameters for $f \ll f_C/2$ should not be used because, in this frequency range, these errors are enormously amplified.

⁵ Note that the number of circuit elements can be further reduced using sensitivity or alteration section, as will be demonstrated in sec. 6.7.

⁶ Alternatively, a substrate extraction tool with sufficient accuracy, e.g. the tool developed in this thesis (see sec. 5.2), in combination with a circuit simulator (S-parameter analysis), can be used.

- The capacitance per area should be the same for all dielectric layers, i.e. the bias points of all n-buried layers should be equal. Otherwise, f_C would vary locally, and thus picking a sampling frequency globally, as described below, becomes a poorer approximation.
- The backside should be either connected to a terminal using PCV boundary conditions, or it should be non-metallized and unconnected. A dielectric layer at the backside may not be used because this would introduce a second critical frequency ⁷.
- Take particular note that this approach imposes PCV boundary conditions at the deep trenches, which shorts-out the composite longitudinal trench resistance. This can cause sizeable deviations (see sec. 6.5.3). In a more refined approach one might include the intrinsic longitudinal trench resistance, the distributed trench oxide capacitance, as well as the metallization connected to the deep trenches, into the field simulation. Instead of applying PCV boundary conditions, one would then contact the deep trenches only at certain points, e.g. at the seal-ring's ground connections.

The Y-parameters of the wafer-substrate with the CLI boundary condition are then sampled at f_S , which is a suitable multiple of f_C . For example, the data in sec. 5.1.1 suggests that $f_S = 4f_C$ (yellow curve) may be a suitable choice to cover the frequency range 30 MHz to 1 GHz for a typical die thickness: Here, the deviation of the absolute impedances was never significantly larger than 2. However, one should *not* presume that $f_S/f_C = 4$ is an universal constant. In fact, this factor depends on the maximum frequency of interest $f_{\max}$, on the die thickness h , and on whether one considers absolute impedances or only the real part. Rather, given that the real part of Y_{ij} is of interest, the following formula, which was learned from the experience in sec. 6.3.1, is proposed:

$$f_S = \sqrt{4f_C f_{\max}} \quad (73)$$

This formula was optimized such that the components of $\text{Re}(Y(f_S))$ roughly equal the geometric mean between the LF-limit and $\text{Re}(Y(f_{\max}))$. ⁸

⁷ In ICs with an exposed-pad but without a galvanic backside connection, the backside capacitance may be an important parameter (see sec. 6.5.2). However, for pencil-and-paper calculations, it is recommend to rather consider two corner cases instead: A shorted, connected backside and a non-connected backside. The experimental result should be between these corner cases – see also sec. 6.3.1.

⁸ Directly computing this geometric mean instead of sampling appears to be a more simple alternative: However, this might not be a good idea because it cannot deal properly with sign changes and it might destroy a matching between positive and negative resistors.

Finally, the Y-parameters $Y(f_S)$ must be converted into real numbers, such that a resistor network of the wafer-substrate can be obtained using the generalized π -equivalent. One approach is to take the component-wise absolute value of the Y-parameter matrix. However, as discussed in sec. 5.1.1, in the PCCD-limit, some entries of Y , specifically $Y_{A,C}$ for $d > 0.65$, vary in sign, and this information would be lost. Therefore, rather, it is recommended to discard the imaginary part of $Y(f_S)$. Given CLI boundary conditions, Y-parameters with a phase φ_{ij} in the range $[45^\circ, 135^\circ]$ are thereby changed in magnitude by more than a factor of two. However, $\varphi_{ij} \in [45^\circ, 135^\circ]$ was *not* observed for any Y-parameter discussed in sec. 5.1.1 at $4f_C$, except for $Y_{A,C}$ in a narrow range of $d/h \in [0.57, 0.68]$ near the singularity. Moreover, observe that discarding the imaginary component does *not* alter the Y-parameters in the PCCD- and in the PCV-limit. Therefore, it is presumed that the errors introduced by this operation to the individual components of Y are mostly negligible.

Since the resistor network obtained from $\text{Re}(Y(f_S))$ contains negative resistors, the passivity of the wafer-substrate model is not self-evident. Passivity is important for stable, transient simulations (see sec. 2.3.2 and sec. 2.4.2). Indeed, $\text{Re}(Y(f_S))$ is actually passive, as will be shown by the following rather abstract argument: In fig. 45, replace the capacitor $-C_B$ by an inductor $L_B = (4\pi^2 f_S^2 C_B)^{-1}$. By construction, its Y-parameters remain unchanged at f_S . Moreover, since the resulting field model then only consists of resistors, positive capacitors and positive inductors, it is then trivially passive and reciprocal at all frequencies. Therefore, in particular it follows that $Y + Y^H$ is positive-definite at $f = f_S$ (see sec. 2.4). And hence, at $f = f_S$, $\text{Re}(Y) = (Y + Y^*)/2 = (Y + Y^H)/2$ is positive-definite as well.

In the so-obtained circuit model, resistors are interpreted as the impedance of the wafer-substrate. This resistor network is directly connected to device models, which contain lumped diodes that describe the p-n-junction between the n-buried layer and the wafer-substrate. By eq. (66), currents across these diodes can be interpreted as the *total current* that enters the wafer-substrate. The question arises, how the nodal voltages can be interpreted. By integrating both sides of eq. (65) over χ_k , and then substituting eq. (66), one arrives at the following result:

$$\frac{1}{|\chi_k|} \int_{\chi_k} \phi(\vec{x}) dA = V_k \quad (74)$$

Therefore, in a field model with CLI boundary conditions, the terminal voltage V_k is interpreted as the *average surface potential* of the wafer-substrate ⁹.

⁹ Note that this also trivially holds for PCV and PCCD boundary conditions

5.1.3 Conclusion

It was shown that low-dimensional, PCV-based substrate extraction suffers from pronounced artifacts: Substrate resistors between two n-epitaxial pockets are underestimated by up to a factor of 6, and substrate resistors connecting large-area pockets with surrounding deep trenches are underestimated by up to a factor of 8.

This applies to any method that constructs equivalent circuits for pencil-and-paper calculations using field simulations with PCV boundary conditions. It also applies to substrate extraction tools that place the interface on the wafer-substrate (fig. 43 (b)). As a remedy, the CLI boundary condition, which corrects the current paths below the n-buried layer at lower frequencies, was introduced. These can be implemented by de-embedding lumped capacitors from field simulations that include a capacitive layer. Thereby, more accurate circuit models for the purpose of pencil-and-paper calculations can be constructed, in which nodal voltages should be interpreted as the *average surface potential* of the wafer-substrate. The practical usefulness of this approach will be demonstrated in sec. 6.7. Note that crude estimations of substrate couplings might be conducted directly using the data from figs. 46–49.

A debated detail regarding the implementation of substrate extraction runsets is whether the n-buried layer should be included in the field model. The discussion above leads to the strong recommendation to include it in the way shown in fig. 43 (a): Even though the n-buried layer’s sheet resistance is neglected, this method removes the above-mentioned pronounced artifacts because the p-n-junction is fractured into an array of capacitors. Verifications of substrate extraction runsets that only consider small-area pockets or very high frequencies have an insufficient coverage: For example, PCV-based substrate extraction is acceptable for small-area pockets at 1 GHz, but it might be insufficiently accurate for large-area pockets at 100 MHz.

An interesting conclusion is that, in circuits for pencil and paper calculations, negative resistors should be present between n-epitaxial two pockets A and B with a distance d beyond the “singularity” at $d = 0.65h$. Preliminary results indicate that these negative resistors $-Y_{A,C}^{-1}$ cancel out wafer-substrate currents flowing indirectly from A to C, e.g. via the wafer-substrate surface below B. In a sense, these compensate for the fact that there is no perfectly conductive plane below B, as it would be in the PCV boundary condition. Unfortunately, these compensation currents are unintuitive and probably prone to cancellation errors. On the other hand, these negative resistors were found to be *negligible* in the developed test-IC (see sec. 6.7). However, this might be only due to the fact that the “positive” substrate coupling via the deep trenches dominates “mixed-sign” direct couplings between n-epitaxial pock-

ets. This might change if the grounding of the seal-ring is improved (sec. 6.7). Moreover, in ICs with a more thin die, the amount of negative resistors and hence possibly their relevance would increase. Future work could aim to study the role of these negative resistors and in the prediction of RF-emissions more thoroughly.

5.2 An Automated Substrate Extraction Tool for BCD-Technologies

Despite the low-dimensional substrate models from sec. 5.1 can achieve a high accuracy, there are some inherent limitations: Firstly, the n-buried layer is regarded as equipotential, which usually works well in practice. However, at higher frequencies or in some particular IC-layouts, this assumption may be violated (see introduction of sec. 5.1). Secondly, these models neglect parasitic elements that interface with the n-buried layer or with the deep trenches: For example, the inductance of the seal-ring is conjectured to become relevant for the RF-emissions of DC/DC-converters if its ground connection is on the far side of the transceiver (sec. 6.7). Moreover, n-sinkers form voltage dividers with other parasitic impedances, and from its division ratio it depends whether the n-sinker resistance and their metal routing is negligible. In technology-modifications with a reduced ρ_{SUB} (see also sec. 6.6.2) or if the die-thickness is decreased, these parasitics might increase in relevance. Third, low-dimensional models put an upper limit on the number of devices. Hence, their utility is diminished for ab-initio studies and pre-silicon verifications that aim for a high coverage. These limitations can only be overcome by a drastic increase in the number of substrate ties. However, dense representations of the substrate without internal nodes do not perform well asymptotically (sec. 2.6.2). Rather, the substrate model should be obtained by re-interpreting the FEM/FDM-equations as a RC-network.

Also consider that investments in software automation are often unavoidable: For example, manually connecting more than e.g. 100 devices to terminals of the substrate model is very time consuming. Only by automation one can achieve a seamless integration of the substrate model with other parasitic elements, like the inductance in power routing (chapter 4). Moreover, the composite longitudinal trench resistance, which is strongly affected by the deep trench metallization, is of some relevance (sec. 6.5.3). Without further automation, each trench segment in the field simulation would have to be manually associated with a metal resistance (sec. 5.1.2). This is clearly an error-prone and tedious process.

For these reasons, in the course of this thesis, a new fully-automated substrate extraction tool flow based on 1st-order FEM was developed. It captures the physics of majority carriers only (sec. 2.6.2). This tool-flow as such is technology-independent, but it was adapted to and tested on the BCD-technology used in the test-IC (sec. 2.2). It is intended to be applied to manually simplified IC-layouts (see sec. 6.3.1) containing several hundred or thousand devices. In addition to AC-simulations, this tool flow shall also support transient simulations, which might be needed for initial transient simulations and, e.g. for the prediction of the robustness to test pulses according to ISO 7637. In order to support transient simulations, special care must be taken that the substrate model is passive. The presented tool flow is *not* based on a commercially available tools like QRC, but instead a novel software is used to generate the substrate netlists. In the course of this thesis, this novel software was written in C++. Thereby, a scientific analysis of the model accuracy is enabled, and it becomes more transparent how the tool- and simulator-implementation are connected to the simulation efficiency.

This section also presents results that have been published previously in [163].

5.2.1 Overview of the Developed Substrate Extraction Tool Flow

The developed substrate extraction tool flow assembles a *composite model* from three subcircuits as shown in fig. 50 (b). The extracted or layout netlist is created by a standard RC- or RLCK-parasitic extraction tool flow (sec. 2.6.1). Conversely, the 2D and the 3D substrate netlists originate from the novel software developed in the course of this thesis.

The 2D substrate netlist describes the n-buried layer, and, depending on the configuration, some wells that exist therein. The IC-layout is decomposed into multiple disjoint *regions*¹⁰, each of which is associated with a *region type*. For example, fig. 50 (a) shows four regions of type “deep-trench”, one region of type “LV/MV-P-well” and one region of type “LV/MV-N-well”. Each region is modeled as multiple *mesh layers*, which are stacked on top of each other. A *mesh layer* denotes a resistor-network representation of a planar conductor, e.g. a FEM-discretization of Laplace’s equation on a triangular mesh. This stack of mesh layers extends down to the surface of the wafer-substrate. The region type defines the number of mesh layers and their physical parameters, i.e. rows R_{nepi} to $R_{\text{trench,z}}$ from table 1. Moreover, the region type defines their interconnection and their connection to the 3D substrate netlist, i.e. rows C_{trench} to C_{nw} from table 1. Regions contain so-called *substrate ties*, which

¹⁰ In the context of the developed substrate tool flow, a *region* refers to polygons that describe fragments of deep trenches or to subdivisions of n-epitaxial pockets.

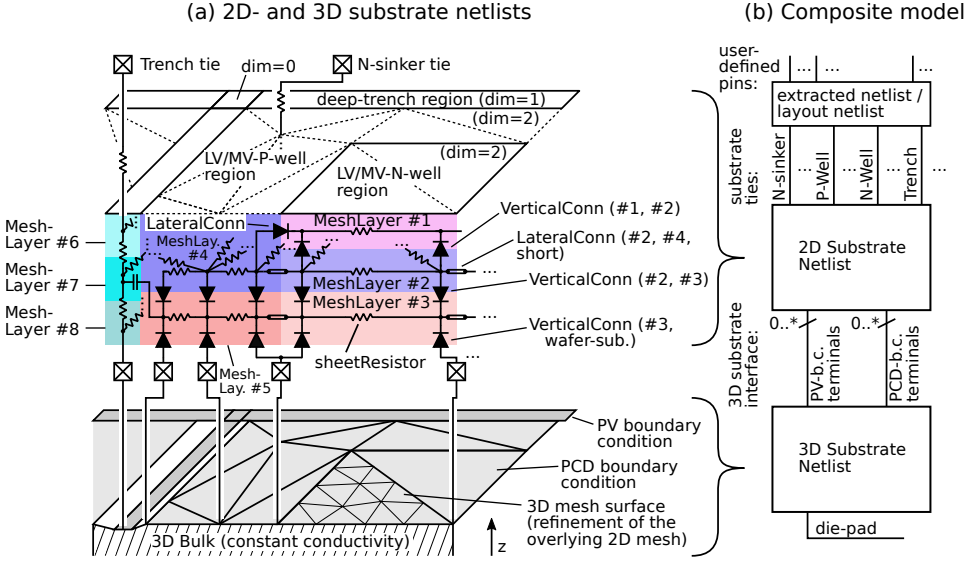


Figure 50: Part (a): The 2D and the 3D substrate netlist generated by the C++ tools developed in the course of this thesis. Part (b): In combination with an extracted or layout netlist, they form the composite model.

define the connections between the 2D substrate netlist and the extracted or layout netlist. Some substrate ties correspond to n-sinkers and contact arrays, i.e. rows R_{nsink} to $R_{\text{trench,via}}$ from table 1.

Typically, a single mesh layer corresponds to a peak in the dopant concentration [168]. This approximation is presumably very good if the peaks are pronounced and isolated. Often, a mesh layer that corresponds to p-type silicon is vertically surrounded by mesh layers corresponding to n-type silicon, and vice versa. Such a mesh layer is then connected to its vertically adjacent mesh layers by an array of diodes, as shown in fig. 50 (a). Conversely, vertically adjacent mesh layers are connected by resistors if there is no p-n-junction in-between. Additionally, the developed software creates lateral connections at the boundary line between two regions. For example, mesh layer #4 and mesh layer #2 in fig. 50 (a) are part of a LV/MV-P-well-region and a LV/MV-N-well-region, respectively. However, both mesh layers correspond to the logic implant in a LV/MV n-epitaxial pocket (see fig. 3 in sec. 2.2), and they must therefore be shorted. Other lateral connections are formed between mesh layer #7 and #5 (trench oxide capacitance), and between mesh layer #4 and mesh layer #1 (well fringe capacitance). Mesh layer #5 and mesh layer #3 are shorted since both correspond to the n-epitaxial layer.

The diodes that connect mesh layers with each other and with the 3D substrate netlist only correctly describe the reverse bias state. Their model

parameters merely account for the equivalent series resistance in reverse bias, as well as for the bias-dependence of the junction capacitance. Due to conductivity modulation and the formation of bipolar transistors, the forward bias state is by far more complex (see sec. 2.2) and is therefore not accounted for. Thus, the developed substrate tool flow cannot be used for simulations of minority carrier injection ¹¹.

Each region is associated with a *dimension* $\in \{0, 1, 2\}$, which determines how the 2D mesh is generated. In regions of dimension 0, each mesh layer collapses to a single electrical node, and regions of dimension 1 are meshed by quads with an arbitrary aspect ratio ¹². Regions of dimension 2 are triangulated by a Delaunay mesh, in which each triangle satisfies a lower bounds on its angles. This is achieved by invoking the software tool “triangle” by J. R. Shewchuk [160], [172]. The 2D meshing process may refine the boundary line between two regions. However, mesh triangles or quads may not cross the boundary line between two regions, and t-junctions are allowed neither in the interior of a region nor at its boundary line. The 2D meshes of all mesh layers coincide when projected along the z-axis.

The 3D substrate netlist is a resistor network that represents the wafer-substrate by a FEM-discretization of Laplace’s equation on a tetrahedral mesh. This tetrahedral mesh will be called 3D mesh in the following. Furthermore, this resistor network may be reduced by eliminating nodes – this is further detailed in sec. 5.2.4. From eq. (14) it is concluded that displacement currents in the wafer-substrate can be neglected if $\rho_{\text{sub}}^{-1} \gg 2\pi f \epsilon_0 \epsilon_{\text{r,sub}}$. In the considered BCD-technology, this is satisfied below 1 GHz, and this approximation might even be appropriate up to 10 GHz. Furthermore, it is proposed to assume that the magnetic field has a negligible impact on the current path in the wafer-substrate if the impedance due to the internal inductance [76], [92] is more than 100-fold smaller than the ohmic resistance. It is easily shown that for a circular conductor with radius R and a resistance per length of $\rho_{\text{sub}} / (\pi R^2)$, this holds if $R < 2\delta / \sqrt{100}$, where $\delta = (2\rho\omega^{-1}\mu_0^{-1})^{1/2}$ is the skin depth [26]. The condition $H_{\text{die}} < 4\delta / \sqrt{100}$ is satisfied even at $f = 10$ GHz. Hence, in the following, $\epsilon_{\text{r,sub}}$ is equated with 0 and the magnetic field is neglected. Thereby, the governing differential equation reduces to Laplace’s equation (see sec. 2.5.1).

The surface of the 3D mesh is a refinement of the overlying 2D mesh, as exemplified in fig. 50 (a). Prescribed current density (PCD) boundary

¹¹ For this reason, the developed tool flow is of limited benefit to latch-up-simulations and to some ESD-simulations.

¹² Dimensions 0 and 1 are used for deep trenches corners and lines, as shown in fig. 50 (a). In interaction with the user, narrow n-epitaxial pockets may also be associated with a dimension < 2 .

conditions are imposed on the areas of the wafer-substrate surface that are covered by the n-buried layer. Conversely, prescribed voltage (PV) boundary conditions are imposed where trenches form a galvanic contact. This approach is justified as follows: As argued in sec. 5.1, the resolution of the n-buried layer's 2D mesh can be as coarse as the critical area from eq. (61). Conversely, this does not apply to the wafer-substrate: For example, in the vicinity of deep trenches, the current paths are strongly curved. The coarse finite elements in the n-buried layer's 2D mesh can be connected to the wafer-substrate by a single lumped capacitor and using the CLI boundary condition (sec. 5.1.1). Assume the model's range of validity is limited by some cutoff frequency f_C . If the size of the finite elements of the n-buried layer's 2D mesh is sufficiently small, for $f < f_C$, the CLI boundary condition approximately reduces to the PCD boundary condition.

5.2.2 Description of the Tool Flow and the 2D Substrate Netlisting Step

The developed substrate tool flow makes use of Calibre [131], QRC [30], Cadence SKILL-scripts and two executables implemented in C++. The transformation of the layout-data into the composite model (#6) is illustrated by the data-flow diagram in fig. 51. It is an extension of the standard RC- or RLCK-parasitic extraction tool flow (see sec. 2.6, fig. 15). The processes and data stores that are encapsulated by the dashed gray rectangle in fig. 51 were added, and the LVS-runset was modified. The 3D substrate netlisting process is separate from the 2D substrate netlisting process, and it is carried out after the 2D substrate netlisting process. The data passed from the 2D to the 3D substrate netlisting is called *3D substrate interface* (#2). Two separate netlists are generated by the 2D and the 3D substrate netlisting (#4, #5), respectively.

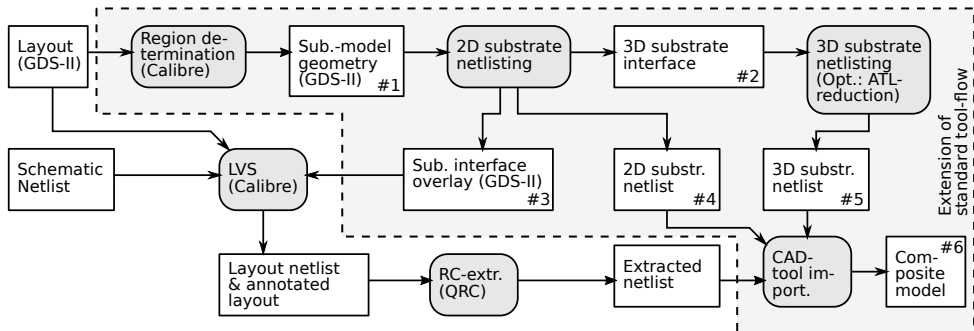
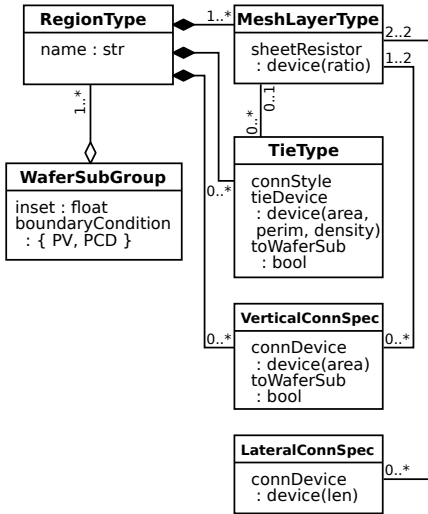


Figure 51: The developed substrate tool flow, which is an extension of the standard RC- or RLCK-parasitic extraction tool flow shown in fig. 15.

(a) 2D substrate netlisting configuration



(b) Connection style of substrate ties

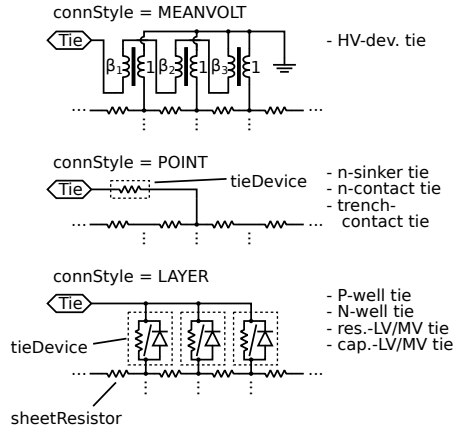


Figure 52: Part (a) Class diagram which describes the 2D substrate netlisting XML configuration file. Part (b) Electrical semantics of the "connStyle" property of the "TieType" class.

These are assembled with each other and with the extracted or layout netlist in the final step #6 (see also fig. 50 (b)). The layout-versus-schematic (LVS) run receives additional information from the 2D substrate netlisting process. This data, which is called *substrate interface overlay* (#3), describes the shapes and the net names of all substrate ties, and it is used by the LVS-runset to connect the semiconductor devices and the metallization to the substrate model¹³. This shows that the LVS-runset must be adapted to the developed substrate tool flow, and it takes an active role in the extraction of the substrate. This deviates from the established methodologies for parasitic extraction¹⁴.

The 2D substrate netlisting (fig. 51) is configured by an XML file. This makes it generic and enables adaption of the developed substrate tool flow to different BCD-technologies. Fig. 52 (a) depicts the objects described by this XML configuration file. An arbitrary number of region types can be defined, each

¹³ Furthermore, in the substrate interface overlay, one can optionally include the net name information of all nodes on the top most mesh layer. Thereby, the capacitances between the metallization and the substrate, which are created by the RC-extraction, are properly connected to substrate model.

¹⁴ The use of LVS to establish the substrate connections allows for a rather clean separation of the 2D and 3D substrate netlisting from the QRC RC-extraction. On the other hand, the layout netlist does not match the schematic netlist, which removes a valuable self-check of the LVS-runset modification. This self-check might be reinstated by additionally transforming the schematic netlist, but this is beyond the scope of this thesis.

of which consists of multiple *mesh layer types*, *tie types* and *vertical connection specifications*. The mesh layer type names a SPICE subcircuit, which is instantiated for each sheet resistor, e.g. see fig. 50 (a). This subcircuit is parameterized a unitless *ratio*, which is computed by applying the 1st-order FEM to the 2D Laplace's equation. The lateral connection specifications define how two regions of a different type shall be interconnected along their boundary line. Specifically, for every vertex that is adjacent to two different region types, the set of *lateral connection specifications* is queried, which may results in multiple applicable specifications. For each applicable specification, the 2D substrate netlisting introduces a point-to-point connection between two corresponding electrical nodes from the specified mesh layers¹⁵. Both, vertical and lateral connections are realized by instantiating SPICE subcircuits, the names of which are given in the XML file, and which are parameterized by an effective area or an effective length, respectively. The tie type defines the mesh layer which is contacted by substrate ties of this type, and the tie type selects a so-called *connection style*. These connection styles are defined in fig. 52 (b): With the mean voltage ("MEANVOLT") and the impedance layer ("LAYER") connection style, connections are introduced to each node, the basis function of which intersects the substrate tie's polygon. Conversely, with the point-contact ("POINT") connection style, a connection is introduced to a new vertex that is added to the 2D mesh at the center of the substrate tie's polygon. The mean voltage connection style effectively imposes a PCD boundary condition onto the targeted mesh layer. The impedance layer connection style¹⁶ connects the targeted mesh layer uniformly by a given conductance or capacitance per area. This conductance or capacitance per area is obtained using a density measure of polygons in the GDS-II layout, e.g. the average count of P-well contacts.

Fig. 53 (a) illustrates the *substrate model geometry* (#1 in fig. 51). It contains, firstly, a set of polygons that define the regions and, secondly, a set of polygons that define the substrate ties. The polygons that define the regions (colored areas in fig. 53 (a)) contain information about the region type and dimension. They must be disjoint and cover the complete IC-layout. The polygons that define the substrate ties (hatched areas in fig. 53 (a)) are associated with a *tie type*, and they must not intersect a region's boundary line. The substrate model geometry is automatically obtained from an IC-layout using Calibre (see fig. 51 (a)). This Calibre script supports special marker layers that allow the user to manually subdivide regions and to alter the regions' dimensions.

¹⁵ This procedure requires that the 2D mesh is free of t-junctions along the boundary line, as stated in sec. 5.2.1.

¹⁶ The impedance layer connection style is not yet implemented.

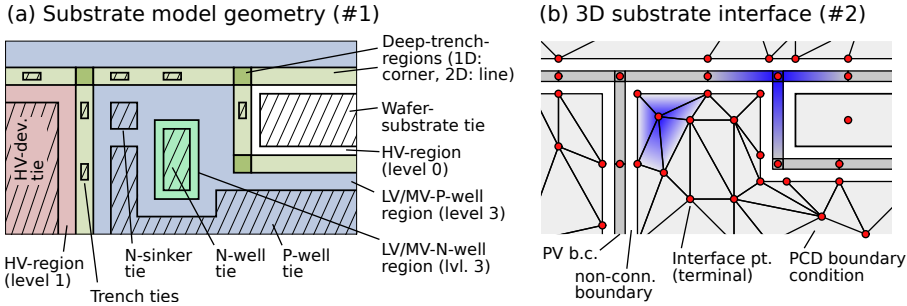


Figure 53: The data stores #1 and #2 from fig. 51: The substrate model geometry and the 3D substrate interface are the inputs of the 2D and the 3D substrate netlisting, respectively. (This drawing only serves as an illustration, and is not based on actual data).

Moreover, as detailed in the following, marker layers also allow to define the *level of detail* of the generated 2D substrate netlist.

HV n-epitaxial pockets (sec. 2.2) are, by default, translated into a single region of type “HV, level 1” (red area). A special marker layer allows the user to request that, instead, *multiple* HV n-epitaxial pockets are unified into a single HV-region of level 0 (white area). This also invokes the deletion of the deep trenches that separate these HV-devices. The user shall mark clusters of small HV-devices using this marker layer¹⁷. This is very important in order to keep the model size within reasonable bounds, but it may lead to an overestimation of resistance between the deep trenches and, firstly, the wafer-substrate and, secondly, the seal-ring (see sec. 6.5.3). Only in HV-regions of level 0, the interface between SPICE device-models and the substrate model is placed at the wafer-substrate surface (fig. 43 (b) from sec. 5.1). Since these regions contain no mesh layers, their dimension must be zero. Each HV-region of level 0 is fully covered by a single substrate tie that connects to the wafer-substrate surface by means of the PCD boundary condition. Hence, all HV-devices that overlap this substrate tie observe this HV-region’s *mean wafer-substrate surface potential*, and their substrate current is evenly distributed over the area of this substrate tie. It is the responsibility of the user to ensure the size of HV-regions of level 0 is sufficiently small, such that this approximation is justified up to the model’s maximum frequency. In HV-regions of level 1, the interface between SPICE device-models and the substrate model is defined at the n-buried layer (fig. 43 (a) from sec. 5.1). The substrate ties that cover these regions are called *HV-device ties* and use the “MEANVOLT” connection style, i.e. they connect the n-buried layer by means of the PCD boundary condition.

¹⁷ This feature is not yet fully implemented, and rather, in the approach of sec. 6.3, small HV-devices are manually deleted from the layout.

LV/MV n-epitaxial pockets are translated into, either, a single region of type “LV/MV, level 2”, or multiple regions of type “LV/MV-P-well, level 3 (or 4)” and “LV/MV-N-well, level 3 (or 4)” (blue and green areas): That is, for a level ≥ 3 , each P- and N-well instantiates a separate region. For level ≤ 3 , bulk connections of individual LV/MV-transistors are not spatially resolved. In contrast, in level 4, substrate ties are added for each device bulk contact and for each transistor finger, but this drastically increases the 2D mesh size¹⁸. Regions of level 3 are fully covered by substrate ties of type “P-well” and “N-well”, respectively, which use “LAYER” connection style, i.e. they introduce a distributed ohmic connection. This conductance per area is determined from the *average density of bulk contacts*. Conversely, in each LV/MV-region of level 2, two different overlapping “LAYER”-style substrate ties, which fully cover its area, are created. The first substrate tie describes its average ohmic connection by p-well bulk contacts. The second substrate tie uniformly distributes the total capacitance the contained n-wells, and it also accounts for the ESR due to n-well bulk contacts.

Deep trenches are represented by regions of type “deep-trench”, as shown in fig. 53 (a). Deep-trench-regions of dimension 0 are created for each *trench corner* (dark green), and dimension 1 is used for each *trench line* (light green). A substrate tie of type “trench-contact” is instantiated for each contact array over deep trenches. In order to keep the model complexity at a reasonable level, the number of trench-contact-ties must be strongly reduced. The current implementation employs a pruning strategy, which, for each deep-trench-region, eliminates a large number of its trench-contact-ties based on a user-controlled minimum distance. The eliminated trench-contact-ties are not simply deleted, but rather groups of trench-contact-ties are simplified by approximately interpreting them as a parallel connection.

Fig. 53 (b) illustrates the 3D substrate interface. It consists of a set of disjoint triangles, quads and concave polygons, which are called *interface facets*, and which form a tiling of the wafer-substrate surface. They are topologically identical to the 2D mesh, but the deep trench’s interface facets are slightly insetted, in order to account for the gap created by the trench oxide¹⁹. The interface facets representing this gap are tagged as *non-connected*. Conversely, the interface facets corresponding to trench or n-epitaxial pockets are tagged with the prescribed voltage (PV), or the prescribed current density (PCD) boundary condition, respectively. The so-called *interface points* are depicted as red dots in fig. 53 (b), and they injectively map to terminals of the 3D

¹⁸ Level 2–3 are not yet implemented. In the approach of sec. 6.3.1, level 2 is emulated by manually deleting all LV/MV-PMOS and LV/MV-NMOS devices.

¹⁹ Moreover, the deep trench’s interface facets are insetted in $-z$ -direction, as shown in fig. 50 (a).

substrate netlist. Each interface point k corresponds to an *interface basis function* $(b_k^{(if)})_{k=1\dots}$. The shaded blue area in fig. 53 (b) visualizes two different interface basis functions (IBFs). The IBFs are continuous piecewise-linear functions that are normalized such that $b_k^{(if)}$ equals 1 at the interface point k . Moreover, they do not extend into the non-connected interface facets, but they densely cover the wafer-substrate surface in the following sense:

$$\sum_k b_k^{(if)} = \chi_{PV} + \chi_{PCD} \quad (75)$$

where χ_{PV} and χ_{PCD} are the set-theoretic indicator function of all PV and PCD interface facets, respectively. The IBFs are used to define of the boundary conditions:

$$\phi(\vec{x}) = \sum_k V_k b_k^{(if)}(\vec{x}) \quad \forall \vec{x} \in PV \quad (76)$$

$$-J(\vec{x}) \cdot \vec{e}_z = \sum_k \frac{I_k}{|b_k^{(if)}|} b_k^{(if)}(\vec{x}) \quad \forall \vec{x} \in PCD \quad (77)$$

where $(V_k)_{k=1\dots}$ and $(I_k)_{k=1\dots}$ are the terminal voltages and currents, respectively, of the 3D substrate netlist, and $|b_k^{(if)}|$ denotes the 1-norm of the IBF.

The 3D substrate netlisting attaches an instance of a SPICE subcircuit at each mesh point on the backside of the wafer-substrate. This subcircuit connects them to the “die-pad” terminal (see fig. 50). Post-hoc, these subcircuits can be translated into capacitors, resistors or short/open-circuits. The proper modeling of the connection between the backside and the die-pad is important for EMC predictions but also rather involved – details are found in sec. 6.3.1.

5.2.3 Performance of Direct and Iterative Linear Solvers when Applied to 3D FEM Models of the Wafer-Substrate

Since the 3D substrate netlist is by far larger than the 2D substrate netlist, it is crucial to understand how the linear solver of the circuit simulator (sec. 2.3.1) performs when applied to the 3D substrate netlist. As described in sec. 2.3.1, in the case of AC simulation or transient simulation, at every frequency point or at every time step, respectively, linear systems of equations are solved:

$$A \cdot x = b \quad (78)$$

where the matrix A is the Jacobian matrix, and its nonzero pattern is inherited from the graph-topology of the circuit if an implicit integration method is

used. Circuit simulators are traditionally based on sparse direct solvers, due to their generality and robustness (sec. 2.3.2).

Sparse direct solvers proceed in three steps: In the first step, the rows and/or columns of A and x are suitably reordered, such that the fill-in in the subsequent LU-decomposition is minimized. This is also known as *symbolic factorization* [40], [43]. An estimate of the worst case asymptotic run time is found in [73]. Since symbolic factorization only depends on the nonzero pattern of A , it is *not* repeated for every time step or every frequency point, respectively [190, Ch. 2]. Hence, in the following, its contribution to the total run time is ignored. But note that the impact of the selected row/column order on the run time of the subsequent LU-decomposition step is not negligible. It can be shown that finding the optimum row/column ordering is an NP-complete problem, and therefore, heuristics are used [43]. Different purpose-specific heuristical row/column ordering schemes have been invented. The class of methods called *minimum degree algorithms*, e.g. the AMD algorithm, had its origins in circuit simulation [43], [190, Ch. 2], [188]. Another notable class of methods are the *nested dissection algorithms*, which have been conceptualized for finite-element problems.²⁰

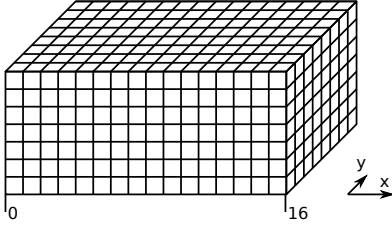
In the second step, an LU-decomposition $A = LU$ is computed using sparse Gaussian elimination, where L and U are sparse matrices as well. This is called *numerical factorization*. The number of non-zero components in L and U that are not present in A are called *fill-in* [40]. Ideally, the fill-in is already determined by the symbolic factorization. However, in practice, the row/column order has to be further modified for numerical reasons, which is also known as *numerical pivoting*. In the third step, the system of equations eq. (78) is solved by left-multiplying b by L^{-1} and then by U^{-1} [40]. This is also called *forwards and backwards substitution*. The run time is proportional to the number of non-zero entries in L and U , and hence this step is much faster than the numerical factorization. In most circuit analyses²¹, the forwards and backwards substitution is only applied to a single vector b , and then the result of the numerical factorization is discarded. Thus, in the following, the run time of the forwards and backwards substitution is neglected.

Fig. 54 (a) shows a 3D mesh, which consists of $N_{\text{box}} = q_x q_y q_z$ boxes of a uniform size. The vertices on the top surface are called *surface terminals*, and their count is denoted by $N_{\text{s.c.}}$. It can be shown that, for $q_x = q_y = q_z = q$, and assuming an optimal row/column ordering, sparse Gaussian elimination

²⁰ Nested dissection algorithms are claimed to be better suited for large-scale 3D problems than minimum degree algorithms [43].

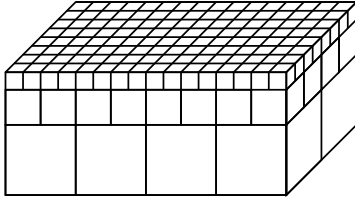
²¹ Transient-, AC- and DC-analysis usually discard the LU-decomposition after a single forwards-/backwards-substitution pass, whereas in the S-parameter-analysis (sec. 2.3.3), the LU-decomposition can be re-used for multiple ports.

(a) Uniform 3D mesh (16 x 8 x 7)



$$N_{s.c.} = (q_x + 1)(q_y + 1)$$

$$N_{\text{box}} = q_x q_y q_z$$

 (b) Log-graded 3D mesh (16 x 8, $\gamma=2$, $L=3$)


$$N_{s.c.} = (q_x + 1)(q_y + 1)$$

$$N_{\text{box}} = \sum_{k=0}^{L-1} q_x q_y \gamma^{-2k} < \frac{q_x q_y}{1 - \gamma^{-2}} \quad (79)$$

Figure 54: Two different 3D mesh topologies for a rectangular parallelepiped that support a regular grid of $N_{s.c.}$ surface terminals. The number of elements, i.e. boxes, is denoted by N_{box} .

requires $\mathcal{O}(q^6)$ floating point operations [43]²². Thus, the run time of a sparse direct solver on an uniform 3D mesh scales very badly with the number of surface terminals, i.e. $\mathcal{O}(N_{s.c.}^3)$. However, it has been observed independently by multiple authors [95], [196] that the 3D mesh of the wafer-substrate can be considerably simplified. Fig. 54 (b) shows a FDM discretization scheme taken from [95]. It consists of a number of layers L , which become successively more thick and more coarse. The ratio between the resolution and the thickness, respectively, of two consecutive layers is called *growth rate* and is denoted by γ . Eq. (79) in fig. 54 (b) follows from the geometric series. It shows that, in a log-graded 3D mesh, the number of non-zero elements in A are roughly proportional to the number of surface terminals. However, as will be shown in the following, this does *not* imply that the direct solver run time is also linear in $N_{s.c.}$.

No theoretical predictions about the optimal run time of direct solvers applied to a log-graded 3D mesh were found in literature. In order to quantify this run time, UMFPACK [40] is applied to two sequences of FDM resistor networks, which are of the kind shown in fig. 54 (a) or (b), respectively. These sequences are parameterized by $N_{s.c.}$, and they conduct a successive refinement of the top surface – that is, in each step by a factor of 2 in both q_x and q_y . In case of the uniform 3D mesh, the refinement step also increases q_z by a factor of 2. Conversely, in the case of the log-graded 3D mesh with $\gamma = 2$,

²² Observe that dense Gaussian elimination needs even $\mathcal{O}(q^9)$ floating point operations.

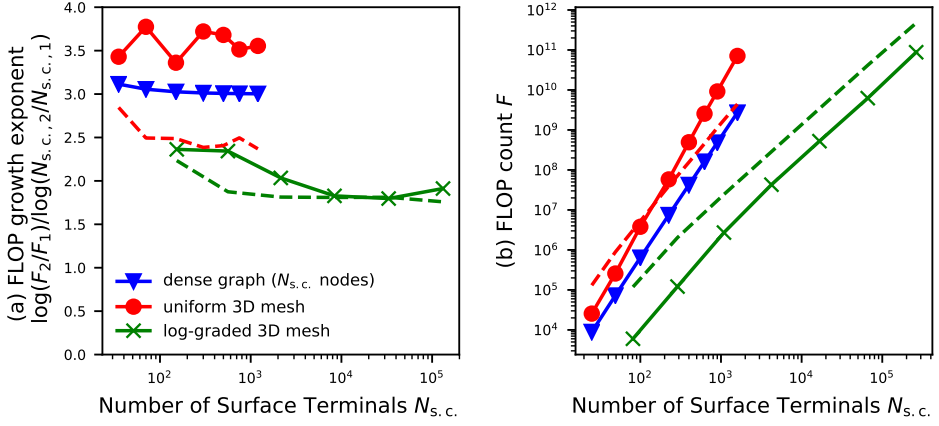


Figure 55: Solid curves: Run time of a sparse direct solver (UMFPACK [40]) applied to Laplace's equation discretized using the FDM (solid red, solid green), and a fully-reduced, dense Y-parameter representation (solid blue), respectively. The dashed curves show the corresponding run time of an iterative linear solver (GMRES [161]). For both solvers, at the top surface, randomized non-zero currents were applied, and the bottom surface of the wafer-substrate was grounded.

the layer count L is increased by 1 in each step. The number of floating point operations (FLOP) performed by the numerical factorization are denoted by F . Now assume two different 3D meshes with surface terminal counts of $N_{s.c.,1}$ and $N_{s.c.,2}$, respectively, have been factorized, and the numerical factorization performed F_1 and F_2 floating point operations, respectively. Then, the *FLOP growth exponent* is defined as $\log(F_2/F_1)/\log(N_{s.c.,2}/N_{s.c.,1})$. In the limit $N_{s.c.} \rightarrow \infty$, it approaches the order of the asymptotic run time.

The solid curves in fig. 55 (a) show the FLOP growth exponent of the direct solver (UMFPACK) as a function of $N_{s.c.}$. The symbolic factorization was performed using the AMD algorithm (UMFPACK_ORDERING_AMD), and the FLOP-count was obtained from the UMFPACK_FLOPS info field returned by `umfpack_di_numeric()`. The solid blue curve represents the run time of UMFPACK applied to a dense Y-parameter representation of the wafer-substrate, i.e. a model where all nodes were eliminated, except for the surface terminals. Here, the FLOP growth exponent approaches 3, as expected for dense Gaussian elimination. The FLOP growth exponent in case of the uniform 3D mesh (solid red curve) is about 3.5, which is slightly higher than expected for an ideal row/column ordering, as described above. The comparison between the solid blue and the solid red curve in fig. 55 (b) shows that direct solvers applied to an uniform 3D mesh are even slower than dense Gaussian elimination applied to a boundary-element discretization. The log-

graded 3D mesh, which is represented by the solid green curve in fig. 55 (a), features a roughly quadratic asymptotic run time in the number of surface terminals²³. This is clearly an improvement over the uniform 3D mesh, but it also shows that even here, direct solvers are *not* very efficient.

In the following, direct solvers will be compared to iterative linear solvers: The iterative linear solver GMRES (see sec. 2.3.1) was applied to the resistor networks described above. The initial guess was a zero vector, i.e. the voltage field was computed from scratch. By the used construction of the matrix A , the results are representative of a Jacobi preconditioner.²⁴ In the estimation of the FLOP-count, multiplications and additions were each associated a weight of 1, which is compatible with the counting method of UMFPACK.

The FLOP growth exponent of GMRES is shown by the dashed curves in fig. 55 (a). The asymptotic run time on the uniform 3D mesh (red curves) is decreased from $\mathcal{O}(N_{\text{s.c.}}^{3.5})$ to $\mathcal{O}(N_{\text{s.c.}}^{2.5})$. This is approximately in line with theory, which predicts an asymptotic run time of $\mathcal{O}(q^{4+\epsilon}) = \mathcal{O}(N_{\text{s.c.}}^{2+\epsilon})$ for the conjugate gradient (CG) algorithm²⁵ [35]. Interestingly, the asymptotic run time of GMRES on the log-graded 3D mesh is similar to UMFPACK (green curves in fig. 55 (a)). Moreover, as shown by the green curves in fig. 55 (b), it appears that GMRES is actually slower in practice. However, note that the actual 3D substrate netlist from sec. 5.2.4 consists of a rather strongly-connected component, which will be called reduced ATL, as well as of a sparse component resembling the log-graded 3D mesh, which will be called residual FEM-mesh. Therefore, it can nevertheless be expected that iterative linear solvers have strong advantages in substrate simulation.

Above, it was observed that iterative linear solvers outperform direct solvers on some mesh topologies, whereas on other topologies, they are on par. This is well-known in theory: For example, on an uniform 2D mesh, direct solvers with an ideal row-ordering need $\mathcal{O}(q^3)$ operations, whereas the worst case asymptotic run time of CG is $\mathcal{O}(q^{3+\epsilon})$, which is essentially the same [35], [43]. In contrast, the respective figures in three dimensions are $\mathcal{O}(q^6)$ and $\mathcal{O}(q^{4+\epsilon})$, respectively [35], [43]. In iterative linear solvers, the exact FLOP count is easily calculated if the number of iterations k is known. For example [161]:

$$F_{\text{GMRES}}^{(\text{mult.})} = (k^2 + 2k)N_{\text{var.}} + kN_{\text{non-zero}} \quad (80)$$

²³ This thesis conjectures that even a run time $\mathcal{O}(N_{\text{s.c.}}^{1.5})$ is possible for the log-graded 3D mesh with an ideal row-ordering, i.e. as in the 2D case. This might be mathematically proven by adapting the seminal proof by Alan George [57].

²⁴ A relative tolerance for the residual of 10^{-5} was used, and it was verified that the voltage fields from both linear solvers were equal roughly up to the fourth decimal place.

²⁵ CG is another Krylov-subspace method, and it is similar to GMRES.

where $F_{\text{GMRES}}^{(\text{mult.})}$ is the number of multiplications performed by GMRES (see sec. 2.3.1), $N_{\text{var.}}$ is the number of columns of A and $N_{\text{non-zero}}$ is the number of non-zero elements in A . It should be expected that k and, hence, also the run time of an iterative linear solver is reduced if the initial guess is better. For example, in transient simulations, the previous time step would be used as an initial guess. This may result in additional performance improvements when switching to an iterative linear solver in transient simulations.

The question that remains to be answered is whether the log-graded 3D mesh is sufficient for substrate simulations, despite it is very coarse at the bottom surface. In fact, it always provides a sufficient resolution for the electric potential ϕ , as will be shown in the following. Firstly, note that solutions of the 3D Laplace's equation in a half-space $z > 0$ can be represented by convolutions of the free space Green's function $G = \rho / (2\pi|\vec{p} - \vec{p}'|)$ with the surface current density [123]. The Hessian of G is denoted by H_G . Its spectral norm is $\|H_G\|_2 = \rho / (\pi|\vec{p} - \vec{p}'|^3)$. By applying Hölder's inequality, one obtains an upper bound for the curvature of the electric potential: $\frac{1}{2}\|H_\phi\|_2 \leq \rho J_{\text{tot.}} / (2\pi z^3)$, where $J_{\text{tot.}}$ is the integral of the absolute surface current density and z is the distance to the surface. From the geometry of the log-graded 3D mesh in fig. 54 (b) it follows that the edge lengths l roughly equal $(\gamma - 1)\gamma^{-1}z$. Using the weak upper bound for tetrahedral meshes in table 2 from [174], one obtains: $\sup(\phi_{\text{interp.}} - \phi) / J_{\text{tot.}} < \text{const.} \cdot z^{-1}$. Thus, despite the element size increases with z , the error does not increase – rather, it even decreases with z .

5.2.4 Detailed Description of the 3D Substrate Netlisting Step: Substrate Extraction using Highly Reduced FEM-Meshes (S-EHRFEM)

In the first step of the 3D substrate netlisting (fig. 51), an irregular three-dimensional tetrahedral mesh is generated. This mesh is simply called 3D mesh in the following. It is illustrated in fig. 56 (a). Because its top surface shall form a proper refinement of the 3D substrate interface (see sec. 5.2.2), a general-purpose tetrahedral mesher must be used: The implementation in this thesis invokes the tool GMSH [58], [59] to construct a quality conformal Delaunay tetrahedralization [160], [173], [177]. The 3D mesh is topologically similar to the log-graded 3D mesh described in sec. 5.2.3. This is achieved by introducing multiple logarithmically-spaced layers of internal vertices, which are termed *seed points* (see fig. 56 (a)).

If the 3D mesh is directly converted into a resistor network, the result is called *initial FEM-netlist*. The initial FEM-netlist might be used as the 3D substrate netlist. However, since the surface of the 3D mesh is a strongly

refined version of the 3D substrate interface, the number of finite elements in the *free tetrahedral layer* (see fig. 56 (a)) is very large. More precisely, the size of the initial FEM-netlist by far exceeds the size of the 2D substrate netlist. Therefore, the use of a coarse mesh for the n-buried layer, which is a kind of RC-reduction (see sec. 5.2.1), is of very limited benefit in itself. It is crucial that, in addition, the 3D substrate netlist is reduced. However, a coarsening of the 3D mesh surface would lead to large errors in shallow current paths, e.g. the current field in the wafer-substrate in the vicinity of deep trenches (sec. 5.2.1).

Therefore, in the following, an alternative approach, termed *substrate extraction using highly-reduced FEM-meshes* (S-EHRFEM), is proposed. This approach is outlined in the following: A thin slab of elements near the top surface, which is called *artificial thin layer* (ATL), is singled out from the 3D mesh, and all inner nodes are eliminated. The ATL comprises the free tetrahedral layer and possibly one or multiple seed layers (see fig. 56 (a)). Due to the log-graded topology, almost all finite elements are located inside the ATL, and hence a strong compression of the ATL will also lead to a strong compression of the 3D substrate netlist. The elimination of the inner nodes is achieved by, firstly, computing the ATL's Y-parameter matrix and, secondly, constructing a generalized π -equivalent circuit from it (see sec. 2.5.1). Each red line in fig. 56 (b) depicts a resistor in this π -equivalent circuit. In addition, the Y-parameter representation of the ATL must be sparsified by deleting resistors that form long range connections. For example, the dashed red line in fig. 56 (b) is a resistor that is deleted from the π -equivalent circuit. The elimination of the ATL's inner nodes and its sparsification is called the *ATL-reduction*. Sparsification is an integral part of the ATL-reduction: Without

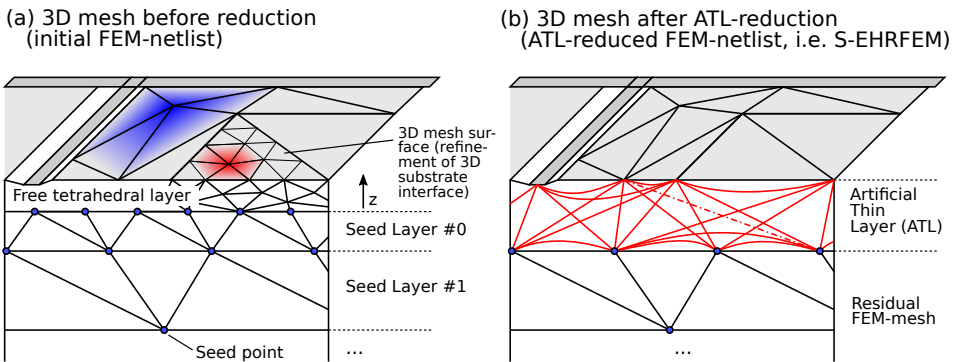


Figure 56: (a): 3D mesh of the wafer-substrate. An IBF is shown in blue and an MPBF is shown in red. This drawing only serves as an illustration, and is not based on actual data. (b): The result of applying S-EHRFEM to this 3D mesh; the red lines depict resistors.

sparsification, the major part of the 3D substrate netlist would consist of negligibly small resistors because every pair of vertices on the ATL's surface would be connected. The part of the model that is left unmodified by ATL-reduction is called *residual FEM-mesh* (fig. 56 (b)). The resistor network that comprises both, the residual FEM-mesh and the reduced ATL, will be called *ATL-reduced FEM-netlist*. In S-EHRFEM, this ATL-reduced FEM-netlist is used as the 3D substrate netlist.

The simplified description above raises a number of questions: Firstly, while replacing the ATL by a generalized π -equivalent circuit is an equivalence transform, the sparsification is merely an approximation: It must be clarified why the deletion of long range connections is acceptable, and how the sparsification should be performed. Secondly, while S-EHRFEM trivially reduces the node count, it is not obvious that it also reduces the resistor count: It must be shown that the ATL-reduced FEM-netlist size is smaller than both, the size of the initial FEM-netlist and the resistor count in a fully-reduced, dense Y-parameter representation. Third, the ATL height is a new variable, which must be fixed: It must be determined how the ATL should be dimensioned to achieve maximum reduction.

Theoretical analysis of the Y-parameters of an infinite thin layer The following paragraphs derive an approximate expression for the Y-parameter matrix of an infinite thin layer that is contacted via surface terminals on the top surface. An *infinite thin layer* shall denote a volume of space $-H \leq z < 0$ where the electric field potential $\phi(x, y, z)$ is defined as solution of Laplace's equation and is subject to the prescribed-voltage (Dirichlet) boundary condition at the *top surface* $z = 0$ and at the *bottom surface* $z = -H$. Furthermore, assume a sequence of basis functions $B_i(x, y)$, the domain of which are bounded subsets of $\mathbb{R}^2$. These basis functions are interpreted as discrete *surface terminals* on the top surface.

To obtain the Y-parameter $Y_{i,j}$ between the basis functions B_i and B_j , the current density in Z-direction is integrated over B_j :

$$Y_{i,j} = \frac{1}{V_0} \iint_{-\infty}^{\infty} dx dy B_j(x, y) \vec{e}_z \cdot \vec{J}(x, y, 0) \quad (81)$$

where $\vec{J} = -\rho^{-1} \nabla \phi$ is the current density field. Furthermore, the boundary is excited at B_i , which is realized by the following Dirichlet boundary conditions:

$$\phi(x, y, 0) = V_0 B_i(x, y) \quad \phi(x, y, -H) = 0 \quad (82)$$

In order to solve eqs. (81,82), the Green's function of the interior Dirichlet problem on $\Omega = \mathbb{R} \times \mathbb{R} \times [-H, 0]$, which is denoted by $G(x, y, z; x', y', z')$, is

exploited. As pointed out by [129], an closed-form solution is not known, but $G(x, y, z; x', y', z')$ can be expressed as an infinite sum using the method of images:

$$G(x, y, z; x', y', z') = \frac{1}{4\pi} \sum_{k=-\infty}^{\infty} \left(\frac{1}{|\vec{p} - \vec{p}'_{k,+}|} - \frac{1}{|\vec{p} - \vec{p}'_{k,-}|} \right) \quad (83)$$

$$\vec{p}'_{k,+} := (x', y', z' + 2kH) \quad \vec{p}'_{k,-} := (x', y', -z' + 2kH)$$

Now, for a point source $\vec{p}' = (x', y', z')$ infinitesimally close to the top surface, i.e. $z' = -\epsilon$, the Green's function from eq. (83) simplifies to:

$$\lim_{\epsilon \rightarrow 0} \frac{1}{\epsilon} G(\vec{p}; \vec{p}', \epsilon) = K(\vec{p}; \vec{p}') \quad K(\vec{p}; \vec{p}') := -\frac{1}{2\pi} \sum_{k=-\infty}^{\infty} \frac{\vec{e}_z \cdot (\vec{p} - \vec{p}'_{k,+})}{|\vec{p} - \vec{p}'_{k,+}|^3} \quad (84)$$

Observe that $K(\vec{p}; \vec{p}')$ can be understood as an infinite sum over mirror images of a double-layer potential [107]. It can be shown that:

$$\lim_{\epsilon \rightarrow 0^+} K(x, y, z \mp \epsilon; x', y') = \pm \delta(x - x') \delta(y - y') \quad (85)$$

This can be proven by integrating both sides over an infinitesimal disc. Eq. (85) entails a representation of $\phi(x, y, z)$ for $(x, y, z) \in \Omega \setminus \partial\Omega$ as a convolution of the top boundary condition by $K(\vec{p}, \vec{p}')$:

$$\phi(x, y, z) = \iint_{-\infty}^{\infty} dx' dy' K(x, y, z; x', y') \phi(x', y', 0) \quad (86)$$

Using the current-voltage relation $\vec{J} = -\frac{1}{\rho} \nabla \phi$ and eqs. (81,84,82,86), one obtains:

$$Y_{i,j} = -\frac{1}{\rho} \iiint_{-\infty}^{\infty} dx dy dx' dy' B_j(x, y) B_i(x', y') \frac{\partial}{\partial z} K(x, y, z; x', y') \Big|_{z=0} \quad (87)$$

For large distances, $\partial/\partial z K(x, y, z; x', y')|_{z=0}$ can be regarded as constant within this integral. By this means, following approximation is obtained:

$$Y_{i,j} \approx -\frac{A_i A_j}{2\pi \rho H^3} \sum_{k=-\infty}^{\infty} \left(\frac{1}{|\vec{d}'_k|^3} - \frac{12k^2}{|\vec{d}'_k|^5} \right) \quad (88)$$

$$\vec{d}'_k := (\vec{p} - \vec{p}')/H + 2k\vec{e}_z$$

where $A_i := \iint dx dy B_i(x, y)$ and A_j are the *effective areas* of B_i and B_j , respectively, and $\vec{p}$ and $\vec{p}'$ are some representative points inside the domain of B_i and B_j , respectively. By numerically evaluating the rather slowly converging sum in eq. (88) with sufficiently many, e.g. $2 \cdot 10^7 + 1$, terms, it was empirically found that the following function fits the data very well:

$$Y_{i,j} \approx -\frac{C_1 A_i A_j}{2\pi\rho H^3} \frac{e^{-C_2\gamma}}{\gamma} \quad \gamma := \frac{|\vec{p} - \vec{p}'|}{H} \quad (89)$$

with $C_1 \approx 14.40$ and $C_2 \approx 2.997$. The relative deviation of eq. (89) from eq. (88) was below 15% for $H/2 < |\vec{p} - \vec{p}'| < 8H$.

$|\vec{p} - \vec{p}'|$ can be understood as the (x, y) -distance between two vertices on the top or bottom surface of the ATL, and H can be understood as the ATL height. After the inner nodes of the ATL have been eliminated, each pair of adjacent vertices are connected by resistors. Eq. (89) describes the distance asymptote of these resistors²⁶. It shows that, for $\gamma := |\vec{p} - \vec{p}'|/H \gg 1$, these resistors are very large and increase roughly exponentially with the distance. Therefore, deleting long range connections from the ATL is well justified. Moreover, a suitable and general criterion is to delete all resistors with $\gamma > \hat{\gamma}$, where $\hat{\gamma}$ is a fixed unitless threshold that depends on the accuracy target.

Note that eq. (89) as well applies in the limit of small surface terminals, i.e. for $\sqrt{A_i} \ll H$. Therefore, it can also be used to analyze methods that directly sparsify the Y-parameter matrix of the whole wafer-substrate using a cutoff distance [180], [189]. In this case, H must be understood as the full height of the wafer-substrate. Eq. (89) implies that, in general, resistors with $\gamma \ll 1$ must *not* be deleted. This strongly limits the usefulness of these methods because the resistor count then grows quadratically, and the direct solver run time even grows with the third power in $N_{s.c.}$ when the surface terminals are downsized (sec. 5.2.3).

Conversely, in S-EHRFEM, a downsizing of the 3D substrate interface, i.e. the 2D mesh²⁷, can be countered by shrinking the ATL height H proportionally. This shows that the ATL height must be fixed to some constant multiple of a *mean feature size* of the 2D mesh. A quantity σ may be called mean feature size if it is roughly proportional to the diameter of the IBFs, i.e. $\sqrt{A_i}$. The optimum proportionality factor will be determined empirically in sec. 5.2.5.

²⁶ Strictly speaking, it does not apply to resistors connecting the top with the bottom surface. Their asymptote should be similar.

²⁷ For example, the 2D mesh must be downsized if the maximum frequency of the substrate model is increased.

(a) Voltage interpolator realizations

... and (b) -circuit transformations

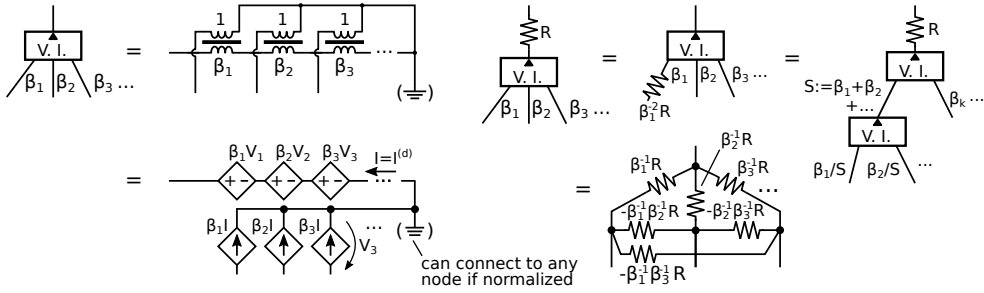


Figure 57: (a): Realizations of the voltage interpolator defined by eqs. (92) in terms of transformers or controlled sources. (b): Equivalent transformations of a normalized ($\sum_k \beta_k = 1$) voltage interpolator with a resistor in series.

A prototypical implementation of S-EHRFEM The surface of the 3D mesh shall be denoted by S . In addition to the interface basis functions (sec. 5.2.2), another sequence of piecewise-linear basis functions is defined on S – the so-called *mesh point basis functions* $(b_k^{(\text{mp})})_{k=1\dots}$. The mesh point basis functions (MPBFs) are depicted by the red gradient in fig. 56, whereas the blue gradient shows the interface basis functions (IBFs). The IBFs reflect the interface facets, whereas the MPBFs describe the refined surface of the 3D mesh. They are also normalized as in eq. (75).

The *mesh-interface coupling matrix* M , which is needed for the implementation of the boundary conditions, is defined as follows:

$$M_{ij} = \iint_S d^2p \, b_i^{(\text{if})}(\vec{p}) \, b_j^{(\text{mp})}(\vec{p}) \quad (90)$$

The mesh-interface coupling matrix is sparse, and its entries are easily calculated by integrating piecewise quadratic functions over triangles. From the normalization condition in eq. (75) follows that:

$$\sum_i M_{ij} = A_j^{(\text{mp})} \quad \sum_j M_{ij} = A_i^{(\text{if})} \quad (91)$$

where $A_k^{(\text{mp})} := \iint_S d^2p \, b_k^{(\text{mp})}(\vec{p})$ and $A_k^{(\text{if})} := \iint_S d^2p \, b_k^{(\text{if})}(\vec{p})$ are the effective areas of the IBFs and the MPBFs, respectively.

In the following, a special linear device, which is called *voltage interpolator* within this thesis, is introduced. The voltage interpolator has a single *driving*

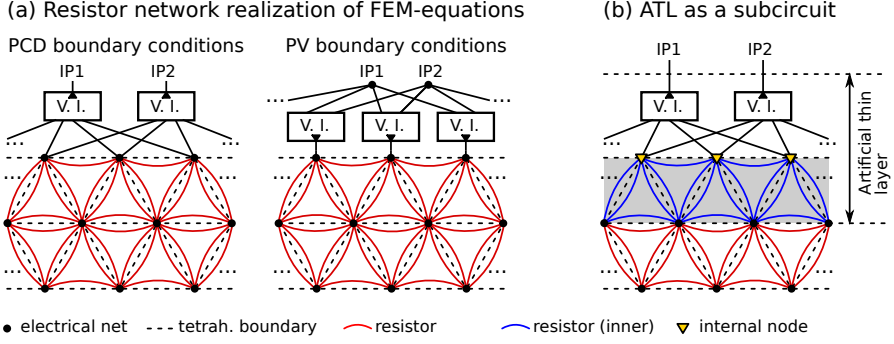


Figure 58: (a): Circuit representation of the FEM applied to Laplace's equation (resistors) and realization of PCD and PV boundary conditions (voltage interpolators connected to interface points IP1 and IP2). Dashed triangles represent tetrahedra. (b): The group of tetrahedra s_{atl} (gray) and the subcircuit X_{atl} (internal nodes, inner resistors and voltage interpolators).

terminals and an arbitrary number of *receiving terminals*. Each receiving terminal k is linked to a coefficient β_k . Its defining equations are as follows:

$$V^{(d)} = \sum_k \beta_k V_k^{(r)} \quad I_k^{(r)} = -\beta_k I^{(d)} \quad (92)$$

where $V^{(d)}$ is the ground-referred voltage at the *driving terminal*, $V_k^{(r)}$ is the ground-referred voltage at the k -th *receiving terminal*, $I_k^{(r)}$ is the current leaving the k -th receiving terminal, and $I^{(d)}$ is the current leaving the driving terminal. The driving terminal is graphically denoted by a small arrow. Fig. 57 (a) shows that the voltage interpolator is equivalent to a certain series connection of transformers. Hence, it follows that the voltage interpolator is reciprocal and passive. Given that the normalization condition $\sum_k \beta_k = 1$ holds, it is also charge-conserving and reference-independent. Fig. 57 (b) shows some neat circuit transformations and resistor equivalent circuits.

An electrical netlist, which is equivalent to the discretization of Laplace's equation on the 3D mesh, is created. This netlist is called *initial FEM-netlist*. It is illustrated by fig. 58 (a). In this construction, vertices in the 3D mesh are converted into electrical nodes. These electrical nodes are called *mesh points* in the following. Furthermore, for each tetrahedron t , and for each edge (i, j) adjacent to t , a resistor $R_{i,j}^{(t)}$ is created:

$$R_{i,j}^{(t)} = -\frac{\rho}{V^{(t)} \vec{G}_i^{(t)} \cdot \vec{G}_j^{(t)}} \quad (93)$$

1: **procedure** HEURISTIC_ATL

- 2: $\sigma \leftarrow$ A continuous function on the wafer-substrate top surface, that is locally roughly 1/2 of the interface facets' shortest edge length
- 3: $s_{\text{pts.}} \leftarrow$ A point set on the connected wafer-substrate surface, such that each triangle on the top surface contains at least one $p \in s_{\text{pts.}}$
- 4: $s_{\text{sph.}} \leftarrow$ The union of all spheres around $p \in s_{\text{pts.}}$ with radius $F_{\text{tl}} \cdot \sigma(p)$
- 5: $s_{\text{seed}} \leftarrow$ Set of all mesh points inside $s_{\text{sph.}}$ (Use spatial tree structures for an efficient implementation)
- 6: $s_{\text{atl}} \leftarrow$ Set of all tetrahedra adjacent to some $p \in s_{\text{seed}}$
- 7: **return** s_{atl}

Figure 59: Algorithm that heuristically groups tetrahedra into s_{atl} , which is an ATL of varying height. The empirical constant F_{tl} is called *heuristic thin layer factor*.

where $V^{(t)}$ is the volume of t and $\vec{G}_i^{(t)}$ is the gradient vector of a first order FEM basis function of vertex i inside tetrahedron t . Eq. (93) is derived by equating the stiffness matrix [47] with the linear system of equations in the MNA (sec. 2.3.1). These resistors are depicted by red lines in fig. 58 (a). The association of these resistors to their defining tetrahedron is denoted by the function τ , i.e. $\tau(R_{i,j}^{(t)}) = t$. Observe that each edge e is associated with multiple parallel resistors, i.e. one resistor from each adjacent tetrahedron. This is called the *resistor bundle* of e .

The boundary conditions are realized using the voltage interpolators defined above. Fig. 58 (a) shows how voltage interpolators must be connected to the resistor network in order to realize PCD or PV boundary conditions: For each mesh point j on the surface part that is subject to PV boundary conditions, one voltage interpolator is created. This voltage interpolator is assigned $\beta_k = M_{k,j} / A_j^{(\text{mp})}$ and links the mesh point j to all interface points k that have an overlapping IBF. Conversely, for each interface point i that is subject to PCD boundary conditions, one voltage interpolator is created with $\beta_k = M_{i,k} / A_i^{(\text{ip})}$. It links the interface point i to all mesh points k that have an overlapping MPBF. The reader can convince himself using eq. (92) that this construction is correct and realizes eqs. (76,77). Note that from eq. (91) it follows that these voltage interpolators are properly normalized.

In the prototypical implementation, the ATL is constructed from a group of tetrahedra, which will be called s_{atl} : A heuristic is used to single out s_{atl} from the *initial FEM-netlist*. This heuristic algorithm is shown in fig. 59. The ATL height H depends on x and y . Specifically, it is locally proportional to an estimate of a *mean feature size* σ . The location-dependence of H is motivated as follows: In sec. 5.2.2, it was recommended that the user should manually

reduce the level of detail in areas that contain a large number of small HV-devices. Despite this, there may also be use cases in which each HV-device should have a separate substrate contact. In this case, the resolution of the 2D mesh is relatively increased in these areas. Moreover, as derived above, the ATL height should be a constant multiple of the mean feature size. Therefore, the ATL height should be locally reduced in areas that contain a large number of small HV-devices.

The set of tetrahedra that forms the ATL s_{atl} , which is depicted by the gray area in fig. 58 (b), gives rise to a subcircuit of the initial FEM-netlist. This subcircuit is denoted by X_{atl} . The internal nodes of X_{atl} are the set of mesh points which are not adjacent to any tetrahedron $t \notin s_{\text{atl}}$. These are depicted by the yellow triangles in fig. 58 (b). Moreover, all resistors x with $\tau(x) \in s_{\text{atl}}$ (depicted by blue lines) and all voltage interpolators are a part of X_{atl} . Observe that resistor bundles at the boundary of the ATL are divided by this construction, and only a part of these resistors are contained in X_{atl} . Terminals of X_{atl} consist of, firstly, the set of interface points, and secondly, the set of mesh points on the boundary of the volume formed from s_{atl} .

The prototypical implementation proceeds by computing the dense Y-parameter matrix of X_{atl} , which is denoted by Y_{ij} : A linear system of equations is obtained by applying the MNA (sec. 2.3.1) to X_{atl} . One at a time, voltage excitations are applied to each terminal, and the resulting system of equations is repeatedly solved using UMFPACK [40]. Since only the right hand side vector b (sec. 5.2.3) changes in each iteration, the result of the symbolical *and* the numerical factorization can be reused. In contrast, the forwards and backwards substitution must be performed in each iteration. From the discussion in sec. 5.2.3 it follows that the asymptotic run time is roughly quadratic in the number of interface points ²⁸.

In the following, r_{ij} refers to a two-dimensional distance metric between terminals of X_{atl} . It can be equated with the Euclidean (x, y) -distance. As described above, a general criterion for the sparsification is to set all components Y_{ij} to zero, for which $r_{ij} > H\hat{\gamma}$. The quantity $R_c := H\hat{\gamma}$ is called *cutoff distance*. However, the cutoff distance depends on the ATL height H , which is not constant. In order to spare the difficulties of heuristically estimating an average local ATL height, the definition of the cutoff distance R_c will be

²⁸ Note that it is crucial to reuse the result of the numerical factorization because otherwise the asymptotic run time would be cubic. Moreover here, switching to iterative linear solvers would *worsen* the asymptotic run time because the system would then be solved for each interface point from scratch.

reformulated in terms of Y_{ij} and r_{ij} only. To that end, the *residual conductance* $Q_i(R)$ is defined as follows:

$$Q_i(R) = \sum_{\forall j: \gamma > R/H} |Y_{ij}| \quad (94)$$

Note that with $\gamma = r_{ij}/H$, the ATL height H cancels out, and thus $Q_i(R)$ can be calculated without the need to estimate H . Now substitute the theoretical estimate for Y_{ij} from eq. (89), and then assign $A_j = 2\pi r dr$ and $\gamma = r/H$. Thereby, the sum in eq. (94) can be approximately predicted by integration in polar coordinates:

$$Q_i(R) \approx \frac{C_1 A_i}{2\pi \rho H^3} \int_R^\infty \frac{e^{-C_2 r/H}}{r/H} 2\pi r dr = \frac{C_1 A_i}{C_2 \rho H} e^{-C_2 R/H} \quad (95)$$

This equation is a theoretical estimate of the asymptote of $Q_i(R)$ for large R . Given a terminal i , it is postulated to determine the cutoff distance as the minimum value for R_c that satisfies the following condition:

$$\kappa^{2\varphi_2-2} Q_i(\varphi_2 R_c) \leq \kappa^{2\varphi_1-2} Q_i(\varphi_1 R_c) \quad (96)$$

where κ is called *pruning threshold* and $\varphi_1 < \varphi_2$ are called *lookahead factors*. For example, with $\kappa = 20$ and $\varphi = (\frac{1}{2}, 1)$, eq. (96) implies that the residual conductance at R_c should be smaller than the residual conductance at $R_c/2$ by a factor of 20. By substituting eq. (95) into eq. (96), it follows that:

$$R_c \approx H \frac{2 \log \kappa}{C_2} \quad (97)$$

Therefore, the criterion eq. (96) effectively realizes a cutoff distance R_c that is proportional to H , as it should be. Moreover, eq. (97) gives the relation between $\hat{\gamma}$ and κ , and it shows that the lookahead factors φ_k can be chosen independently²⁹.

It has been argued above that the ATL should have a variable height. In some cases, it might even be beneficial to use an ATL with a curved surface. For example, in BCD-technologies, in which the deep trenches cut very deeply into the wafer-substrate, the optimal ATL might be folded around these cutouts. It is not very difficult to generalize the procedure HEURISTIC_ATL (fig. 59) to this case. However, the sparsification method that is described above is not

²⁹ The choice of φ_k depends on stability considerations of the algorithm. In practice, it was found that $\varphi_1 = 1/2$, $\varphi_2 = 1$ works well. A more conservative variant introduces a third lookahead factor into eq. (96), and assigns e.g. $\varphi_1 = 1/2$, $\varphi_2 = 1$ and $\varphi_3 = 2$.

extended as easily because the Euclidean (x, y) -distance r_{ij} must be replaced by a manifold distance. Fortunately, this can be circumvented by replacing r_{ij} by the effective distance r_{ij}^{eff} , which is defined as follows:

$$r_{ij}^{\text{eff}} := \sqrt{\frac{1}{2\pi} \sum_j A_{L_i(j)}} \quad (98)$$

where A_i is an *effective area* of the i -th terminal of X_{atl} , and L_i is a permutation of the terminals that approximates ascending sorting by r_{ij} . In the prototypical implementation, L_i is a descending sorting of the terminals j by $|Y_{ij}| / (A_i A_j)$, which is motivated by eq. (89). Eq. (98) exploits the effective areas, which are easily computed as integrals over the two-dimensional basis functions, e.g. IBFs. On the ATL's top surface, they can be equated with $A_k^{(\text{if})}$.

The prototypical implementation sparsifies Y_{ij} with a cutoff distance obtained using eq. (96). It uses the effective distance from eq. (98) as distance metric. Afterwards, it deletes the subcircuit X_{atl} – i.e. all voltage interpolators, inner resistors and internal nodes of X_{atl} are deleted from the initial FEM-netlist. In exchange, a generalized π -equivalent of the sparsified Y_{ij} is created, i.e. fig. 7 (a). Note that this construction requires that the Y -parameters Y_{ij} are reciprocal and reference-independent, which is guaranteed by the fact that each normalized voltage interpolator is reciprocal and reference-independent. Finally, all parallel resistors are merged, whereby the resistor bundles collapse. The result is the *ATL-reduced FEM-netlist*.

Efficiency and stability of the 3D substrate netlist in SPICE-simulation

In order to convert a circuit into linear equations, SPICE-like simulators typically use the MNA (sec. 2.3.1). The 3D substrate netlist consists a resistor network, and, if the ATL-reduction is disabled, also voltage interpolators are present. If the MNA is applied to the 3D substrate netlist, in the resistor network part, each variable corresponds exactly to one mesh point. Therefore, the coding of the resistor network into equations is as compact as in dedicated FEM-software, and the resulting coefficient matrix is exactly equal the FEM stiffness matrix. However, if the ATL-reduction is disabled, i.e. if the initial FEM-netlist is directly passed to a SPICE-like simulator, additional variables might be introduced for the voltage interpolators. Specifically, if they are represented by controlled sources as shown in fig. 57 (a), one variable is added for each receiving terminal. This is remedied by grouping multiple voltage controlled voltage sources (VCVS) into a single PCVS-element.

It is easily shown that the initial FEM-netlist and the ATL-reduced FEM-netlist are reciprocal, charge-conserving and reference-independent: Namely,

all constituents, i.e. the resistors and the normalized voltage interpolators, are reciprocal, charge-conserving and reference-independent. These are important quality characteristics of the substrate model (see sec. 2.3.2). To ensure simulator stability in transient simulation, passivity is required in addition, as explained in sec. 2.3.2 and sec. 2.4.2. However, the initial FEM-netlist frequently contains negative resistors, which arise from eq. (93). Those may *not* be clamped to zero, as they are indeed an essential part of the substrate model. Furthermore, additional negative resistors may be introduced when voltage interpolators are eliminated, which is exemplified by fig. 57 (b). However, as will be shown in the following, the 3D substrate netlist is *indeed expected to be passive*, despite the unavoidable presence of negative resistors: If the 3D mesh's tetrahedra are of sufficient quality, it can be shown that the eigenvalues of the FEM stiffness matrix are greater than zero [174]. Therefore, the resistor network of the initial FEM-netlist should be passive (see sec. 2.4.1). Moreover, since voltage interpolators are passive, the ATL-reduced FEM-netlist is passive as well, assuming that the error introduced by the ATL-reduction is sufficiently small.

5.2.5 Evaluation of S-EHRFEM

The prototypical implementation of S-EHRFEM, which was described in sec. 5.2.4, is evaluated using a 7×7 grid of rectangular HV-devices. These HV-devices are separated by deep trenches. Fig. 60 (a) shows the 3D substrate interface of a single grid cell in the 7×7 grid. Conversely, fig. 60 (b) shows the surface of the 3D mesh of this grid cell. The surface of the 3D mesh has much higher resolution than the 3D substrate interface. The cross section of the 3D mesh along A–A is depicted in fig. 60 (c) and (d). The blue bar visualizes the size of a grid cell. It can be seen that the die thickness H_{die} is roughly three times larger than the size of a grid cell.

The boundary between the ATL (gray) and the residual FEM-mesh (black) is depicted by the red line in fig. 60 (c) and (d). The ATL height in fig. 60 (c) is larger than in (b) because F_{tl} was increased from 2.0 to 3.5. Observe that, despite the ATL height is roughly constant, the bottom surface of the ATL is rather ragged³⁰. This is due to the fact that HEURISTIC_ATL (fig. 59) creates the ATL by simply grouping randomly arranged tetrahedra.

S-EHRFEM was applied to the 7×7 grid for three different pruning thresholds κ , and the heuristic thin layer factor F_{tl} was swept. The size of the 3D substrate netlist is quantified by the sum of the node count and the resistor

³⁰ Note that the some angles of the depicted polygons are very small. This does *not* imply that the corresponding tetrahedra are degenerate: In fact, a non-degenerate tetrahedron can have a cross-sectional polygon with arbitrary small angles.

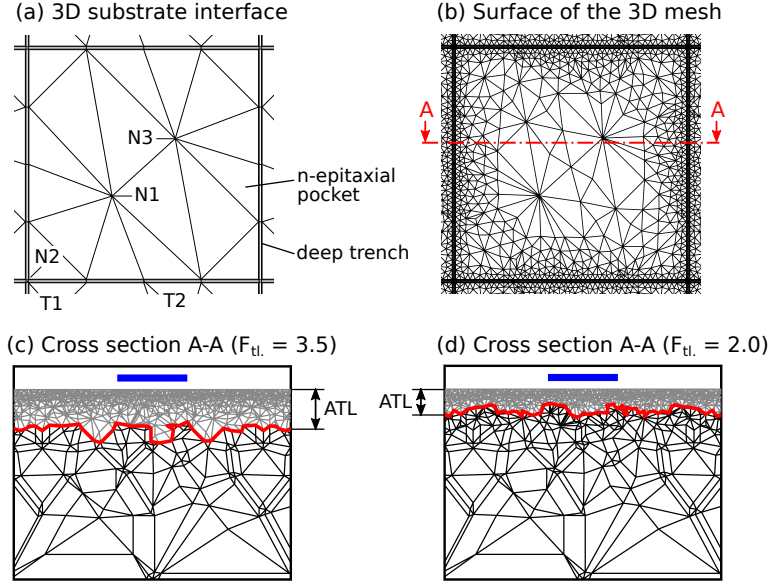


Figure 60: The 3D substrate interface and the 3D mesh in the 7×7 grid of rectangular HV-devices. The part shown in (a) and (b) corresponds to the grid cell # (5, 5). The height of the cross sections in (c) and (d) equals the die thickness.

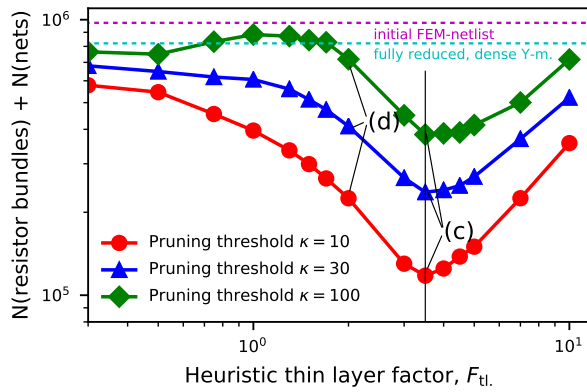


Figure 61: Size of the 3D substrate netlist as a function of the heuristic thin layer factor F_{tl} in the 7×7 grid of rectangular HV-devices. Lookahead factors of $\varphi = (\frac{1}{2}, 1)$ were used. The labels (d) and (c) refer to fig. 60.

	nodes		resistor bundles			V. I.
	term.	mesh pt.	$T \leftrightarrow T$	$T \leftrightarrow B$	$B \leftrightarrow B +$ (residual) FEM *	
initial FEM-netlist	1380	144674	0	0	827990	74884
S-EHRFEM $\kappa = 30$	1380	1590	70757	114287	48660	0
S-EHRFEM $\kappa = 10$	1380	1590	37426	53668	23780	0
fully red., dense Y	1380	0	806377	0	0	0
in the 7×7 grid of rectangular HV-devices with $\varphi = (\frac{1}{2}, 1)$ and $F_{tl} = 3.5$. * count of resistor bundles connecting mesh points. They arise from resistors inter- connecting bottom terminals of X_{atl} if ATL-reduction is enabled, and from the (residual) FEM-mesh.						

Table 7: Comparison between reduced netlists to the initial FEM-netlist in terms of size.

bundle count. The result is shown in fig. 6l. Using this data it is determined empirically that the optimum is at $F_{tl} = 3.5$, regardless of the selected pruning threshold κ . In addition, a 3D substrate netlist was obtained in which *all* mesh points in the initial FEM-netlist were eliminated and sparsification was disabled. This netlist is called the *fully-reduced, dense Y-parameter representation*, and its size is depicted by the dashed cyan line in fig. 6l. The curves impressively demonstrate that, at $F_{tl} = 3.5$, the ATL-reduced FEM-netlists are smaller than, both, the initial FEM-netlist and the fully-reduced, dense Y-parameter representation.

Table 7 further breaks down the netlist sizes at the optimum heuristic thin layer factor $F_{tl} = 3.5$. The number of nodes can be broken down into the number of terminals, i.e. interface points, and the number of mesh points. Observe that the number of mesh points that remain in the residual FEM mesh is only slightly larger than the number of interface points. $T \leftrightarrow T$ denotes resistors in the reduced ATL between top surface vertices, i.e. between interface points. Conversely, $T \leftrightarrow B$ denotes the resistors in the reduced ATL between the top surface and the bottom surface. It can be seen that the total resistor count in the ATL-reduced FEM-netlists is dominated by resistors directly connecting to interface points, i.e. $T \leftrightarrow T$ plus $T \leftrightarrow B$. Using the data in table 7, it is calculated that the node reduction factor is 49, and, for $\kappa = 10$, the resistor reduction factor is 7.2.³¹

³¹ At least for GMRES, the node reduction factor is more important: Not only is it thought to reduce the effective resolution, and hence the iteration count, but also the node count contributes more to the overall run time per iteration, as can be seen after dividing eq. (80) by k .

	(N3, N2-2) *	(N3, N2-1) *	(N3, N2)	(N3, T2)	(T1, T2)
S-EHRFEM $\kappa = 30$	0.85%	2.51%	0.06%	0.05%	0.05%
S-EHRFEM $\kappa = 10$	1.96%	9.25%	1.34%	0.10%	0.31%
in the 7×7 grid of rectangular HV-devices with $\varphi = (\frac{1}{2}, 1)$ and $F_{\text{H}} = 3.5$. The labels N3,N2,T1 and T2 refer to the interface points in fig. 60 (a). * In this nomenclature, N2 is located at $\#(5 - k, 5)$ in the 7×7 grid, whereas N2-k is located at $\#(5 - k, 5)$.					

Table 8: Relative errors of Y-parameters of the 3D substrate netlist introduced by the ATL-reduction.

In order to evaluate the errors introduced by the ATL-reduction, the Y-parameters of 3D substrate netlists were calculated using DC-simulations. The entries in table 8 show the relative deviation between the ATL-reduced FEM-netlists and the initial FEM-netlist. The worst case deviations is 2.5% for $\kappa = 30$, whereas for $\kappa = 10$ all deviations are below 9%. This is very convincing, and suggests that $\kappa = 10$ is sufficiently precise.³²

The creation of the 2D mesh is controlled by a *maximum triangle area* and a *maximum edge length* in regions of dimension 2 and dimension 1, respectively. In an ideal hexagonal tiling, the effective IBF area $|b_k^{(\text{if})}|$ equals twice the triangle area. Thus, in this thesis, the triangle area is limited to $A_c/2$, with A_c from eq. (61)³³. Furthermore, the mesh size should be sufficiently small, such that using the PCD boundary condition on the wafer-substrate surface is justified (see sec. 5.2.1). To evaluate this, test structures akin to fig. 44 from sec. 5.1.1 were simulated. The results, which are summarized in [44], suggest that a maximum triangle area of $A_{\text{max,nepi}} = H_{\text{die}}^2$ in n-epitaxial pockets, and a maximum edge length of $l_{\text{max,tr}} = H_{\text{die}}/2$ is sufficient. For good measure, in this thesis, $A_{\text{max,nepi}}$ will be set to $H_{\text{die}}^2/4$ and $l_{\text{max,tr}} = H_{\text{die}}/3$.

Sec. 6.3 will apply the prototypical implementation of S-EHRFEM to an actual IC-layout. Fig. 62 (a), zooms into a small part of this layout, and depicts the 3D substrate interface. Fig. 62 (b) shows a full-height cross-section of the 3D mesh along B-B. The blue bar in fig. 62 (b) represents the clipping shown in (a). In fig. 62 (a), it can be seen that the size of the 2D mesh increases from left to right. Likewise, in fig. 62 (b), it can be seen that the ATL increases in height from the left end of the blue bar to its right end. This shows that

³² In both cases, the largest relative error was observed for (N3, N2+1). This suggests that interface point pairs spaced approximately R_c apart have Y-parameters with the worst accuracy.

³³ This ignores triple-well structures, e.g. N-wells inside the logic implant, as well as LV-devices inside P-wells. If these are to be described accurately, the mesh ought to be further refined.

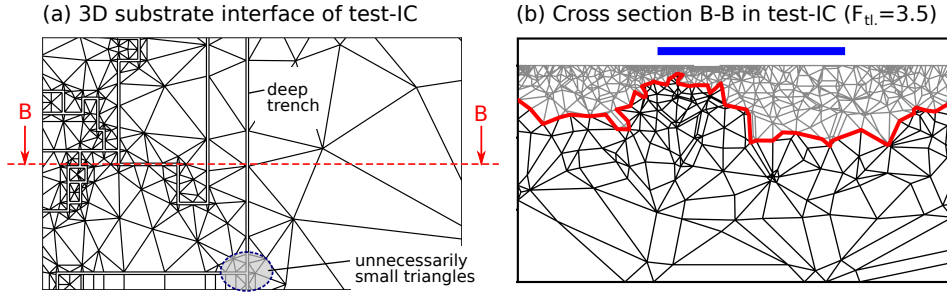


Figure 62: Part (a): The 3D substrate interface in a small part of the IC-layout of the test-IC from chapter 6. Part (b): A cross section of the resulting 3D mesh, which is partitioned by the red line into the ATL (gray) and the residual FEM-mesh (black).

HEURISTIC_ATL correctly scales the ATL height proportionally to the local feature size.

At the deep trench corners, very short edges are necessarily present in the 2D mesh. Since the Delaunay triangulation (sec. 5.2.1) enforces a minimum angle, this leads to a cluster of unnecessarily small triangles. This is highlighted by the dashed circle in fig. 62 (a). It was estimated that the node count in the 2D substrate netlist of the test chip might be decreased by a factor of 3 if this peculiarity was removed. However, it has proven surprisingly hard to fix this algorithmically: For example, if the angle constraint is abandoned in some selected regions, the 3D tetrahedral mesher fails frequently. Moreover, removing the angle constraint can make the FEM stiffness matrix indefinite [174], which might lead to passivity violations.

5.2.6 Conclusion and Outlook

This section has described a new substrate extraction tool flow, which aims to achieve efficient AC and transient simulations. For efficiency reasons, coarse 2D meshes must be used for the description of the N-buried layer and the overlying wells. This is justified by the rather large critical area of the n-buried layer (eq. (61) in sec. 5.1). Marker layers allow the user modify the level of detail selectively and locally, which is another key feature for high performance simulations. In contrast to the 2D mesh, coarsening the 3D mesh is expected to lead to significant errors. Therefore, the novel S-EHRFEM approach, which compresses the 3D mesh in a more suitable manner, was introduced: It reduces the node count in the wafer-substrate by almost two orders of magnitude, and the resistor count was reduced by roughly one order of magnitude at an error bound $< 10\%$ (sec. 5.2.5). It was shown that the choice of the linear solver for FEM/FDM-based 3D substrate models deserves particular attention:

Even though an optimized log-graded mesh is used, the direct solver run time scales quadratically with the number of nodes on the top surface of the wafer-substrate. The use of iterative linear solvers may be a feasible solution to reduce the run time significantly. However, it must be kept in mind that switching to an iterative linear solver is not trivial because it may impair the robustness of the circuit simulation (sec. 2.3.1).

Porting the Tool Flow to Proprietary Substrate Extractors If the developed software for generating 2D and 3D substrate netlists should be further developed for productive use, additional permanent maintaining efforts will arise. Thus, question must be raised whether this tool flow should rather be ported to, for example, the QRC substrate extractor. The developed substrate extractor has numerous unique and useful features, which cannot be mapped to QRC. For example, substrate ties offer fine control over the used connection style, e.g. the boundary conditions at the n-epitaxial layer. Moreover, to the current understanding, QRC does not offer options that enable a suitable reduction of the trench ties. In sec. 5.2.3, the tremendous importance of adequate meshing became evident: For example, assume the 2D mesh is refined by a factor of four in, both, the x and the y dimension. If the substrate model is the bottleneck, this refinement is expected to cause a 256-fold increase in the SPICE-simulation time – i.e. this makes the difference between *an overnight run and four months worth of computation*. Therefore, no matter which substrate extraction tool is used, *a thorough understanding and documentation of the mesher must be a basic requirement* of such a tool flow. The mesh should always be subject to user interaction and user review³⁴. Therefore, in a QRC-based substrate extraction tool flow, special marker layers, which allow to locally control the level of detail, should be supported as well (sec. 5.2.2). The ATL-reduction of the developed tool enables an efficient, high-precision description of wafer-substrate currents, while allowing for a low-resolution 2D mesh of the n-epitaxial layer. It is yet to be understood how this compares to the “substrate RC-reduction” feature of QRC (see sec. 2.6.2).

Next Steps in the Further Development of the Substrate Extraction Tool

In sec. 5.2.5 it was observed that the 2D mesh contains a large number of unnecessarily small triangles at trench corners. If this was improved and the number of interface points could be reduced three-fold, then the efficiency of SPICE-simulations with direct linear solvers might improved by roughly an order of magnitude (sec. 5.2.3). Moreover, this issue also has implications

³⁴ The default mesh will almost certainly result exceed the circuit simulator’s capabilities, and simplifying the mesh requires that a suitable level of detail is found for each part of the layout. This cannot be fully automated, and thus the meshing process must be exposed to the user.

on the usability: In polygon-representations of realistic IC-layouts, there are many cases besides trench corners, in which yet smaller edges are present. This must be resolved to the best possible extent, in order to get an efficient substrate model. Currently, this requires manual work, which is rather tedious. For example, in small regions, the dimension should be reduced manually by means of marker layers (sec. 5.2.2), and sometimes devices and trenches must be moved or deleted. A more powerful and more automatic approach is highly desirable: Future solutions might short-out vertices in the 2D mesh by a semi-automated method, or an RC-reduction akin to TICER (sec. 2.6.1) might be applied to the 2D mesh.

The part of the source code that prototypically implements S-EHRFEM requires improvement: Firstly, computing the Y-parameters of X_{atl} has a quadratic asymptotic run time, as argued in sec. 5.2.4. Extracting the IC-layout from sec. 6.3.1 is already very hard, due to the poor scaling of this step's run time. The asymptotic run time clearly *cannot* be improved further in the linear solver because the size of the output, i.e. the dense Y-parameter matrix of X_{atl} , already scales quadratically in $N_{\text{s.c.}}$. One possible solution would be to break X_{atl} into many overlapping patches, and to compute their Y-parameters separately³⁵.

Secondly, as shown in sec. 5.2.5, the bottom surface of the ATL in the prototypical implementation is not smooth. As a consequence, more than necessary mesh points are inside each cylinder with radius R_c . For example, if the surface raggedness leads to a twofold increase in the number of mesh points on the ATL's bottom surface, the resistors count $T \leftrightarrow B$ (see table 7) is twofold increased and the resistors count $B \leftrightarrow B$ is four times larger. This has a large impact on the netlist size because it is dominated by the resistors in the ATL (see sec. 5.2.5). Moreover, in the computation of r_{ij}^{eff} using eq. (98), a ragged bottom surface leads to errors because the sorting $L_i(j)$ is inadequate. In order to make the bottom surface of the ATL more smooth, it has to be triangulated prior to meshing the ATL and the residual FEM-mesh. This is most easily realized if the ATL height was not location-dependent.³⁶

Third, the requirement that the 3D mesh surface is a proper subdivision of the 3D substrate interface has led to extensive, fragile fine-tuning of mesher parameters. Possibly, a custom mesher based on axis-aligned oct-trees might be more simple and robust, and it could provide the log-grading as an intrinsic feature. The electrical connection between interface and mesh points via the

³⁵ Besides improving the asymptotic run time, in addition, this enables parallelization.

³⁶ Note that using a flat ATL one can also get rid of HEURISTIC_ATL, and instead, in each run of the 3D substrate netlisting, optimize the global ATL height using a sweep. However, thereby, optimization potential is lost if the size of the 2D mesh varies from place to place.

mesh-interface coupling matrix M_{ij} from eq. (90) works here as well. However, the computation of M_{ij} becomes more involved.

Future Extensions and Research Opportunities In the future, the developed substrate extraction tool might serve as a platform for future research in other areas: For example, it might be extended to support the simulation of minority carrier injection (see sec. 2.2). Another possible extension is the support for displacement currents in the wafer-substrate, which could be relevant for higher frequencies or for higher ρ_{sub} (sec. 5.2.1). This is implemented astonishingly easily: After the extraction, every resistor in the 3D substrate netlist is augmented by a parallel capacitor, which has a proportional capacitance. Despite this creates negative capacitors, the stability of transient simulations should not be impaired because this capacitance matrix is positive definite.

In sec. 2.6.2 it was remarked that inductance extraction faces similar computational challenges because, also here, the canonical network parameter representation is not easily sparsified. It can be shown that there is actually an exact duality between inductance extraction and substrate extraction: Specifically, inductance extraction can be achieved by solving two Laplace's equation in a half space, i.e. for the A_x - and the A_y -field (sec. 2.5.2). Therefore, in analogy to S-EHRFEM, a more efficient method for inductance extraction might be constructed. This method could be termed LK- or *RLCK-extraction using highly reduced FEM-meshes* (LK- or RLCK-EHRFEM). This would solve the cutoff distance issue of inductance extraction (see sec. 2.6.1).

Experimental Verification The RF-emission measurements in sec. 6.5 provide an indirect experimental verification of the developed substrate tool flow. However, in this thesis, no direct measurements of substrate resistances are presented. This is due to the fact that substrate resistances of small test structures are of little informative value, whereas large test structures are rather expensive and their measurement is quite involved: For example, assume a small HV-device is used as a test structure, and its circumference is scaled in multiple steps. Measurements of the resistance between this n-epitaxial pocket and the surrounding trench are easily performed using a VNA. However, this resistance is similar to $R(B, T)$ from sec. 5.1.1, and it is thus expected to carry almost no frequency dependence and only a weak dependence on the circumference. This quantity is “trivial”, and it's rather well predicted by any FEM simulator, no matter which boundary condition is used. Conversely, more meaningful on the substrate extractor's accuracy are resistances that involve at least one n-epitaxial pockets larger than the die thickness. For example, a meaningful verification approach would be to measure a quantity akin to $R(A, C)$ from sec. 5.1.1. However, in order to measure only a single

data point from fig. 46 (a), already multiple square millimeters of silicon area are needed ³⁷. Moreover, the backside would have to be metallized, properly connected and used as common reference because the backside otherwise couples to the prober tip in an undefined manner (see sec. 4.4.1). This can be realized by mounting the test chip into an IC-package, but then, the measured network parameters also include the lead frame and the bond wires. Removing the lead frame and the bond wires parasitics by means of de-embedding is hardly possible because they are rather large, and open-/short-structures are not easily realized.

³⁷ Maybe, multiple data points could be realized in a single test-IC, by nesting multiple n-epitaxial pockets B in one another. The size of B could then be altered by reconnecting these n-epitaxial pockets via focused ion beam (FIB) modifications.

5.3 Summary

- In many cases, the n-buried layer can be regarded as equipotential. Prescribed constant voltage (PCV)-based substrate extraction goes one step further, and also approximates the wafer-substrate surface of each n-epitaxial pocket as equipotential.
- It was shown that low-dimensional, PCV-based substrate extraction suffers from pronounced artifacts: Substrate resistors between two pockets are underestimated by up to a factor of 6, and substrate resistors connecting large-area pockets with surrounding deep trenches are underestimated by up to a factor of 8. Two solutions were proposed: Either the p-n-junction below the n-epitaxial layer must be fractured into an array of diodes. Alternatively, one can use the novel capacitive-layer impedance (CLI) boundary conditions.
- A heuristic was presented that allows to obtain a real-valued, frequency-independent and passive resistor network using CLI-based substrate extraction. This resistor network, in which nodes represent the *average surface potential* of the wafer-substrate, facilitates accurate pencil-and-paper calculations.
- Low-dimensional substrate models put an upper limit on the device count, and they cannot easily incorporate the voltage gradients in the n-buried layer, the inductance of the seal-ring, the n-sinker resistance and their metal routing. Moreover, further software automation is needed for the seamless integration with metal parasitics, and in order to account for the composite longitudinal trench resistance. To overcome these limitations, a novel substrate extraction tool flow, which is based on 1st-order FEM, was developed.
- In this tool-flow, the substrate model is divided into the 2D substrate netlist and the 3D substrate netlist. The 2D substrate netlisting, which is concerned with the trenches, the n-buried layer and the wells it contains. It is highly customizable and unique in the aspect that the precise semantics of the field model are transparent to the user. A novel approach to interactively control the model's "level of detail" using marker layers was introduced. This is very important to keep the model complexity within reasonable bounds.
- The 3D substrate netlist is a resistor network that represents the wafer-substrate by a FEM-discretization of Laplace's equation on a tetrahedral mesh. It is expected to dominate the run time of the direct linear solver, and thus, a focus was put on its optimization: It was shown that the use of a log-graded 3D mesh allows to reduce the asymptotic run time from $\mathcal{O}(N_{s,c}^{3.5})$ to roughly $\mathcal{O}(N_{s,c}^2)$. In practice, additional improvements of the run time might be achieved by using iterative linear solvers. 2D FEM-elements in the n-buried layer can be easily coarsened up $A_c/2$, where A_c is the critical area (sec. 5.1). Conversely, to reduce the 3D mesh, a new technique (S-EHRFEM), which preserves the accuracy of shallow current paths, e.g. in the vicinity of deep trenches, was invented.

CHAPTER 6

Evaluation of the Methodology and Analysis of the Coupling Paths Based on a Test-IC

6.1 Introduction

This chapter uses the developed physically-based methodology to predict the RF-emissions of a test-IC. This test-IC, which resembles a complex Automotive System IC, was developed in the course of this thesis specifically for this purpose. Moreover, counter-measures against these RF-emissions are envisioned and tested. They actually attenuate the RF-coupling, and thus go beyond conventional approaches that merely shape the spectrum of the disturbance source. Additionally, the transfer functions implicated in the RF-emissions are described using simple equivalent circuits, which enables a better understanding. This is achieved by applying a computer-aided procedure that removes negligible parasitic elements. This chapter also presents results that have been published previously in [164], [165].

In automotive ECUs, there is no alternative to DC/DC-converters: They are required to down-convert the battery voltage into lower and more stable supply voltages in an energy efficient manner. For example, they are used to supply automotive microcontrollers and sensors, and they are used to pre-stabilize the input voltage of LDOs [8], [91]. Various market forces (see sec. 1.2) have led to the integration of DC/DC-converters into Automotive System ICs that contain transceivers. It is known for some time that the combination of DC/DC-converters and transceivers on a single die is rather problematic from the EMC-perspective: Although DC/DC-converters typically operate at comparatively low switching frequencies (typ. 300 kHz – 2.2 MHz [89], [91]), the large non-sinusoidal switching currents and voltages lead to pronounced high frequency emissions. Very high harmonics of integrated DC/DC-converters in the order of hundreds of MHz [104] were observed to crosstalk to transceiver pins in System Basis Chips. Since the specifications of automotive buses do not allow the installation of a considerable capacitance at the bus lines [10], [116], such RF-emissions can't be easily filtered externally. Moreover, the digital core, which is present in any Automotive System IC (sec. 2.1), is also often a culprit for RF-emissions at the transceiver pins. Both, digital RF-emissions and RF-emissions due to the DC/DC-converter are known to be very relevant, yet rather elusive and difficult to predict. Therefore, these scenarios are considered suitable for evaluating the developed physically-based methodology.

The developed test-IC monolithically integrates a DC/DC-converter with three bus transceivers. The experiments and simulations conducted in this chapter study the RF-emissions at the three transceiver pins. These RF-emissions are caused by the operation of the integrated DC/DC-converter, as well as by an emulation of a digital clock distribution network, which will be called “disturbance source”. The three transceivers are located at different distances to the DC/DC-converter. Thus, the RF-coupling paths to the DC/DC-converter differ among the three transceivers.

6.2 Description of the Test-IC and the Packaging Variants

The test-IC, which was developed in the course of this thesis, is based on a typical architecture for Automotive System ICs (sec. 2.1). It uses a BCD-technology akin to sec. 2.2. Fig. 63 shows a simplified top-level schematic of this test-IC. It contains four analog/power modules, i.e. the three transceivers and the integrated step-down DC/DC-converter. The DC/DC-converter is clocked at 3 MHz (clk_dcdc) and the digital “disturbance source” is clocked at 32 MHz (clkd). In addition, the test-IC contains a pad-row, a central functions module and a digital part. Details on the floor plan are found in sec. 6.3.1.

The integrated DC/DC-converter in fig. 63 was derived from a state-of-the-art Infineon design, which is similar to step-down converter discussed in sec. 2.1. It can be configured and enabled by the SPI-accessible registers “reg_dcdc”. The power ground of the DC/DC-converter (PGND) is separated from the system ground (SYSGND) and it is connected to the PCB-ground via two dedicated pins, each of which is double-bonded. In the course of this thesis, the DC/DC’s original design was modified by replacing the “regulation loop and the control logic” (fig. 2): Rather, the new “custom PWM-generator, startup- and shutdown-logic” (fig. 63) clocks the half bridge of the DC/DC-converter at a constant frequency and with a constant duty cycle. This is supposed to increase the spectral purity of the RF-emissions, for the purpose of achieving more predictable and reproducible measurements (see sec. 6.4). It should be noted that, in this design, a certain amount of minority carriers (sec. 2.2) are presumably injected into the wafer-substrate at the low-side switch ML. The question of their relevance for the EMC will be answered in chapter 7.

Each transceiver can be selectively configured and enabled via the SPI-registers “reg_tr*”. The output stage of the transceivers is a series connection of

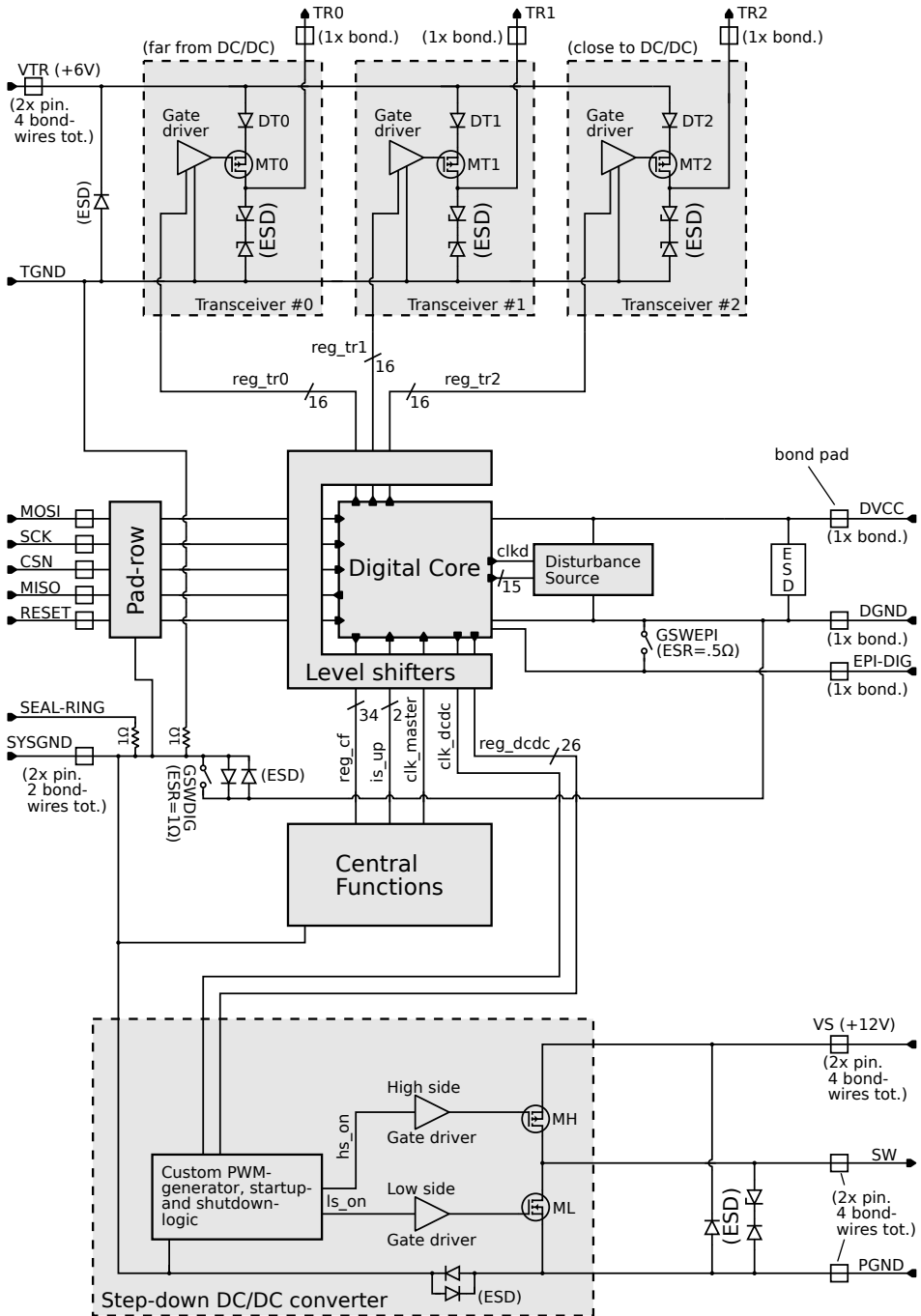


Figure 63: Simplified top level schematic of the developed test-IC, in which the RF-emissions at the transceiver pins (TR0, TR1 and TR2) will be measured. TGND and SEAL-RING are depicted as schematic terminals, but they are not bonded to IC-pins. This is indicated by the lack of a bond pad symbol (white square).

a large-area HV-MOSFET and a diode¹, i.e. MT* and DT*. ² In addition, two anti-serial diodes are connected to the transceiver output for ESD-protection. Depending to the selected bus state (ON, OFF), which is selected by “reg_tr*”, the gate driver either charges or discharges the gate of the HV-MOSFET MT*. In the ON-state, MT* pulls the bus line to the power supply pin VTR, which is shared among all three transceivers. Conversely, in the OFF-state, the voltage of the bus line is determined by an external pull down resistor. This circuitry does not correspond to any of the established automotive buses. For example, the LIN-bus [116] is inverted, i.e. the signal wire is pulled to ground in the dominant state. However, the RF-coupling mechanism is thought to be highly comparable to LIN-transceivers.

The digital “disturbance source” (fig. 63) is placed in the n-epitaxial pocket of the digital core, and it runs on the same power domain as the digital core. It consists of multiple inverter chains that are capacitively loaded by a total of roughly 84 pF. This emulates a clock distribution network that drives a large number of synchronous D-flip-flops. A SPI-register allows to enable these inverter chains selectively. The “disturbance source” creates sharp current pulses at the rising and falling edges of the clock.

The central function block contains a bandgap voltage reference generator, an oscillator and a phase-locked loop (PLL). Moreover, it generates bias currents, which are distributed to each of the three transceivers, and to the DC/DC-converter (not shown for clarity). Note that each component of the central functions module is configured by a part of the 34-wide SPI-accessible register “reg_cf”. The phase-locked loop is used for synthesizing “clk_master” from the oscillator output. The voltage reference is required by the gate driver circuitry of the DC/DC-converter (not shown for clarity). Multiple low-voltage supplies (see also VDDDIG, VDDANA from sec. 2.1) are needed by the digital part, its level-shifters, the central functions and each analog/power module. The supply of the digital part is called DVCC in fig. 63, whereas the other low-voltage supplies are omitted from this schematic for clarity. In the developed test-IC, these low-voltage supplies are *not* internally generated, but instead supplied via IC-pins. This simplifies the implementation of the test-IC³.

¹ Strictly speaking, DT0, DT1 and DT2 are rather body diodes and diode-connected power-MOSFETs connected in parallel. However, for simplicity, they will be called and depicted as diodes.

² For brevity, MT* and DT* shall refer to one of { MT0, MT2, MT2 } and { DT0, DT1, DT2 }, respectively.

³ It must be remarked that, in real-world Automotive System ICs, these low-voltage supplies are usually internally generated because these ICs are typically required to be powered directly and only by the car battery.

The digital core implements multiple SPI-accessible registers, as well as SPI-configurable clock-dividers and -gates for “clk_d” and “clk_{ddc}”. It runs on the dedicated (DVCC, DGND) power-domain, i.e. the digital power supply (DVCC) and ground (DGND) is separated from the system level power supply and ground (SYSGND). In the course of this thesis, the dedicated digital ground pin was invented as an attempt to reduce digital emissions at the transceiver pins (TR0, TR1 and TR2). This ground separation is a novel design concept, and the classical architecture instead runs the digital core on the system level ground for economical reasons (sec. 2.1). To the current knowledge, this has not yet been attempted in an Automotive System IC before ⁴. A disadvantage of this approach is that an array of low-voltage level-shifters, which transfer digital signals between the (DVCC, DGND) and the system-level power domain, has to be added. These level-shifters were custom-designed and -optimized, and a single level shifter requires an area of about 400 μm^2 . In the developed test-IC, the area of these level-shifters is roughly 8% of the area of the digital core ⁵.

Another attempt to reduce the digital RF-emissions was to connect the n-epitaxial layer below the digital core to a dedicated IC-pin, which is called EPI-DIG. Firstly, connecting EPI-DIG to a high potential reduces the effective junction capacitances of the n-buried layer, and secondly, the n-buried layer might then shield the substrate from the digital ground. To evaluate the significance of these counter-measures against digital RF-emissions, two modifications of the standard bonding diagram, which are termed *DIG-NO-EPI* and *DIG-NO-EPI-GND*, were realized: In *DIG-NO-EPI*, only the EPI-DIG bond wire is removed, and in *DIG-NO-EPI-GND*, both the EPI-DIG and the DGND bond wires are removed. Note that, if the EPI-DIG-pin is removed, EPI-DIG will be connected to DGND on the die, and conversely, if the DGND-pin is removed, DGND will be connected to SYSGND on the die. These connections have a well-controlled ESR ($\text{ESR} = 0.5\ \Omega$ and $1\ \Omega$, respectively) and are denoted by GSWDIG and GSWEPI in fig. 63.

The system level ground (SYSGND) is bonded to two separate pins. The seal-ring and the transceiver ground (SEAL-RING and TGND in fig. 63) are connected to SYSGND at two locations on the die, with an ESR of $1\ \Omega$ each. The initial concept allowed to separate these grounds, and it featured dedicated pins. The separation of these grounds will not be further investigated in

⁴ This ground separation will improve the RF-isolation rather strongly (see sec. 6.5.6). It is *not* to be confused with the introduction of dedicated ground pins for some analog modules, which, in contrast, is very common (sec. 2.1).

⁵ It is presumed that this percentage is larger in productive ICs, due to the increased number of internal I/Os of the digital core and due to a reduced filler capacitor ratio. Moreover, in a productive IC, duplications of parts of the central functions (see sec. 2.1) would further increase the die area.

	Description	Bonding diag.	Die backside	Die attach glue	Die-pad
#C1	Ceramic	standard	silicon	non- conductive	none (ablated)
#P1	Plastic (default)	standard	metallized	highly conductive	exposed, grounded
#P1M	Plastic, die-pad milled out	standard	metallized	highly conductive	none (milled out)
#P1S	Plastic, backside milled out	standard	silicon (milled out)	none (milled out)	none (milled out)
#P1-UNMOD	Plastic, additional grounding	ADD- GND	metallized	highly conductive	exposed, grounded
#P1-DNE	Plastic, no EPI-DIG-pin	DIG- NO-EPI	metallized	highly conductive	exposed, grounded
#P1-DNEG	Plastic, no EPI-DIG pin and no digital ground	DIG- NO-EPI- GND	metallized	highly conductive	exposed, grounded
#P5	Plastic (undefined backside)	standard	non- metallized	slightly conductive	exposed, grounded

Table 9: Packaging variants of the test-IC.

the following because the benefit for the EMC was not found significant enough. For reasons of ESD-protection, the separate grounds DGND and PGND must be clamped to SYSGND by anti-parallel diodes. Moreover, fig. 63 shows additional required ESD-structures that protect VTR, DVCC, VS and SW.

Table 9 lists the packaging variants that are investigated in this thesis. Note that in all measured samples, the die thickness is 600 μm . In the packaging variant #C1, the test-IC is housed by a ceramic package with 64 pins without exposed pad. In order to rule out an ohmic or capacitive connection of the die backside⁶ with the non-connected metallized die-pad, the metallization of the die-pad was partly ablated. This is shown in fig. 64 (a). In addition, the die was attached using non-conductive glue, which prevents shorting of different regions of the die backside. This is based on the presumption that otherwise the glue would have to be included in the substrate model (see sec. 6.5.2). In the packaging variant #P1, a 64-pin plastic IC-package is used (LQFP-64 from chapter 3), which features an exposed pad. This exposed pad is soldered and connected to the PCB ground plane. As opposed to #C1, in #P1 the die backside is metallized, and the die was attached to the die pad via

⁶ The backside of the die in the packaging variant #C1 is not metallized but is rather bare silicon, as indicated by the column “die backside” in table 9.

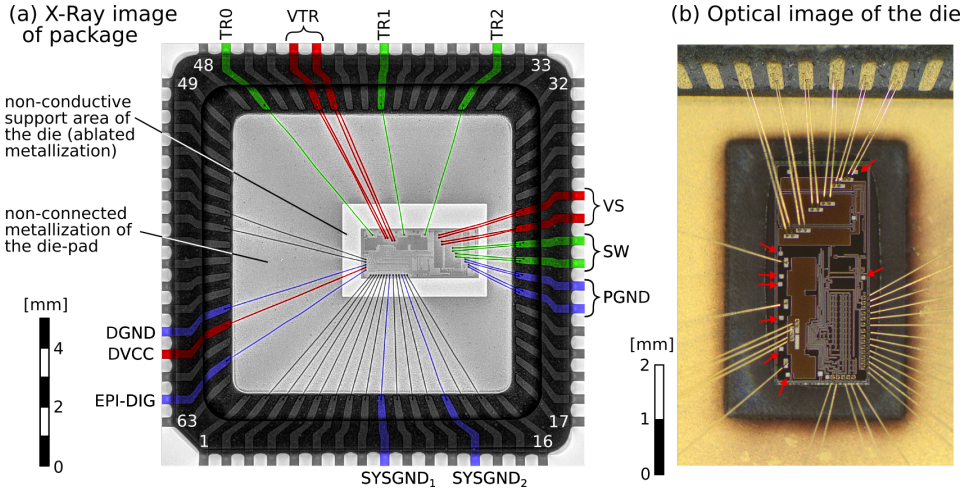


Figure 64: X-Ray and optical images of the developed test-IC with packaging variant #C1. In (a): Pins that are relevant for the EMI measurements are marked in color. The remaining pins are either low-voltage digital I/Os, or low-voltage power supplies. Red arrows in (b) mark additional ground bond pads used in the bonding diagram ADD-GND.

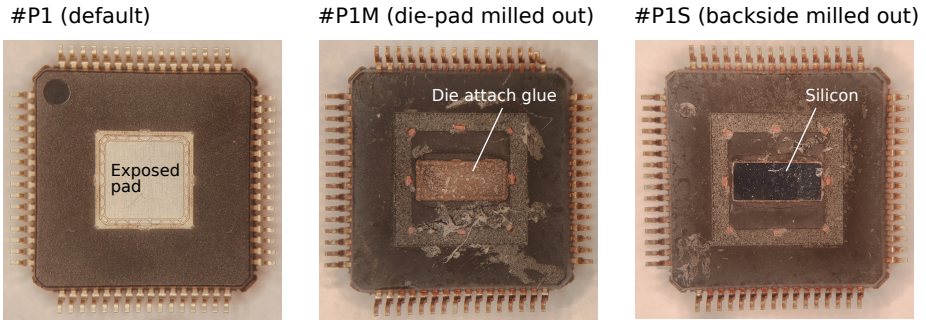


Figure 65: Bottom view of the packaging-variants #P1–#PIS. In #P1 and #P1M, grooves of different depths were milled out.

a highly conductive glue (see sec. 2.2). In cooperation with engineers at the semiconductor fabrication plant, special care was taken that the die backside metallization forms an ohmic connection with the wafer-substrate.

Samples of type #P1M and #P1S in table 9 are modifications of #P1, obtained by milling out a rectangular groove at the package backside. This groove is roughly 0.15 mm deep. These modifications, which are depicted in fig. 65, allow to investigate the impact of the die backside grounding. In #P1M, the die-pad was milled out, but the die attach glue was not removed. Conversely, in #P1S, the groove penetrates slightly into the silicon, such that it removes the glue and the die backside metallization layer. Samples of type #P1M and #P1S

must *not* be soldered at the backside, but instead a film of solder resist that isolates it from the PCB ground plane will be applied. In the packaging variant #PI-DNE (table 9), the bond wire at EPI-DIG were removed, as described above (bonding diagram DIG-NO-EPI). In #PI-DNEG, additionally, the bond wire at DGND were removed. In #PI-UNMOD, a large number of optional bond-pads (red arrows in fig. 64 (b)) are connected to ground pins: Specifically, three additional ground-bonds attach directly to the seal-ring, four additional bonds ground the trenches of each transceiver and the DC/DC-converter, and another ground-bond is connected to TGND in fig. 63.⁷ The packaging variants #C1 and #PIS both feature a galvanically unconnected backside. However, in #C1, the pin-inductances, as well as their mutual inductances, are significantly larger.

In some samples of type #PI-#PI-DNEG, rather large voids were observed in the die attach glue. This can also be anticipated from fig. 65 (b). However, apparently these glue voids are benign: Measurements of the DC resistance between the SYSGND-pin and the backside have shown a negligible sample variance, and SEM-images revealed that the glue does not delaminate. Moreover, the measurements in sec. 6.5 are generally in good alignment with simulation.

It must be remarked that the previously-described plastic packaging variants were specifically engineered to have an electrically well-defined backside. This might not apply to the backside of all real Automotive System ICs. Rather, in some ICs, the glue, which must be conductive for thermal reasons (sec. 2.2), forms a poorly-controlled electrical contact with the wafer-substrate. Note that even if a backside *metallization* is applied to the die backside, the formed contact might still be electrically undefined. Physically, the die backside contact may be a Schottky-diode, an isolating oxide layer or a galvanic contact. The nature of the backside contact can vary across the wafer. Such an electrically-undefined backside contact was implemented in the packaging variant #P5 (table 9): Here, a die without backside metallization is attached to the die pad using a slightly conductive glue. For one sample of type #P5, a small-signal characterizations of the backside was performed at zero DC bias, and a capacitive characteristic with $43 \frac{\text{pF}}{\text{mm}^2}$ was found.

⁷ These optional ground-bonds are not shown in fig. 63. Moreover, for simplicity, simulations of the #PI-UNMOD are left out from the descriptions in sec. 6.3.

6.3 Predicting the RF-Emissions using the Developed Methodology

6.3.1 A System Model that Combines the Integrated Circuit, the Substrate, the Package and the PCB

In order to predict the RF-emissions of the test-IC, in the course of this thesis, a system model was created. It integrates the semiconductor devices, the substrate-, the IC-package- and the PCB-model.

Package Models Table 10 summarizes the multiple package models that are tested. None of these package models makes use of vector fitting (sec. 3.2.4). The package models #P-BB, #P-HYB and #P-EXT are models of the 64-pin plastic IC-package (sec. 6.2) with port semantics. They are interchangeable and can describe the packaging variants #P1 – #P5 (table 9). #P-BB and #P-HYB

	Description	Die reference	Tool	Excitation	Inclusion in circuit simulation
#C-BB	Ceramic package (Maxwell eq., black box)	Floating reference	HFSS	Lumped ports	Network parameters instantiation (AC only)
#P-BB	Plastic package (Maxwell eq., black box)	Metallic extension	HFSS	Lumped ports	Network parameters instantiation (AC only)
#P-HYB	Plastic package (Maxwell eq., lumped-elements, loop ind.)	Metallic extension	HFSS	Lumped ports	Ground-return inductances from port-based H-parameters
#P-EXT	Plastic package (quasi-static, lumped-elements, loop ind.)	Metallic extension	Q3D	Port-like	Ground-return inductances from transformation in fig. 25
#P-EXT-NOR	Plastic package (quasi-static, lumped-elements, partial ind., eddy)	–	Q3D	Terminal-like	Partial inductances (incl. ground plane eddy currents)
#P-EXT-NOP	Plastic package (quasi-static, lumped-elements, partial ind.)	–	Q3D	Terminal-like	Partial inductances (not including ground plane)

Table 10: Package models used in the simulations of the test-IC.

are based on the same network parameter dataset, but each uses a different method to include this dataset into the SPICE simulation. This network parameter dataset was obtained using a HFSS-simulation, in which the lumped ports refer to a “metallic extension” on top of the die pad (see sec. 3.2.1). In #P-BB, the network parameters were directly instantiated, which is feasible only for AC-simulations (sec. 2.4.2). Conversely, #P-HYB is a lumped-element model constructed from these network parameters in the port-based H-parameter form (sec. 3.3.3) ⁸. In contrast to #P-BB and #P-HYB, the package model #P-EXT from table 10 is based on quasi-static approximations of Maxwell’s equations (sec. 2.5.2): The parasitic extraction tool Q3D was used to compute a capacitance, a resistance and an inductance matrix from a 3D model. In this 3D model, the PCB ground plane is present, and reference terminals are placed, both, onto the ground plane or onto the metallic extension (see sec. 3.3.1 and sec. 3.3.4). The resistance matrix is computed at DC, whereas the inductance matrix corresponds to the high-frequency limit, which is required to correctly account for magnetic shielding (sec. 3.3.4). The circuit representation of #P-EXT is obtained using the transformation to port-based H-parameters from sec. 3.3.3 (fig. 25). The package model #P-EXT-NOR is a modification of #P-EXT, in which the reference terminals were omitted. The PCB ground plane is still present but floating. Thus, #P-EXT-NOR represents the pin-parasitics by *partial* inductances, in which ground plane eddy currents are included, but no true return currents (sec. 3.3.1). The package model #P-EXT-NOP goes even further than #P-EXT-NOR, and removes the PCB ground plane entirely.

The ceramic packaging variant #CI (table 9) is described using the package model #C-BB. #C-BB is based on a network parameter dataset from a HFSS-simulation that uses a floating reference, as described in sec. 3.2.5. A single lumped port was placed between the PCB ground plane and the floating reference, and this port was eliminated as shown in fig. 21.

Substrate and Layout Parasitics Table 11 summarizes the various substrate models used throughout this chapter. The argument C_{bs} to #X-CAP and #X-MCAP represents the capacitance per area at the backside. The substrate models #X-* are created by applying the automated substrate extraction tool flow (sec. 5.2) to a simplified layout of the IC. Specifically, to create the simplified IC-layout, many small n-epitaxial pockets, as well as the trenches that separate them, were removed manually. Moreover, all remaining semiconductor devices were moved from the IC-layout to a schematic, which is described

⁸ This lumped-elements model includes resistances (R), capacitances (C), inductances (L) and inductive couplings (K). The inductances are interpreted as ground-return inductances. The resistances were obtained at 10 MHz, whereas L, C and K were obtained at 100 MHz.

	Type	b.c.	Backside
#X-NC	Extracted Layout with Substrate	–	not shorted, not connected
#X-GND	Extracted Layout with Substrate	–	shorted, connected
#X-CAP(C_{bs})	Extracted Layout with Substrate	–	not shorted, distributed capacitance
#X-MCAP(C_{bs})	Extracted Layout with Substrate	–	shorted, lumped capacitance
#R-CLI-NC	Resistor Network of Wafer-sub.	CLI	not shorted, not connected
#R-CLI-GND	Resistor Network of Wafer-sub.	CLI	shorted, connected

Table II: Substrate models used in the simulations of the test-IC.

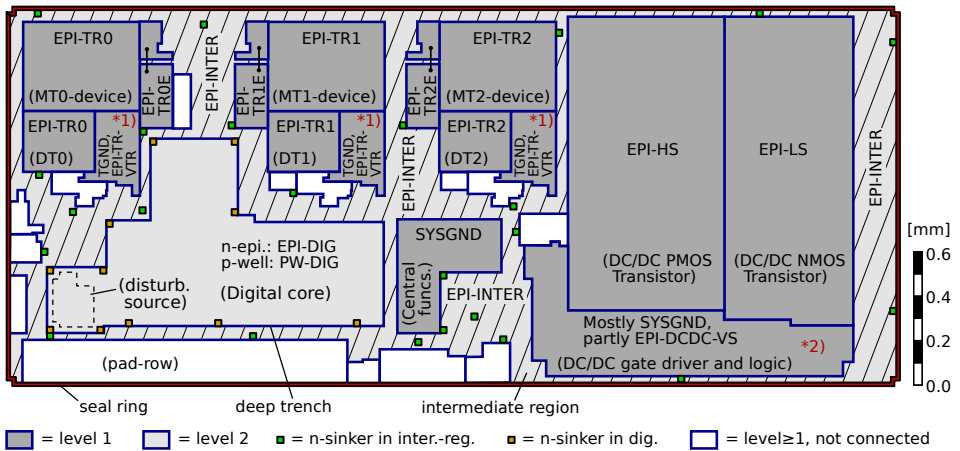


Figure 66: Overview drawing of the simplified IC-layout. The labeling of the n-epitaxial pockets (light-, dark-gray) denotes the net names of the n-epitaxial layer. In the simplified IC-layout, further subdivisions of n-epitaxial pockets and further deep trenches are present (not shown here for clarity).

below (fig. 67). Separating these devices from the layout enables an unbiased comparison of #X-* to the low-dimensional substrate models #R-CLI-*⁹.

Fig. 66 shows a further simplified overview drawing of this simplified IC-layout. The individual modules (DC/DC and transceiver #0, #1, #2), the digital part, the central functions and the pad-row are separated from each other by

⁹ However, of course, in a productive work-flow, the devices should rather enter the model via the extracted netlist, since otherwise some benefits of the automation are lost.

the so-called *intermediate region* (hatched area). The intermediate region is used for signal- and power-routing only, it contains no semiconductor devices, and its n-epitaxial layer as well as its logic implant are connected to EPI-INTER, which is connected to SYSGND via a $0\ \Omega$ resistor. Such a region is usually present in Automotive System ICs, but is typically more compact than in the test-IC developed in this thesis¹⁰. The dark gray areas represent regions of level 1 (sec. 5.2.2), i.e. regions in which the interface to SPICE-device models is placed at the n-buried layer. Applying level 1 to the used HV-devices is justified by the introductory considerations of sec. 5.1. Conversely, in the light gray area, effectively level 2 is used. In the simplified IC-layout, level 2 only applies to the intermediate region and the digital part. Here, the sheet-resistance of the n-buried layer as well as the logic-implant's capacitance and sheet-resistance are a part of the field model. In level 2, by default, the description of the p- and n-wells would include their average contact resistance, and the average n-well-capacitance would be evenly distributed over the area (sec. 5.2.2). However, the n-wells in the digital part were removed in the simplified layout because their capacitance is already included in the lumped element CDIG, as described below. Furthermore, due to the current lack of experimentally verified figures, the average p-well contact resistance was set to zero.

The labels in fig. 66, e.g. SYSGND, EPI-INTER or EPI-DIG, describe the net name to which the n-buried layer is galvanically connected. Moreover, PW-DIG is the net name of the p-wells and the logic implant in the digital part. These net names refer to terminals of the substrate model. The n-buried layer in the intermediate region and the digital part's pocket are contacted by a large number of n-sinkers (green and orange rectangles, respectively). The metallization connecting the n-sinkers of level-2 regions is present in the simplified IC-layout, but it was omitted here for clarity. Note that the metallization connecting the digital part's n-sinkers is a closed loop that surrounds the whole perimeter. Moreover, the simplified IC-layout also contains the metallization that connect the deep trenches to the seal-ring (sec. 2.2), i.e. it correctly accounts for the composite longitudinal trench resistance. Since the extraction of the metallization (QRC in fig. 51, sec. 5.2.2) is currently only a RC-extraction, inductances of this interconnect network are *not* modeled. The last column in table 1 summarizes which parasitic elements are included in the substrate models #X-^{*}.

The substrate models #R-CLI-^{*} in table II contain low-dimensional resistor network representations of the wafer-substrate only. Thus, from all parasitics listed in table 1, these models *as such* only account for ρ_{sub} . However, trench

¹⁰ Furthermore, in productive ICs, neighboring modules often share the same deep trench. This does not occur in the developed test-IC.

oxide capacitances (C_{trench}) and the capacitances between the wafer-substrate and the n-buried layer (C_{sub}) are added subsequently in the form of lumped elements. Furthermore, in the digital part, the capacitance of the logic-implant (C_{log}) and an effective connecting resistance of the n-buried layer is reintroduced as a lumped element. This will be detailed below (fig. 69). In #R-CLI-NC and #R-CLI-GND, the resistor network was computed as described in sec. 5.1.2 – that is, CLI-boundary conditions are used below the n-buried layer and the PCV-boundary condition is used at the interface between deep trenches and the wafer-substrate. Note that the latter turns deep trenches into perfect conductors, i.e. it neglects $R_{\text{tr,long,comp}}$. Technically, #R-CLI-* were obtained by applying S-parameter analysis to the 3D substrate netlists of #X-NC and #X-GND, and using the construction from fig. 45.

To predict the packaging variants #PI and #PI-* (table 9), the backside was approximated as perfectly shorted, and it was connected to ground. Thus, one of the substrate models #X-GND and #R-* -GND must be used. Conversely, in samples of type #CI and #PIS (table 9), the backside is described as a capacitive layer, which is realized by #X-CAP. The validity of this description will be verified in sec. 6.5.2. To predict #P5, the backside is described by #X-CAP(C_{bs}) as well, with the capacitance per area C_{bs} obtained from the small signal characterization (sec. 6.2). However, it is important to understand that such a backside parameterization is of little value in practice because these electrical properties are not process-controlled: Since it must be guaranteed that every IC is EMC-compliant, a more meaningful approach for designers is to consider the corner cases, e.g. #X-NC and #X-GND.

Integrated Circuitry included in the EMC Simulations Fig. 67 shows the simulation schematic that contains the semiconductor devices. As noted above, all semiconductor devices that remained in the IC-layout after manual simplification have been moved to this schematic. The circuit simplifications for simulation can be understood by comparing fig. 67 to fig. 63: Firstly, the digital core, the level shifters, the pad-row and the central functions have been completely removed. In place of the digital core, in fig. 67, there is a single lumped capacitor (CDIG) and its equivalent series resistance and inductance (RDIG, LDIG). Secondly, the ESD-structures were removed, except for those directly attached to the transceiver outputs. Third, the gate drivers of the transceivers, which consist of many LV-devices, as well as some other small LV- and HV-devices, have been replaced by simple equivalent circuits that merely ensure a correct DC bias. Note that this DC bias differs among the three transceivers: For example, when the RF-emissions are measured at transceiver #1 in the ON-state, meanwhile, the transceivers #0 and #2 are switched off. Of course, this must also be accounted for in the simu-

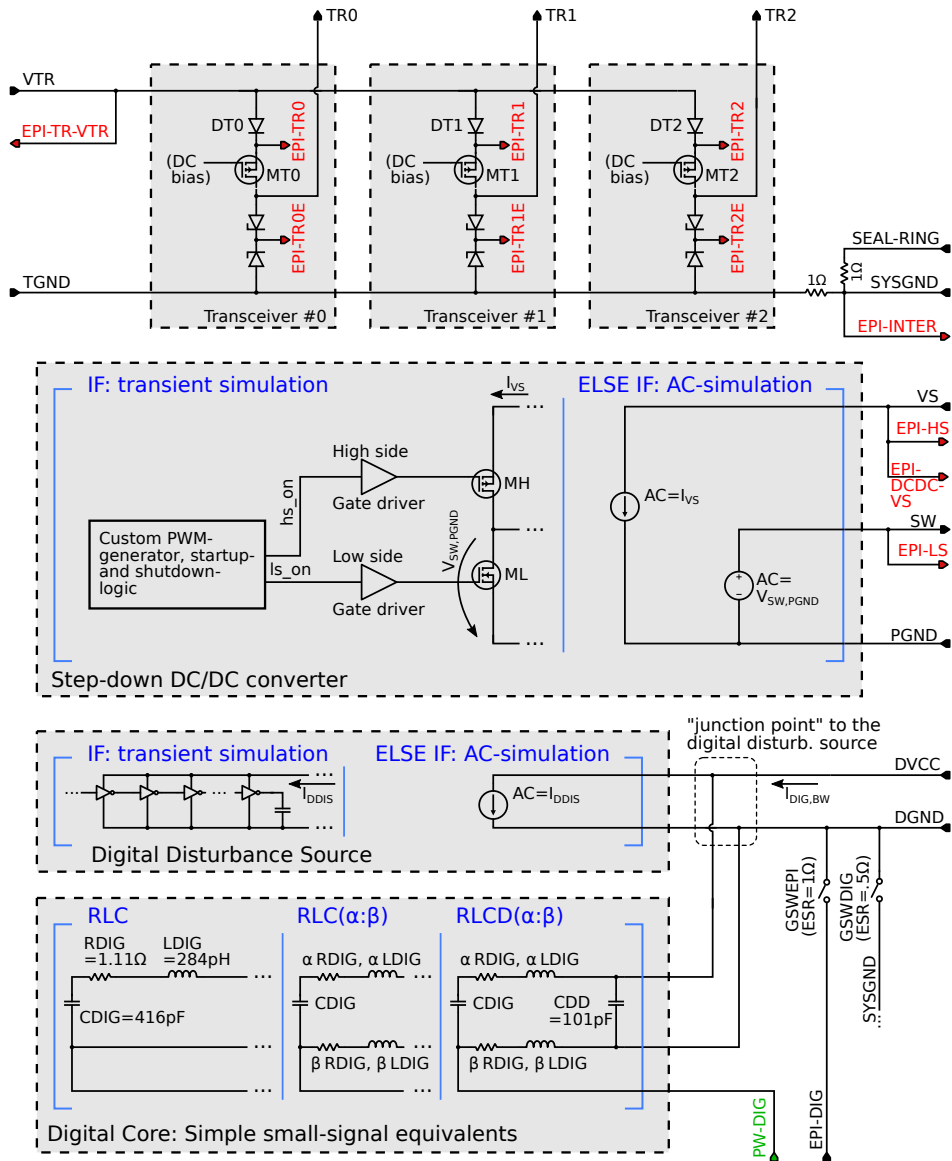


Figure 67: Simplified schematic of the test-IC, which is used for EMC predictions. The additional terminals (red, green) tap the n-buried layer and the p-wells, respectively. Large square brackets (blue) symbolize IF-THEN-ELSE clauses.

lations because, e.g., the RF-coupling between the DC/DC-converter and transceiver #1 might depend on the bias point of transceiver #2 (see also sec. 6.7).

Observe that in fig. 67 the DC/DC-converter module, including its half bridge, is completely omitted from AC simulations. In place of it there is a time-dependent current source and a time-dependent voltage source, which apply a periodic current transient $I_{VS}(t)$ and $V_{SW,PGND}(t)$, respectively. In fact, this is *not* a crude approximation, but actually an *equivalent transform*, if realized properly: The details are elaborated in sec. 6.3.2. A similar simplification was applied to the digital “disturbance source”.

Fig. 67 contains additional terminals that are not present in fig. 63 (shown in red and green). The red terminals tap the nodes that correspond to the n-buried layer in the SPICE device models. For example, EPI-LS is the n-buried layer of the low-side power-MOSFET “ML”. EPI-TR2 is, both, the n-buried layer at the diode of transceiver #2 “DT2”, as well as the n-buried layer at the pass-device of transceiver #2 “MT2”. They happen to be connected to the same node. The asymmetry between EPI-LS and EPI-HS is due to the fact that the n-epitaxial pocket of an N-LDMOS is connected to its drain, whereas the n-epitaxial pocket of an P-LDMOS is connected to its source (sec. 2.2). Observe that the n-buried layer of each HV-device is tied to one of its terminals at DC, but the presented model additionally assumes that the AC-voltage of the n-buried layer is equal to the AC-voltage at that terminal. Using technology information, it was estimated that this is well satisfied for the used HV-devices up to 1 GHz¹¹. For example, in the N-LDMOS, the effective connection resistance of the n-buried layer via the drain-terminal was estimated from the doping profiles. Then, the corner frequencies that it forms with various capacitances attached to the n-buried layer were shown to be significantly larger than 1 GHz.

The Small-Signal Equivalent of the Digital Part The digital part was strongly simplified, as shown in fig. 67. This model was primarily tailored towards the RF-emission prediction of the DC/DC-converter, where it is not necessary to use a more detailed description of the digital part’s distributed capacitance. This chapter does *not* intend to describe the RF-emissions of the digital part at the same high level of accuracy as the RF-emissions of the DC/DC-converter. Rather, the aim is to determine up to which frequency the primitive lumped-elements models of the digital part RLC, $RLC(\alpha, \beta)$ and $RLCD(\alpha, \beta)$ are feasible assumptions for the digital RF-emissions. The capacitor CDIG is sum of the logic cell’s effective capacitance, the capacitance

¹¹ Some caution must be taken because this might not apply to other devices or in other technologies

of all filler caps, as well as the capacitance of all n-wells to the logic implant. CDIG was predicted using a schematic-level AC-simulation of the complete digital netlist in the supplied DC-state, as well as using DC-biased on-wafer measurements using a VNA. These VNA-measurements have led to minor corrections of CDIG.

In order to obtain the ESR and ESL of CDIG, which are termed RDIG and LDIG, respectively, the following simulation procedure was used: Firstly, a separate test layout, which includes the power- and ground-routing in all metal layers except for metal-1, was drawn manually. The lowest metal layer (metal-1) was coarsened in a way that negligibly affects the power routing losses. Secondly, the capacitance CDIG was uniformly split into a rather large number of ideal lumped capacitors, which were then evenly distributed in the test layout manually. In the following, these ideal lumped capacitors and the associated part of the power-grid are termed *logic tiles*. Third, RLCK-extraction and AC-simulation was applied to this test layout, whereby the impedance characteristic of the digital part at the DVCC- and DGND-pads, which is termed $Z(\text{DVCC}, \text{DGND})$, is computed. Then, RDIG was obtained from $\text{Re}(Z(\text{DVCC}, \text{DGND}))$, and LDIG was computed from the location of the minimum of its imaginary part, which is called the self-resonance frequency. It was observed that RDIG is considerably frequency-dependent, and it was read off at 500 MHz. This frequency was selected such that the absolute impedance of the RLC-model is best matched to $|Z(\text{DVCC}, \text{DGND})|$ from DC to 1 GHz. Fourth, the impedance characteristic $Z(\text{DVCC}, \text{DGND})$ was measured using a VNA, a detailed discussion of which is beyond the scope of this thesis.¹² It was observed that the ESR at 500 MHz is quite well described by the logic tiles model. Thus, in this frequency range, it is apparently dominated by the metallization. Conversely, at lower frequencies, there was a significant disagreement between measurement and simulation: This might be due to the fact that the logic tiles model neglects, among others, the connection resistance of the p- and n-wells. However, this is thought to be of lesser importance because, below the self-resonance frequency of 460 MHz, the impedance of the digital part is mostly dominated by its capacitance.

Note that these small-signal equivalents of the digital core are based on the assumption that the impedance at the effective “junction point” of the digital disturbance source (fig. 67) is roughly equal to the impedance at DVCC

¹² In this delicate measurement, special care was taken to eliminate the contact resistance of the wafer prober. Specifically, a large number of impedance characteristics were recorded, and the curve with the lowest ESR was selected. Furthermore, the “SHORT” calibration structure was repeatedly probed, in order to rule out a calibration offset. Moreover, the selected data was crosschecked against other measurements of the IC inside the package at lower frequencies.

and DGND. At first glance, this assumption seems well justified because the disturbance source is rather well confined (see fig. 66), and it is located close to the DVCC- and DGND-pads. However, the ESR observed at this effective “junction point” might be considerably smaller, e.g. because the digital disturbance source much less localized as the connection point of the pads: Note that the disturbance source spans multiple power grid cells. In fact, sec. 6.5.6 will show that reducing RDIG from $1.11\ \Omega$ to $0.2\ \Omega$ leads to a considerably different RF-emission characteristic and is better aligned with the measurement. Moreover, the model “RLC” in fig. 67 oversimplifies the interface between the small-signal equivalent of the digital part with the p-well and the logic implant of the substrate model, i.e. PW-DIG. Even if one approximates the local supply and ground potential, and hence also the logic implant, as equipotential over a major part of the digital core, the question must be raised, which fraction of RDIG and LDIG is concentrated in the supply and ground path, respectively. In order to evaluate the significance thereof, the parameterized model $RLC(\alpha, \beta)$ in fig. 67 was introduced. An extension thereof is the model $RLCD(\alpha, \beta)$, which also includes the capacitance of the digital disturber in the “clkd = 1”-state, termed CDD¹³. A more precise approach to model the digital RF-emissions would integrate the logic tiles model described above into the substrate model. This approach would require to combine RLCK- and substrate-extraction, which is certainly possible, but this is beyond the scope of this thesis. Note that commercial tools that predict dynamic voltage drop and substrate noise in microcontrollers [85], [86] even allow to resolve the distribution of the capacitance, resistance and inductance as well as switching currents at the logic gate level.

Parasitic Model of the PCB In DPI tests (IEC 62132-4) or RF-emission tests using the 150 Ohm method (IEC 61967-4), parasitics on the PCB-level may or may not play only an important role. If care is taken that certain transfer-functions of the PCB to the IC-pin are flat, and if low-ESL blocking capacitors are used, then the PCB-model can usually be heavily simplified. The PCB designed for the test-IC has four metal layers, and the PCB ground planes (layer 2 and 3) are continuous. Moreover, the routing guideline that ground vias connecting layer 2 and 3 are to be placed near every signal via was followed [94]. This ensures a clean current return path. It should be pointed out that such ground vias were also placed near each power supply via, in order to guarantee that even the power supply traces form well-defined, mutually shielded microstrip lines.

¹³ As can be seen in the schematic of the digital disturbance source in fig. 67, this capacitance is strongly reduced “clkd = 0”-state. This shows that $RLCD(\alpha, \beta)$ neglects the time-dependence of CDD.

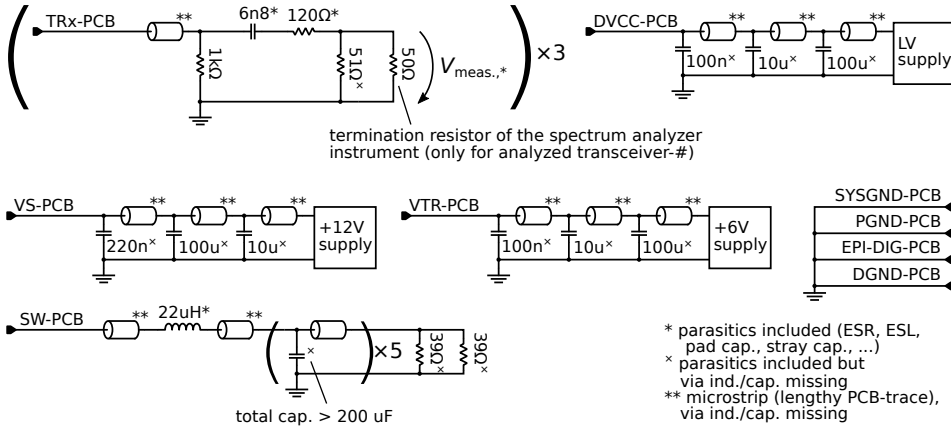


Figure 68: Circuit model of the printed circuit board, which is used for EMC predictions.

Fig. 68 shows the model of the PCB. Simple uncoupled microstrip line models were instantiated for each PCB-trace that is significantly longer than the attached SMD components. For each discrete capacitor and resistor, its ESL and ESR, as well as its capacitance to the ground plane, were modeled. The capacitance to the ground plane is predominantly due to the pads. However, the excess capacitance and inductance of vias [94] in power supply traces, at IC ground pins and at components connecting to ground are ignored in the presented PCB-model: While omitting these parasitics is *not* recommended in general, in the performed simulations, their impact on the result was small. The 50 Ω resistor at $V_{\text{meas},*}$ is not a discrete component, but it instead describes the loading of an SMA-connector by the cable and the termination resistor of the EMI receiver. The 22 uH SMD inductor of the DC/DC-converter was characterized on a test-PCB using 2-port VNA-measurements (sec. 2.4.3). An intricate model of this SMD inductor, which accounts for the multiple self-resonances of this component below 1 GHz, was created. The details are beyond the scope of this thesis. It was later found that, both, the parasitics of the SMD inductor and the parasitics of the microstrips can be completely neglected in the prediction of the RF-emissions at the transceiver pins.

Assembly of the System Model Fig. 69 shows how a system model is formed by connecting the substrate model (fig. 66, table II), the semiconductor devices (fig. 67), the package model (table I0) and the PCB model (fig. 68). If the substrate model is formed from a resistor network of the wafer-substrate (i.e. #R-CLI-*), then lumped diodes and capacitors have to be added for each n-epitaxial pocket because these are not included in these substrate models

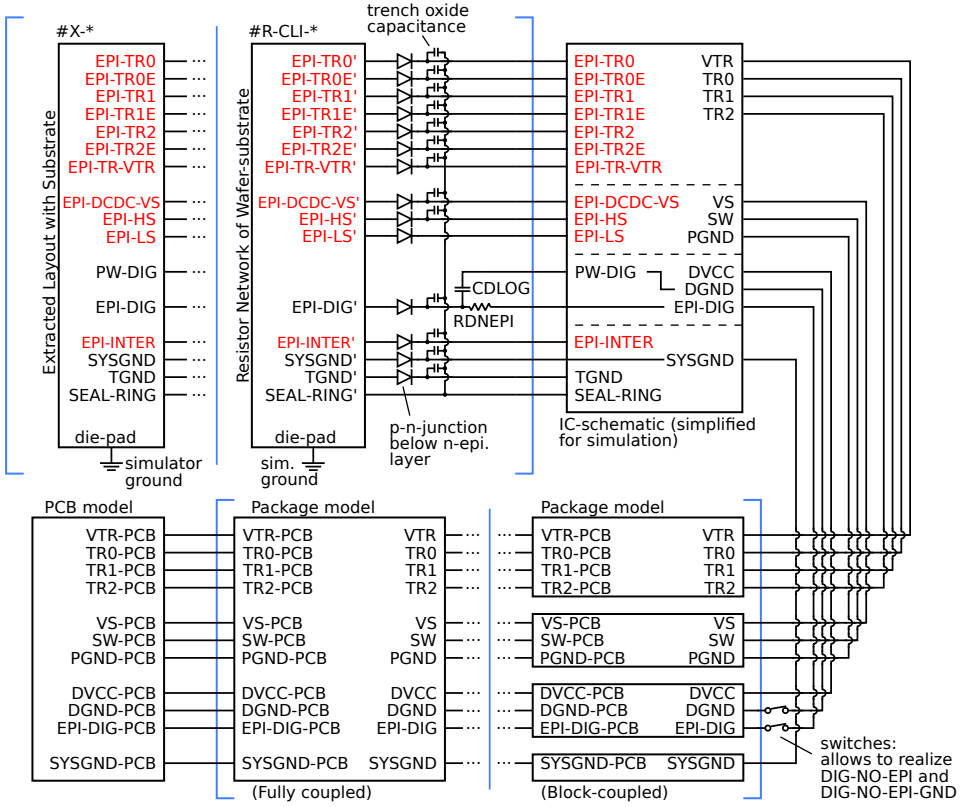


Figure 69: System model for EMC predictions, which instantiates the substrate model (fig. 66, table II), the semiconductor devices (fig. 67), the package model (table 10) and the PCB model (fig. 68). Large square brackets (blue) symbolize IF-THEN-ELSE clauses.

as such. These diodes and capacitors describe the p-n-junction below the n-epitaxial layer and the trench-oxide capacitance, respectively. Observe that no trench-oxide capacitance is added for EPI-LS: This accounts for the fact that, in the used DC/DC-design, the transistor ML is surrounded by a floating trench. All trench-oxide capacitances in fig. 69 connect to SEAL-RING because, in the substrate models #R-CLI-*, the trench filling material is a perfect conductor. Furthermore, if #R-CLI-* is used, for the digital part, one must externally add the capacitance between the logic-implant and the n-buried layer (CDLOG), as well as the effective connecting resistance of the n-buried layer (RDNEPI). CDLOG can be easily computed using the region area and the bias voltage. In order to obtain RDNEPI, AC-simulations of #X-GND were performed, and the real part impedance between EPI-DIG and PW-DIG was used. RDNEPI is presumably influenced by the n-sinker resistance, the n-buried layer's sheet resistance and the metal-routing of EPI-DIG.

By default, there is a single instance of the package model in fig. 69. This shall be referred-to by the term *fully coupled package model*. Alternatively, the package model can also be instantiated multiple times – i.e. one instance per *coupling group* of pins. In these so-called *block-coupled package models*, all couplings between ground-return inductances that cross a coupling group are removed, but the pin-loop inductances are negligibly modified. This will also be called *package coupling knock-out*, by means of which the relevance of inductive pin-couplings can be investigated. Likewise, it is possible to delete the substrate model entirely (not shown for clarity in fig. 69), which is then called *substrate coupling knock-out* in analogy¹⁴.

Despite fig. 69 appears trivial, there are some hidden subtleties: In the IC-schematic and the substrate model, the nodal voltages essentially represent an absolute electric potential ϕ_{IC} (sec. 2.5.2). In contrast, in the PCB-model, the nodal voltage represents the integral over the E -field from different points on the PCB ground plane to conductors (sec. 2.5.1). Care must be taken when interfacing these two domains, which are based on potentially conflicting voltage definitions, via the package model. The approach here is to connect the die-pad terminal¹⁵ of the substrate model to the simulator ground, which fixes the reference point of ϕ_{IC} . As elaborated in sec. 3.2.5, if this convention is used, then the die-side lumped ports in the package model must indirectly refer to the die-pad, which may require to transform the network parameters. Moreover, the package model must pose a realistic impedance to a non-zero total current that enters the IC via the pins and leaves it via the die-pad, i.e. via the simulator ground (sec. 3.1).

6.3.2 Small-Signal Analysis using the Substitution Theorem

The substitution of certain circuit blocks (large blue square brackets in fig. 67) by frequency-dependent AC sources allows to simplify the EMI prediction using comparatively fast AC-simulations. In the following, it is argued that the introduced errors by that substitution are largely negligible.

In the first step, two transient simulations of the system model (fig. 69) are performed. These are used to obtain $V_{SW,PGND}(t)$ and $I_{VS}(t)$ (fig. 67), firstly, for the plastic package, and secondly, for the ceramic package. In these transient simulations, very strong simplifications can be applied to the sub-

¹⁴ In substrate coupling knock-out, the capacitances CDLOG and RDNEPI are *not* removed. Thus, to be more specific, substrate coupling knock-out is formally a low-dimensional substrate model with the #R-CLI-***-block in fig. 69 being an empty subcircuit.

¹⁵ In general, the voltage at the die-pad terminal may not be equated with the voltage at the die backside. For example, if the die is not galvanically connected at the backside, these voltage differ.

strate and package model – more details will be provided below. Thereby, the simulation time is drastically reduced in comparison to transient simulations of the complete model. Subsequently, circuit blocks (large blue square brackets in fig. 67) are substituted by time-dependent voltage and current sources, which enforce $V_{\text{SW,PGND}}(t)$ and $I_{\text{VS}}(t)$ at the corresponding nodes and branches, respectively. Due to the *substitution theorem* [62], [143], this is an *exact equivalent transform*. This might seem surprising at first because the related Norton- and Thévenin-equivalents [62] additionally require a frequency-dependent series or parallel impedance: The difference comes from the fact that, in the Norton-equivalent, the equivalent current is determined *in shorted condition*, whereas in the substitution theorem, it is determined *already at the correct AC-load*. Note that simplifications of switching non-linear circuitry using Norton- and Thévenin-equivalents in order to predict RF-emission is quite common [13], [86], [117], [122], [145], [175], [183].

In the second step, the RF-emissions at $V_{\text{meas},*}$ (fig. 68) are predicted using AC-simulations based on $V_{\text{SW,PGND}}(t)$ and $I_{\text{VS}}(t)$ from the transient simulations.¹⁶ In these AC-simulations, the selected package- and substrate-models are different and more complex than in the preceding transient simulations – e.g., in the AC-simulations, the substrate models #X-* can be used. The following additional approximations are introduced by this approach: Firstly, the selection of a different package- and substrate-model in the AC-simulation alters the AC-load of the substituted circuit blocks. Despite $V_{\text{SW,PGND}}(t)$ and $I_{\text{VS}}(t)$ depend on the AC-load, they are not updated. However, this introduces only small errors because the spectra of $V_{\text{SW,PGND}}$ and I_{VS} are actually *very stable parameters*: They are roughly unaffected by substrate parasitics, and, in contrast to the RF-emission spectrum, small long-range mutual inductances have a negligible impact on them. This will be demonstrated below.

Secondly, AC-simulations linearize the model at a fixed operating point (see sec. 2.3). In the following, the p-n-junction between EPI-LS (see fig. 69) and the wafer-substrate is denoted by $D_{\text{EPI-LS}}$ ¹⁷. Consider the fact that $V_{\text{SW,PGND}}(t)$ has a voltage swing of roughly 12 V, and consider that $V_{\text{SW,PGND}}(t)$ is directly attached to the non-linear device $D_{\text{EPI-LS}}$. Thus, at first glance, the linearization at a fixed operating point appears to be a poor approximation. However, note that the differential capacitance of $D_{\text{EPI-LS}}$ changes only by a factor of roughly 2 when the reverse bias voltage is increased from 0 V to 12 V. Moreover, by replacing $D_{\text{EPI-LS}}$ by a constant, effective capac-

¹⁶ In phasor analysis (sec. 2.3), these time-dependent voltage and current sources can be equivalently understood as superimposed frequency-dependent sinusoidal AC-voltage and AC-current sources.

¹⁷ In the case of the substrate models #X-*, the p-n-junction is actually described by an array of diodes

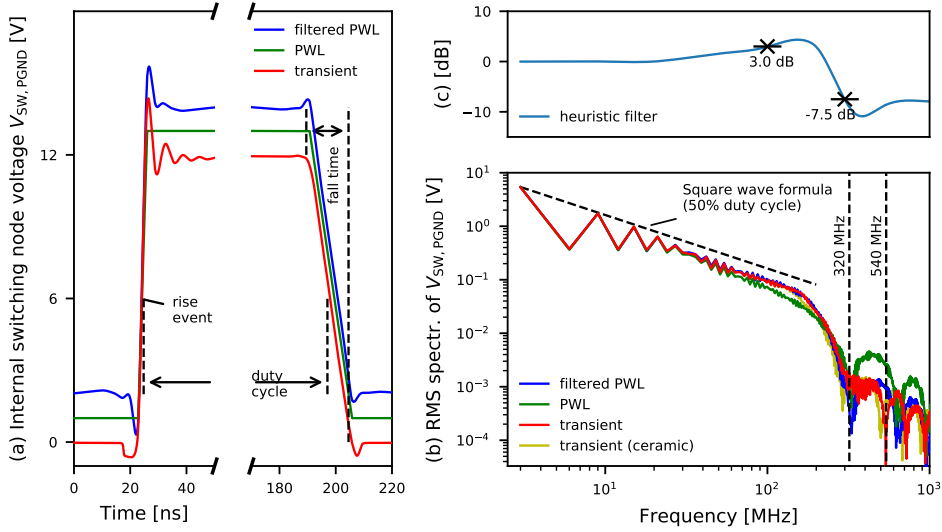


Figure 70: Red curves in (a) and (b) show the transient and the RMS-spectrum, respectively, of a single period of $V_{SW,PGND}$ in the plastic package. (The blue and green curves in (a) were offsetted in y-direction for clarity). They are obtained by applying transient analysis to fig. 69 with #R-CLI-GND and #P-EXT. The yellow curve is the corresponding result for the ceramic package. The blue curves are obtained from the green curves (PWL waveform) by applying a heuristic filter, the amplitude response of which is shown in (c).

itance $C_{EPI-LS} := Q_{EPI-LS}/12\text{ V}$, the linearization errors are reduced even further: Here, Q_{EPI-LS} is the total charge that flows across D_{EPI-LS} , when quasi-statically increasing its bias voltage from 0 V to 12 V. By this construction, the total charge injected into the wafer-substrate is correct even under linearization. It was found that this approach indeed yields quite accurate results.

The implementation developed in the course of this thesis does not actually conduct AC-simulations with frequency-dependent AC-voltage and AC-current sources. Rather, it first computes the transfer functions from $V_{SW,PGND}$, I_{VS} and I_{DDIS} to $V_{meas,*}$ using the XF-analysis (sec. 2.3.3).¹⁸ Then, the AC-voltage at $V_{meas,*}$ is obtained by applying the convolution and superposition theorems [135]. Since two terms are superimposed in the prediction of the DC/DC-converter emissions, care must be taken to correctly account for the phase of the $V_{SW,PGND}$ - and I_{VS} -spectrum, as well as for the phase of the associated transfer functions.

¹⁸ A little known property of the XF-analysis is that it simultaneously computes these three transfer functions, and thus the required effort is the same as the effort of a single AC-simulation (sec. 2.3.3).

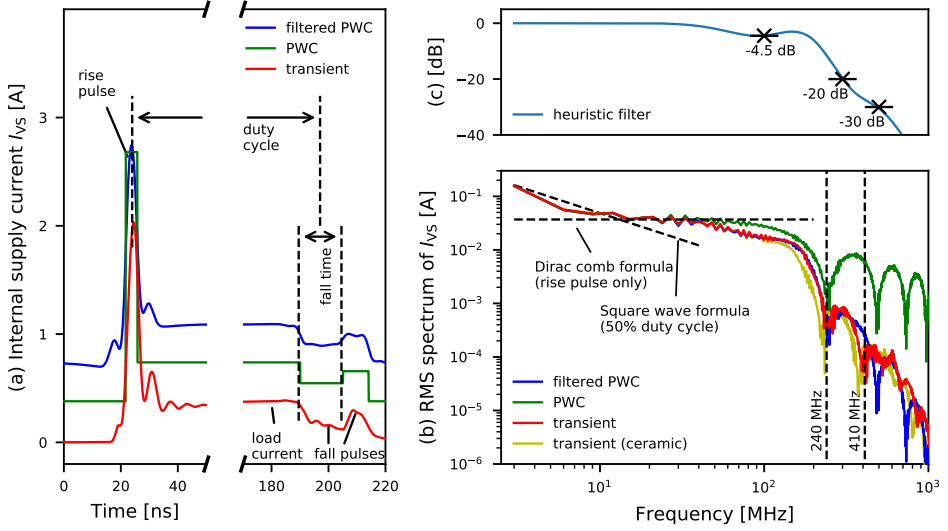


Figure 71: Red curves in (a) and (b) show the transient and the RMS-spectrum, respectively, of a single period of I_{VS} in the plastic package. (The blue and green curves in (a) were offsetted in y-direction for clarity). In other respects, this figure is analogous to fig. 70.

The red curves in fig. 70 (a) and fig. 71 (a) show a part of a $V_{SW,PGND}$ - and an I_{VS} -transient, respectively. These transients have a period of $T_{DC/DC} = 333$ ns (see sec. 6.2). The red curves in fig. 70 (b) and fig. 71 (b) show the corresponding RMS-spectra. To obtain them, a part of $V_{SW,PGND}(t)$ or $I_{VS}(t)$, respectively, was decomposed into sinusoids using the Fourier series¹⁹. To ensure a good accuracy even at very high harmonics, the smoothstep-cross-fading technique from sec. 2.7.2 is used, and special care is taken regarding the spline interpolation.

An ideal square wave with a peak-to-peak amplitude A_{p-p} , a duty cycle of 50% and an infinitesimal rise- and fall time exhibits the following Fourier series coefficients [135]:

$$c_k = \begin{cases} -i \frac{A_{p-p}}{\pi k} & \text{f. } |k| \text{ odd} \\ 0 & \text{f. } |k| \text{ even} \end{cases} \quad (99)$$

The dashed line in fig. 70 (b) is based on eq. (99) for $A_{p-p} = 12$ V. It precisely describes the odd-numbered RMS-amplitudes of the $V_{SW,PGND}$ -spectrum at low frequencies, and the deviation is less than 6 dB until roughly 150 MHz.

¹⁹ The Fast-Fourier-Transform (FFT) is used to compute c_k from eq. (21). The peak amplitude of each sinusoid is $2|c_k|$, and the RMS-spectrum is given by $\sqrt{2}|c_k|$.

Symbol	Description	Value
$t_{DC/DC, \text{rise}}^{\dagger}$	Rise time of internal switching node $V_{SW,PGND}$	3.1 ns
$t_{DC/DC, \text{fall}}$	Fall time of internal switching node $V_{SW,PGND}$	15.0 ns
$D_{DC/DC}$	Duty cycle of $V_{SW,PGND}$	0.522
$I_{DC/DC, \text{load}}$	Steady-state load current in I_{VS}	0.36 A
$Q_{DC/DC, \text{rise-pulse}}$	Area under current pulse in I_{VS} at rising edge	8.7 nC
$f_{SW, \text{min}-1}^{\dagger}$	First pronounced minimum in the spectrum of $V_{SW,PGND}$	320 MHz
$f_{VS, \text{min}-1}^{\dagger}$	First pronounced minimum in the spectrum of I_{VS}	240 MHz
$Q_{DDIS, \text{rise-pulse}}$	Area under current pulse in I_{DDIS} at rising edge	170.5 pC
$Q_{DDIS, \text{fall-pulse}}$	Area under current pulse in I_{DDIS} at falling edge	26.5 pC
All values correspond to the plastic package		
$\dagger$ values in the ceramic package differ significantly.		

 Table 12: Basic parameters of the transients and spectra of $V_{SW,PGND}$, I_{VS} and I_{DDIS} .

The Fourier series coefficients of an ideal Dirac comb with period T are given by [5], [24]:

$$c_k = \frac{Q_p}{T} \quad (100)$$

where Q_p is the area under each spike. Eq. (100) with $Q_p = Q_{DC/DC, \text{rise-pulse}}$ and $T = T_{DC/DC}$ predicts the I_{VS} -spectrum quite well between 6 MHz and 100 MHz. The 3 MHz-point in the I_{VS} -spectrum rather corresponds to a square wave spectrum with $A_{p-p} = I_{DC/DC, \text{load}}$ (table 12). This is shown by the dashed lines in fig. 71 (b).

In order to gain further understanding of the frequency characteristic of $V_{SW,PGND}$ for $f > 150$ MHz, a piecewise-linear (PWL) curve was fitted (green square wave in fig. 70 (a)). (Please keep in mind that *none* of the fitted and heuristically filtered spectra, which are presented in the following, will be used in the actual emission predictions in sec. 6.5.) The fit parameters D_{DC-DC} , $t_{DC/DC, \text{rise}}$ and $t_{DC/DC, \text{fall}}$ are found in table 12²⁰. As shown by the green curve in fig. 70 (b), the spectrum of this PWL-curve is valid until roughly 300 MHz, and, in contrast to eq. (99), it correctly predicts the even-numbered RMS-amplitudes of $V_{SW,PGND}$ at low frequencies. In analogy, a piecewise-constant

²⁰ D_{DC-DC} and $t_{DC/DC, \text{fall}}$ were fitted to the transient $V_{SW,PGND}(t)$. Conversely, $t_{DC/DC, \text{rise}}$ was set to $f_{SW, \text{min}-1}^{-1}$, such that the first pronounced minimum of the green and red RMS-spectra precisely coincide.

(PWC) waveform is fitted to I_{VS} -spectrum²¹. The spectrum of this PWC-curve is valid until roughly 200 MHz. Thus, including the basic timing parameters into these PWL/PWC-waveforms offers *only limited benefits*, and it merely increases the upper applicable frequency by a factor of two. Also note that PWL- and PWC-based spectra are capable of describing the first pronounced minima $f_{SW,min-1}$ and $f_{VS,min-1}$ (table 12), but the second pronounced minima have a significant frequency offset.

Only by applying heuristic filters (figs. 70 (c) and 71 (c)) to these PWL/PWC-curves, their validity range could be extended to 1 GHz. This is shown by the blue curves in figs. 70 (b) and 71 (b). The amplitude response of these heuristic filters was manually tuned to achieve a good agreement. Note that these heuristic filters introduce corrections to the PWL/PWC-based spectra of 7.5 dB and 20 dB, respectively, at 300 MHz. In the time domain (blue curve in fig. 70 (a)), these heuristic filters²² increase the smoothness of the PWL/PWC-curves, and they introduce ringing at the rising edge of $V_{SW,PGND}(t)$. These heuristic filter probably represent the dynamics of VS- and PGND-pin-inductances and the capacitances of MH and ML. One might proceed with the construction of a formula for their amplitude and phase responses. Related calculations can be found in literature [11], [141]. This is beyond the scope of this thesis. The EMI-predictions conducted within this chapter directly and only use the red and yellow curves from figs. 70 (b) and 71 (b).

The transient simulation used to obtain the red curves in figs. 70 and 71 is based on the #R-CLI-GND substrate model and on the #P-EXT package model. The question arises whether these transient simulations can be further simplified: A transient simulation in which the substrate couplings were removed (substrate coupling knock-out, sec. 6.3.1) resulted in $V_{SW,PGND}$ - and I_{VS} -spectra that were almost perfectly aligned (not shown here for clarity). Thus, despite MH and ML have a considerable parasitic capacitance to the wafer-substrate, it evidently has no impact on the $V_{SW,PGND}$ - and the I_{VS} -spectrum. Furthermore, presumably these spectra only depend on the two large pin-loop inductances VS→PGND and SW→PGND, as well as on their inductive coupling coefficient. Therefore, in predictions of $V_{SW,PGND}$ and I_{VS} , an almost trivial package model might be used. This is in contrast to the transfer functions, which may depend on numerous small long-range mutual inductances (see also chapter 3). Extreme caution must be taken in attempts

²¹ The durations of the fall pulses were fitted to the transient, whereas the duration of the rise pulse was obtained from the spectrum as $f_{VS,min-1}^{-1}$.

²² For simplicity, their phase response was set to zero. Despite this, the overlap in the time-domain was surprisingly good.

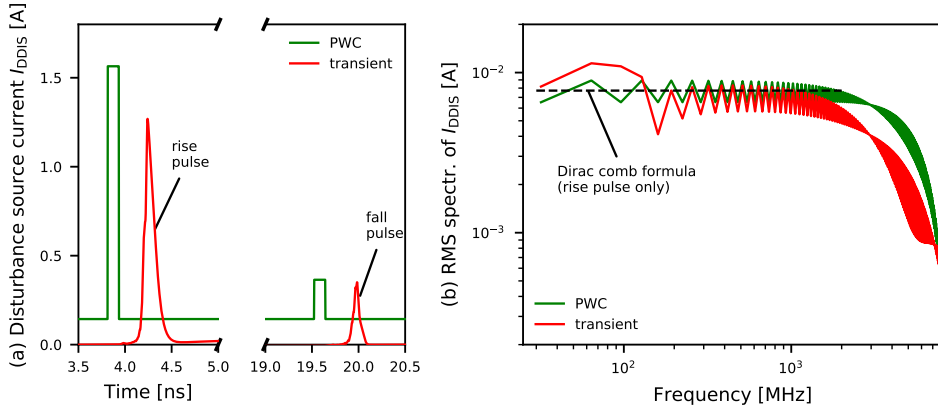


Figure 72: Red curves in (a) and (b) show the transient and the RMS-spectrum, respectively, of a single period of I_{DDIS} , obtained from a simple schematic-level model. (The green curve in (a) were offsetted in x- and y-direction for clarity).

to simplify the gate driver and logic circuits of the DC/DC-converter²³: The gate driver strength obviously has a significant impact because it affects the rise time of $V_{SW,PGND}$. Moreover, other particularities of the gate drivers might be important in the prediction of the shape and amplitude of the rise and fall pulses in fig. 71 (a). For example, the rise pulse is not only due to the ramp-up of $V_{SW,PGND}$, but it also traces the charging-process of MH's gate²⁴.

The predictions of digital RF-emissions are also based on the substitution theorem (fig. 67). In order to obtain $I_{DDIS}(t)$, transient simulation of the digital disturbance source is performed on the schematic level. These simulations also contain the inductance of the DVCC-, DGND- and EPI-DIG-pins, and their mutual inductances. Furthermore, CDIG and RDIG (fig. 67) as well as CDLOG and RDNEPI (fig. 69) are included. It was found that these package and substrate parasitics can be neglected between 200 MHz and 2 GHz, and have only a moderate influence of harmonics #1 to #6 and on the spectrum beyond 2 GHz. This is related to the fact that the shape of the current spikes in $I_{DDIS}(t)$ is mostly immune to small voltage drop in (DVCC, DGND). The transient of I_{DDIS} , which has a period of $T_{DDIS} = 31.25$ ns (sec. 6.2), and its RMS-spectrum is shown in fig. 72. The Dirac comb model eq. (100) with $Q_p = Q_{DDIS, \text{rise-pulse}}$ and $T = T_{DDIS}$ is shown by the dashed line. It predicts the transient data rather well up to 2 GHz because the current spikes are

²³ In the implementation developed in the course of this thesis, indeed the complete schematic of the custom PWM-generator, startup- and shutdown-logic and of the gate drivers is instantiated (fig. 67)

²⁴ In comparison, the first fall pulse in I_{VS} is due to the ramp-down of $V_{SW,PGND}$, and the second fall pulse is due to the charging of ML's gate.

extremely brief. Moreover, a PWC-model (green curve) can approximate this data even up to 8 GHz. However, preliminary transient simulations based on RC-extraction have indicated that the accuracy of the schematic-level simulation (red curve) is poor beyond 2 GHz. Note that I_{DDIS} may not be equated with the current through the power supply pin $I_{DIG,BW}$ from fig. 67.

The substitution of the digital disturber described above is comparably simple because it assumes that it is connected to the digital core only at a single junction point (see fig. 67). However, even in this rather simple digital disturber, this assumption is not entirely accurate (sec. 6.3.1), and it is inapplicable to productive ICs, in which the switching gates are distributed over a larger part of the digital core. To predict RF-emissions from highly distributed switching currents, the following approach is proposed instead²⁵: Each logic cell in the digital part shall be represented by a transient current source and an array of effective capacitors connecting power, ground, p-wells and n-wells. Note that the logic activity pattern, e.g. due to the executed program in the case of a microcontroller, must be known to determine these current sources. A common solution in dynamic voltage drop analysis is to perform HDL-based gate-level simulations, and then to convolve the resulting distribution of the switching events with PWL current spikes [85], [145]. Subsequently, the power grid shall be described using a detailed RLC-model. To simplify this model, so-called *logic tiles* (see also sec. 6.3.1), which span multiple power grid cells, shall locally cumulate a large number of logic gates. These logic tiles are formally multi-terminal Norton-equivalents of the contained power grid, parasitic capacitors and the current sources. Similar constructions can be found in literature regarding the EMC of microcontrollers (“internal activity sub-model”) [117], [145]. The commercial tool Ansys RedHawk introduces the related term *chip power model* [85], [86]

6.4 Measurements of the Absolute Fourier Series Coefficients in the Presence of Clock Jitter, Switching and Random Noise

The emissions at the transceiver pins are decoupled via the 150 Ω method (IEC 61967-4). Their spectrum is measured using the R&S ESW-8 EMI-receiver [154] (sec. 2.7.1). The EMI-receiver essentially records the spectrum of $V_{meas,*}$ in fig. 68. As discussed in sec. 2.7.3, measured spectral peak amplitudes *cannot* be directly equated with the Fourier series coefficients of a single EMI-period. This is because the measured spectrum is potentially affected by the phase

²⁵ The evaluation of this approach in the context of a Smart Power IC could be addressed by future research.

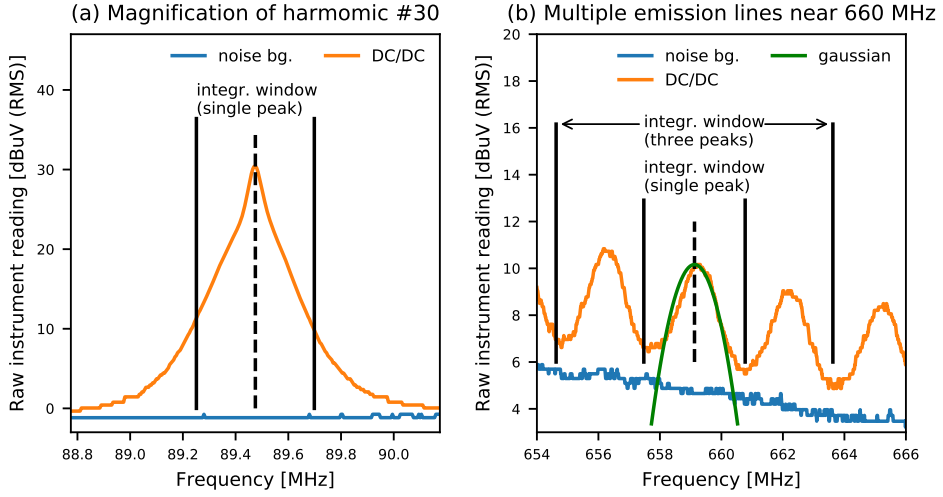


Figure 73: Small excerpts from the measured raw readings of the EMI-receiver, attached to transceiver #1. The emission lines are due to the operation of the DC/DC-converter clocked at $f_{\text{base}} = 3$ MHz.

noise of the clock source. One approach would be to translate the simulated Fourier series into predictions of EMI-receiver readings using the procedure from sec. 2.7.3. This would require to characterize the phase noise of the phase-locked loop in the central functions module (see sec. 6.2 and fig. 63). However, this chapter rather takes the inverse approach: The Fourier series of a single EMI-period are recovered from the measured spectrum by integrating each peak's power, as described below. This step eliminates the unwanted phase noise from the measurement data. Thereby, a more clean data representation is obtained, which simplifies the subsequent evaluations in sec. 6.5.

The R&S ESW-8 EMI-receiver was configured to use a Gaussian filter and an RMS-detector. Furthermore, the filters have sufficient overlap: Specifically, the frequency spacing Δf equals $f_{\text{BW}}/4$, where f_{BW} is the 3 dB-bandwidth of the Gaussian filters. This configuration allows to recover the absolute value of the Fourier series coefficients $|c_k|$ using eq. (38) from sec. 2.7.3. The correction factor $G_0 B_N / \Delta f$ was theoretically predicted to be $2\sqrt{\pi / \log 2}$. This was verified experimentally by measuring multiple frequency-modulated sine wave signals, with different modulation indices and frequency deviations.

The orange curve in fig. 73 (a) shows a magnified section of some raw instrument readings at the 30-th harmonic of the DC/DC-converter. The sum in eq. (38) ranges over the depicted integration window, and left hand side of eq. (38) for the k -th harmonic will be denoted by F_k . A rather high frequency

resolution is used, such that f_{BW} is between $4 \cdot 10^{-4} f$ and $4 \cdot 10^{-5} f$.²⁶ This is important to minimize the integration windows and to separate very high harmonics of the DC/DC-converter. Each integration window spans only $f_{\text{harm}} \pm 0.25\% \cdot f_{\text{harm}}$, where f_{harm} is the harmonic's peak frequency (dashed vertical line). Minimizing the integration window size is important to reduce the offset error due to the background noise. The drawback is that the base frequency f_{base} must be known very precisely in order to locate these narrow integration windows. It turned out that, due to a random drift of the phase-locked loop, f_{base} needs to be continuously re-calibrated during an ascending-frequency search that localizes the peak frequencies.

The green curve in fig. 73 (b) shows a Gaussian fit to a measured power spectrum of the DC/DC-converter (the standard deviation will be denoted by σ). The depicted peak frequency is the critical frequency at which the peak separation equals 4σ . Thus, at higher frequencies, individual emission lines of the DC/DC-converter cannot be resolved any more. For DC/DC-emissions at $f > 500$ MHz, instead, three-peak integration windows (fig. 73 (b)), each spanning $\pm 1.5 f_{\text{base}}$, are processed. A third of the integrated power is then used as the estimate for F_k . Nevertheless, it is impressive that individual emission lines of the DC/DC-converter can be resolved up to the 220-th harmonic. This is enabled by the developed custom PWM-generator (sec. 6.2) – presumably the phase noise would be much larger if the DC/DC's regulation loop was not removed.

The data evaluation procedure subtracts the background noise from the measurement data, as will be explained in the following: In addition to the RF-emission spectrum, *two* background spectra are recorded. Firstly, in the measurement of the *background noise spectrum*, the test-IC is in a static state. These instrument readings (blue curve in fig. 73) represent electrical noise from the circuit and from the instrument itself. Secondly, in the measurement of the *switching background spectrum*, the test-IC is clocked²⁷, but the power stage of the DC/DC-converter and the digital disturbance source, respectively, are disabled. Thus, in the switching background spectrum, some weak spurious emission lines may be superimposed on the noise floor. These two background spectra will be integrated over the same integration windows, and the left hand side of eq. (38) will be denoted by N_k and S_k , respectively. Then, in the first step, the background noise power N_k is subtracted from

²⁶ This is in contrast to CISPR-16-1-1-compliant measurements: In the CISPR band C [28], [29], f_{BW} is typically 120 kHz, whereas the measurements in this chapter are conducted using, e.g., $f_{BW} = 20$ kHz at $f = 100$ MHz.

²⁷ That is, the oscillator, the PLL, a part of the digital core, the clock-dividers, the clock level shifters and buffers are running.

F_k and S_k , respectively, and the resulting power measures are converted into RMS-voltage amplitudes $\sqrt{2}|c_k^{(F)}|$ and $\sqrt{2}|c_k^{(S)}|$, respectively:

$$\sqrt{2}|c_k^{(F)}| = \sqrt{F_k - N_k \pm c\sqrt{2}\sigma_k^{(N)}} \quad \sqrt{2}|c_k^{(S)}| = \sqrt{S_k - N_k \pm c\sqrt{2}\sigma_k^{(N)}} \quad (101)$$

where $\sigma_k^{(N)}$ is an estimate of the standard deviation of N_k , and c is a constant used to set the confidence level²⁸. In the second step, the confidence interval of $|c_k|$ is estimated using $|c_k^{(F)}|$ and $|c_k^{(S)}|$ as follows:

$$\sqrt{2}|c_k| = \sqrt{2}|c_k^{(F)}| \pm \sqrt{2}|c_k^{(S)}| \quad (102)$$

Note that the best guess of the single-period RMS-voltage amplitude $\sqrt{2}|c_k|$ does not differ from $\sqrt{2}|c_k^{(F)}|$, but only the confidence interval is enlarged: As opposed to the background noise, one *may not* subtract the switching background from the data. That is because the relative phase between $c_k^{(F)}$ and $c_k^{(S)}$ is unknown, and they might as well interfere destructively. While this might appear as a rather theoretical objection, it is indeed simple to construct a practical example: For example, assume $c_k^{(F)}$ is due to current spikes at the rising clock edge, whereas $c_k^{(S)}$ is due to current spikes at the falling clock edge. Then, for odd k , the complex numbers $c_k^{(F)}$ and $c_k^{(S)}$ have an opposing sign, whereas in all even-numbered harmonics, their phases are equally aligned.

In practice, the PEAK-detector often used, and the RMS-detector plays a lesser role. Thus, in the course of debugging EMI-simulations, EMC engineers might rather want to compute $|c_k|$ from PEAK-detector readings because these are readily available. At first glance it appears that this is easily achieved by reading off the local maxima from the PEAK-detector-spectrum. In the following, this metric will be denoted by PEAK(PEAK). Indeed, it is easily shown that for an FM sine signal, PEAK(PEAK) is correct if either the modulation frequency f_m or the frequency deviation f_Δ is smaller than the filter bandwidth f_{BW} . However, for example with $f_\Delta = 10f_{BW}$ and $f_m = f_{BW}$, the PEAK(PEAK)-value is too small by 10 dB. This was predicted using the algorithms from sec. 2.7.1 and also verified experimentally²⁹. Therefore, the use of e.g. PEAK(PEAK) is not recommended. It is important to understand that *only RMS-detector-spectra* allow to exactly recover the Fourier series coefficients

²⁸ A 2-sigma confidence interval is used, i.e. $c := 2$. The additional factor $\sqrt{2}$ accounts for the fact that the statistical error $\sigma_k^{(N)}$ occurs, both, in F_k (or S_k , respectively) and N_k .

²⁹ Similar results can be found in [142].

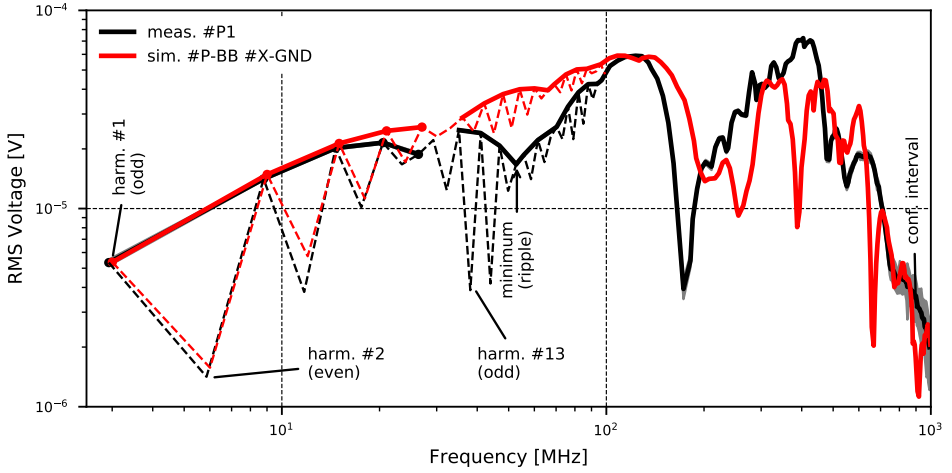


Figure 74: RF-emissions at transceiver #0 caused by the operation of the DC/DC-converter. The measurement results of sample #P1 (black curves) show the RMS-voltage amplitudes $\sqrt{2}|c_k|$, recovered using the emission-peak integration method described above. The dashed curves connect all available data points, either from simulation (red) or measurement (black). Conversely, the solid curves exemplify the proposed unusual data presentation, in which only some selected even or odd harmonics are connected.

of a single EMI-period. This is due to distinguished mathematical properties of the RMS detector, i.e. Parseval's theorem (sec. 2.7.2).

In RF-emissions of the DC/DC-converter that are dominated by the transfer of noise from $V_{SW,PGND}$, a pronounced ripple between even and odd harmonics is observed below 100 MHz. This is depicted by the dashed curves in fig. 74. This is related to the fact that, for an idealized duty cycle of exactly 50%, all even harmonics of $V_{SW,PGND}$ would be exactly zero (eq. (99))³⁰. The prediction of this ripple effect is complicated by the fact that it is very sensitive to slight deviations of the duty cycle. For example, at harmonic #13, the dashed red and black curves deviate strongly. Therefore, in the remainder of this chapter, following the data presentation is instead used to visualize the RF-emissions of the DC/DC-converter: Below 30 MHz only the odd harmonics are shown and connected by a curve. Above 30 MHz, subsequent even and odd harmonics are grouped into pairs – then, the data point with the smaller RMS-voltage is deleted from each pair, and the remaining data points are connected by a curve. This is exemplified by the solid red and black curves in fig. 74. Thereby, the ripple effect is mostly removed, except that some weak local minima remain, e.g., at 53 MHz. Such hull-curves are, of course, equally adequate to assess the RF-emissions, e.g., with respect to the EMI limit values.

³⁰ Above 200 MHz also a ripple in I_{VS} can lead to similar, but less pronounced artifacts.

Note that the confidence interval according to eq. (102), which is depicted by the shaded gray region, is negligible below 700 MHz in this case. The reproducibility of these curves was substantially below ± 0.5 dB up to 1 GHz, albeit, in some rare cases, repeated measurement yielded inexplicable outliers. These outlier curves were blacklisted, and they will not be analyzed in the following.

6.5 Empirical Study of the Measurement and Simulation Results

6.5.1 The Accuracy Achieved in the DC/DC-converter's RF-emissions, and Differentiation between Substrate-, Package-, I_{VS} - and $V_{SW,PGND}$ -dominated RF-emissions

Fig. 75 compares the measurement results of #P1 (black curve) to simulation (red curve) below 200 MHz.³¹ Observe that for all transceivers and in both bus states, the EMI limit values (dashed black curve) [10] are violated.³² The deviation between measurement and simulation is typically no more than ± 6 dB, with a worst case of 5.8 dB at transceiver #2 (ON) at 150 MHz. An exception is at transceiver #0 (ON) between 15 MHz and 45 MHz, where the deviation was larger than 10 dB. It turns out that this is a rare special case, as will be explained in the next paragraph.

Substrate- vs. Package-Emissions, I_{VS} - vs. $V_{SW,PGND}$ -Dominance, and Destructive Interference The green curve in fig. 75 shows the simulation result for package knock-out (sec. 6.3.1), i.e. it represents substrate couplings only. Conversely, the blue curve represents the substrate knock-out. It was verified that a combination of substrate and package knock-out results in negligible RF-emissions, and hence there is *no* third significant coupling mechanism in the model. A frequency range is called *substrate-dominated* if the package knock-out curve (green) is more than 6 dB above the substrate knock-out curve (blue). Conversely, the term *package-dominated* RF-emissions shall be used if the green curve is more than 6 dB *below* the blue curve. In fig. 75, substrate- and package-dominated frequency domains are marked by the green and blue bars, respectively. Another classification distinguishes between $V_{SW,PGND}$ - and I_{VS} -dominated RF-emissions: E.g. a frequency range is called $V_{SW,PGND}$ -

³¹ The measurement approach, the post-processing and the data presentation was described in sec. 6.4. The shaded region is the confidence interval according to eq. (102).

³² However, this comparison is rather conservative because the phase noise of the clock source was neglected. Spread spectrum modulation might reduce the RF-emissions by 10 dB if measured using a PEAK-detector (sec. 6.4). This which would shift the emissions of e.g. transceiver #1 (OFF) below the limit line.

dominated if, in the superposition of transfer functions (see sec. 6.3.2), the $V_{SW,PGND}$ -term is more than 6 dB greater than the I_{VS} -term in magnitude. This is depicted by the yellow and magenta bars, respectively, in fig. 75. The black bars labeled “d.i.” indicate a *destructive interference* between package and substrate or between the $V_{SW,PGND}$ - and the I_{VS} -term, respectively. For example, destructive interference between package and substrate shall refer to the red curve being more than 6 dB below, both, the blue and the green curve. The large prediction errors of > 10 dB in transceiver #0 (ON) between 15 MHz and 45 MHz are due to destructive interference: Here, the substrate-dominated $V_{SW,PGND}$ -term and the package-dominated I_{VS} -term are similar in magnitude but of opposing phase³³. Apparently, this coincidental fine tuning is not as pronounced in the measurement, which explains the deviation.

Fig. 76 compares the measurement results of #PI (black curve) to simulation (red curve) above 100 MHz. In contrast to the low-frequency RF-emission characteristic discussed above, in this frequency range, multiple local extrema are observed. Unfortunately, the simulation predicts some pronounced local minima which were not observed experimentally. Near these spurious minima the simulation underestimates the RF-emissions by more than 6 dB. Apart from this, a prediction accuracy of ± 6 dB was achieved above 100 MHz as well.

Discussion of the Local Extrema of the RF-emissions above 100 MHz, and Analysis of the Spurious Minima Some extrema of the simulation data (red curve) in fig. 76 have been labeled as follows: Firstly, all pronounced minima have been identified in the spectra of $V_{SW,PGND}$ and I_{VS} (sec. 6.3.2). Secondly, extrema in the transfer functions from $V_{SW,PGND}$ and I_{VS} , respectively, (sec. 6.3.2) have been tabulated. The minima and maxima in these transfer functions are interpreted resonances and anti-resonances, respectively. Now, consider a I_{VS} - or $V_{SW,PGND}$ -dominated frequency range: Here, both, the minima in the I_{VS} - or $V_{SW,PGND}$ -spectrum, respectively, as well as the extrema in the associated transfer function are reflected in the RF-emission characteristic. These features were labeled exhaustively. In the used naming scheme, the prefix “IM” indicates a minimum in the I_{VS} -spectrum and “VAR” is an anti-resonance in the $V_{SW,PGND}$ transfer function³⁴. Finally, local minima in the predicted RF-emissions that are due to destructive interference between the I_{VS} - and $V_{SW,PGND}$ -term are denoted by the prefix “DI”.

³³ As shown by the dashed red and black curves, in this case, the destructive interference only affects the odd-numbered harmonics.

³⁴ By analogy, e.g. “VM” indicates a minimum in the $V_{SW,PGND}$ -spectrum, “VR” is a resonance in the $V_{SW,PGND}$ -transfer, et cetera. However, these labels do not occur since such features were not found in the red curve.

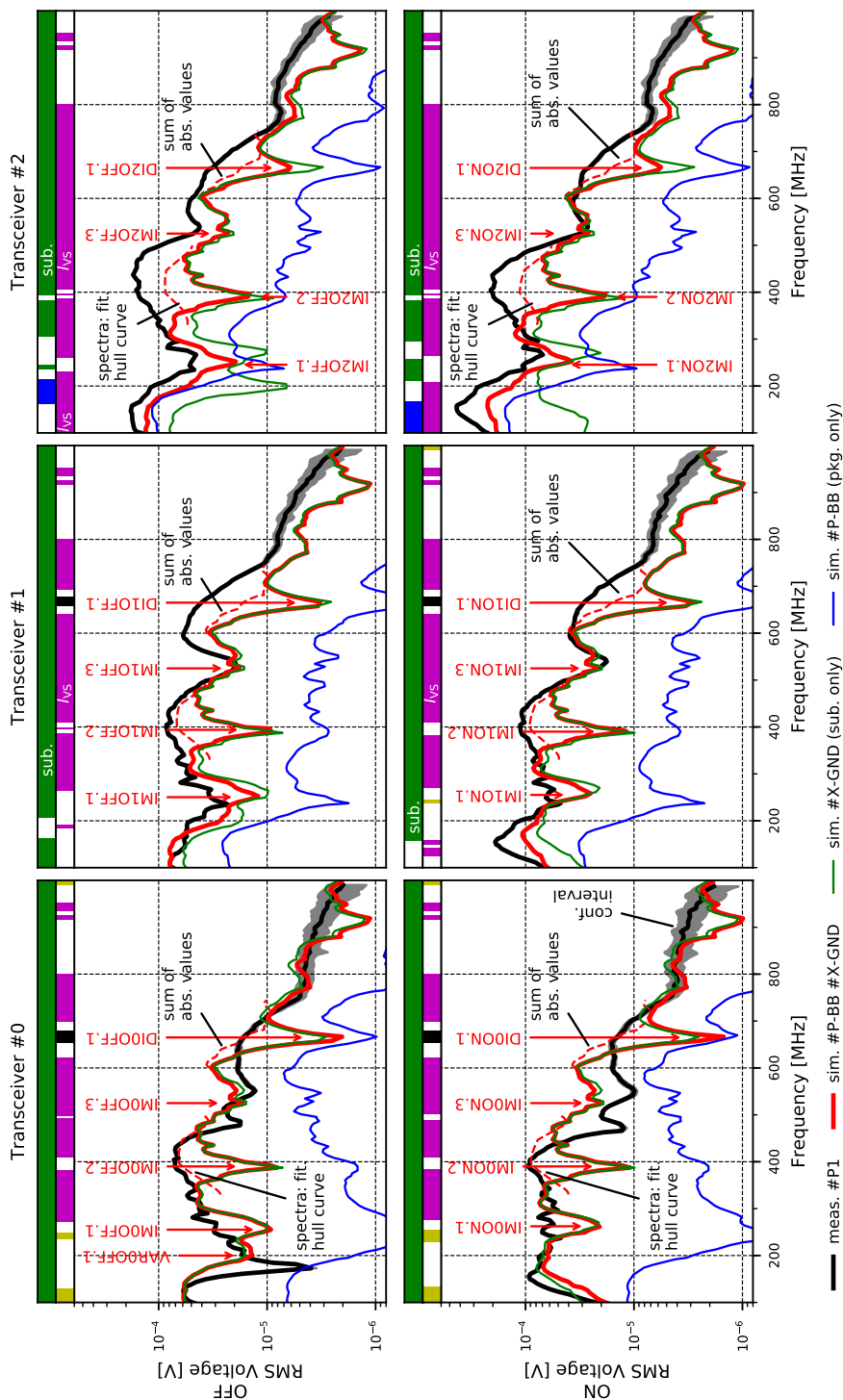


Figure 76: RF-emissions above 100 MHz at the three different transceiver pins (columns) and in two different bus states (rows), caused by the operation of the DC/DC converter. This data corresponds to the packaging variant #P1.

Surprisingly, none of the maxima in the predicted RF-emissions (red curves) was associated with a resonance: Rather, the maxima have no particular meaning and merely emerge in-between two minima, which are mostly due to nulls in the I_{VS} - or $V_{SW,PGND}$ -spectra. The location of the features IM*.1 and IM*.3 are consistent between measurement and simulation³⁵. In contrast, the predicted features IM*.2 and DI*.1 were not observed in measurement. It is not clear how the simulation prediction of I_{VS} can be improved in order to avoid the phony minimum IM*.2. Thus, instead, it is proposed to replace the spectrum of I_{VS} by a suitable hull-curve, by which it is avoided that the RF-emissions are underestimated. The feasibility of this approach is demonstrated by the dashed red curve in fig. 76 in the range [330 MHz, 500 MHz]. A heuristic solution for phony destructive interferences like DI*.1 and the large prediction errors in transceiver #0 (ON) can also be proposed: The superposition of transfer functions (see sec. 6.3.2) can be modified by discarding the terms' phases. This results in a certain upper bound (dashed red curve in fig. 76 in the range [600 MHz, 750 MHz]). In all following plots (sec. 6.5.2 – sec. 6.6.3), *neither* will hull curves for I_{VS} and $V_{SW,PGND}$ be used, *nor* will the phases be discarded.

Distance- and the State-Dependence of the Substrate- and Package-Emissions It can be seen that the substrate-emissions below 200 MHz (green curve in fig. 75) are larger in the OFF-state than in the ON-state. Conversely, the package-emissions (blue curve) are increased in the ON-state. In contrast to the frequency range < 200 MHz, for $f > 200$ MHz (fig. 76), both substrate- and package-emissions are mostly independent of the bus state. When increasing the distance to the DC/DC-converter, the package-emissions below 200 MHz (fig. 75) decrease rapidly, whereas the substrate-emissions don't decrease as much. A quantitative analysis of this effect is found in sec. 6.6.1, and the theoretical background is provided in sec. 6.7. The observation that the substrate-emissions are mostly independent of the distance of the transceiver applies to frequencies above 200 MHz as well (green curves in fig. 76). Thus, since the RF-emissions above 200 MHz (red curves) are typically substrate-dominated, their distance-dependence is weak.

Correlation between Package/Substrate-Dominance and $I_{VS}/V_{SW,PGND}$ -Dominance In fig. 75, observe that, below 200 MHz, substrate-emissions are predominantly caused by $V_{SW,PGND}$, whereas package-emissions are predominantly caused by I_{VS} . This is very intuitive: The voltage-ripple in the SW-node capacitively injects parasitic currents into the wafer-substrate at ML

³⁵ However, in measurements of transceiver #0, IM*.1 is not as pronounced as in simulation. Conversely, in transceiver #2 the alignment is better.

(fig. 67). In addition, the current-ripple across the VS-PGND-loop directly induces interference voltages at the transceiver output pins via the IC-package. This low-frequency behavior will be described using two simple circuit models in sec. 6.7. However, above 200 MHz (fig. 76), predominantly I_{VS} couples to the transceiver via the *substrate*. As will be further elaborated in sec. 6.7, this can be understood as follows: Firstly, the package-inductance of the VS-PGND pin-loop converts I_{VS} into voltage ripples at the VS-, SW- and PGND-nodes. Secondly, this provokes parasitic current into the wafer-substrate, due to the fact that the n-epitaxial layer of ML and ML (fig. 67) are connected to VS and SW, respectively.

Conclusion Spurious destructive interference constitute a problem, and, in one case, this caused an error > 10 dB between 15 MHz and 45 MHz. A related issue are spurious local minima in the current spectrum I_{VS} . Both issues *cannot* be easily fixed by drawing a hull curve over the RF-emission spectrum because the erroneous drop can be potentially very broad, and because it can coincide with a maximum of the true RF-emission curve. A better heuristic solution, which was tested above, introduces heuristic hull curves for I_{VS} and $V_{SW,PGND}$, and additionally discards the transfer function phase. This approach can globally achieve an accuracy of ± 6 dB, which is considered sufficient. In addition, one should use substrate and package knock-out tests to screen for destructive interferences between package and substrate. However, yet other spurious destructive interferences might occur within the AC-simulation itself, and bridging over minima in I_{VS} might still underestimate the true I_{VS} -spectrum. A more general countermeasure against coincidental parameter matching might be a Monte-Carlo procedure that varies global parameters such as the rise time, the bond-wire dimensions and the substrate conductivity.

It was shown that one may *not* simply understand substrate-emissions as a transfer of the $V_{SW,PGND}$ -ripple via the wafer-substrate. In fact, above 200 MHz, the more relevant substrate noise source is the dynamic voltage drop caused by I_{VS} over the package inductances.

The best evaluation scenario for substrate-emissions is transceiver #0 (OFF) because here the substrate-emissions are e.g. 19 dB above the package-emissions at 100 MHz. Conversely, for studying package-emissions, the ON-state, in particular transceiver #2 (ON), should be used: In transceiver #2 (ON), package-emissions are 14 dB larger than the substrate-emissions at 100 MHz.

6.5.2 The Impact of Die-Backside Connection on the Propagation of RF-disturbances via the Substrate

Fig. 77 shows the RF-emissions in the packaging variants with altered die-backside – that is #PIS (non-connected silicon backside), #P1M (non-connected metallized backside) and #P5 (electrically undefined backside). Since backside grounding affects the propagation of RF-disturbances via the substrate, transceiver #0 (OFF) was selected for this benchmark. Both in #P5 and #PIS, the die-backside is modeled as a distributed capacitance (see sec. 6.3.1), however with a very different capacitance per area, i.e. $43 \frac{\text{pF}}{\text{mm}^2}$ and $59 \frac{\text{fF}}{\text{mm}^2}$, respectively. The backside capacitance per area of $C_{\text{bs}} = 59 \frac{\text{fF}}{\text{mm}^2}$ results from the parallel-plate capacitor formula and the depth of the milled groove (sec. 6.2).

The Non-Connected vs. The Grounded Die-Backside The good agreement between the solid and the dashed blue curve in fig. 77 validates the developed methodology in the case of an non-connected backside. In the developed test-IC, backside grounding results in a reduction of substrate-coupled RF-emissions by 11 dB at 10 MHz and 5.5 dB at 800 MHz. This is well predicted by the conducted simulations.³⁶ Note that these figures considerably understate the benefit of die-backside grounding because the sample's die thickness of 600 μm is rather large – as will be shown in sec. 6.6.2 (i.e.

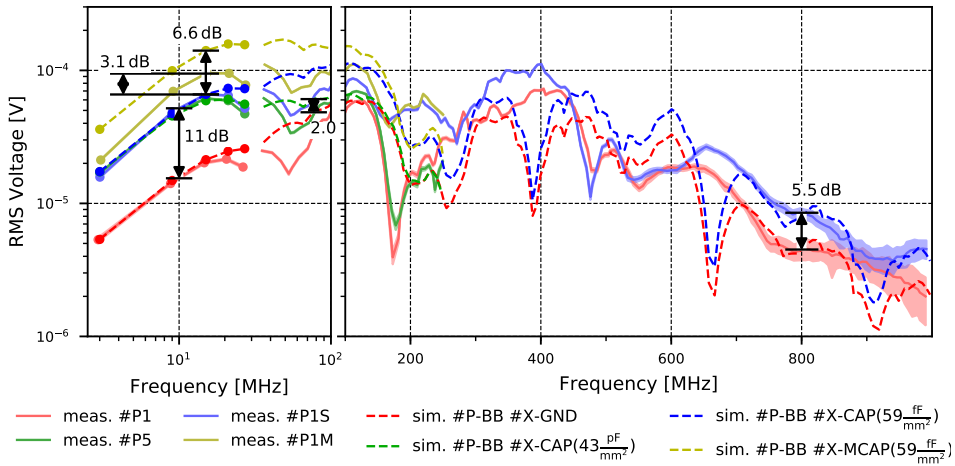


Figure 77: Comparison between different die-backside connections in measurement (solid curves) and simulation (dashed curves). This graph shows various predicted/measured RF-emissions at transceiver #0 (OFF), caused by the operation of the DC/DC converter.

³⁶ An exception is the range from 410 MHz to 610 MHz, in which the reduction due to backside-grounding is virtually zero: This is not predicted correctly.

fig. 86 (b)), for a die thickness of 220 μm , the reduction would instead be 20 dB at 10 MHz and 12 dB at 800 MHz. The fact that backside-grounding can reduce substrate-propagated RF-emissions in Smart Power ICs is already known [50]. It is new, though, that a precise prediction of this effect was achieved in simulation, and that this effect is now better understood (see sec. 6.7).

The Electrically Undefined Die-Backside and the Capacitively-Connected Die-Backside in General The backside resistance of a large-area HV-device can be thought to form a series connection with the corresponding fraction of the backside capacitance. This leads to the following corner frequency:

$$f_{\text{crit,bs}} = \frac{1}{2\pi\rho_{\text{sub}}H_{\text{die}}C_{\text{bs}}} \quad (103)$$

Given a die thickness of $H_{\text{die}} = 600 \mu\text{m}$ and for $C_{\text{bs}} = 43 \frac{\text{pF}}{\text{mm}^2}$, the corner frequency is $f_{\text{crit,bs}} = 77 \text{ MHz}$. Thus, for the electrically undefined backside (sample #P5, green curve in fig. 77), the large backside capacitance is not negligible. At 77 MHz, the prediction of #P5 (dashed green curve) is larger than the prediction of #P1 (dashed red curve) by roughly 2.0 dB. For larger frequencies, the RF-emissions of #P5 (green curves) converge to #P1 (red curves), whereas for $f \ll f_{\text{crit,bs}}$, the RF-emissions of #P5 approach #PIS (blue curves). This is fully consistent between simulation and measurement. This discussion shows that only for $f < f_{\text{crit,bs}}$, the switchover from an electrically-undefined backside (#P5) to proper galvanic backside grounding (#P1) significantly reduces the RF-emissions.

Conversely, for $C_{\text{bs}} = 59 \frac{\text{fF}}{\text{mm}^2}$, the corner frequency from eq. (103) is much larger than 1 GHz. Hence, the very small backside capacitance of the #PIS-sample is clearly negligible. In fact, it was found that a curve almost identical to the dashed blue curve in fig. 77 could be obtained using #P-BB combined with #X-NC (not shown for clarity). Thus, in the following, the substrate model #X-NC will be used to model the sample #PIS.

The Metallization and The Die-Attach Glue in a Non-Connected Die-Backside For a non-connected but *shorted* die-backside, the simulation (dashed yellow curve in fig. 77) predicts an increase in the RF-emissions by 6.6 dB at 15 MHz. In contrast, experimentally, the RF-emissions of the #PIM-sample (solid yellow curve) were elevated by only 3.1 dB. This suggests that the sheet resistance of the backside metallization and of the die attach glue in #PIM should not be approximated as a perfect electrical conductor. Nevertheless, this shows that, even if the IC-package does not feature an

exposed pad, it is advisable to model the glue at the die-backside. Above 200 MHz, the difference between #PIM and #PIS is mostly negligible, both in simulation and measurement (curves were truncated above 250 MHz for presentability).

6.5.3 Relevance Estimation of Various Substrate Parasitics and the Accuracy of the Low-Dimensional Substrate Models

Fig. 78 provides a relevance estimation of various substrate parasitic elements. The red curve shows the simulation prediction with all parasitics enabled, and the dashed black curve represents the complete substrate-knockout. In the remaining dashed curves, only a single type of parasitic element was removed selectively.

Relevance of C_{SUB} and C_{TRENCH} In the dashed yellow curve, only the capacitances between the n-buried layer and the wafer-substrate C_{sub} (table 1) have been removed. Up to 280 MHz, the C_{sub} -knockout (dashed yellow curve) drops down to the package-emissions (dashed black curve), which clearly shows the very high significance of C_{sub} ³⁷. However, above 380 MHz, remov-

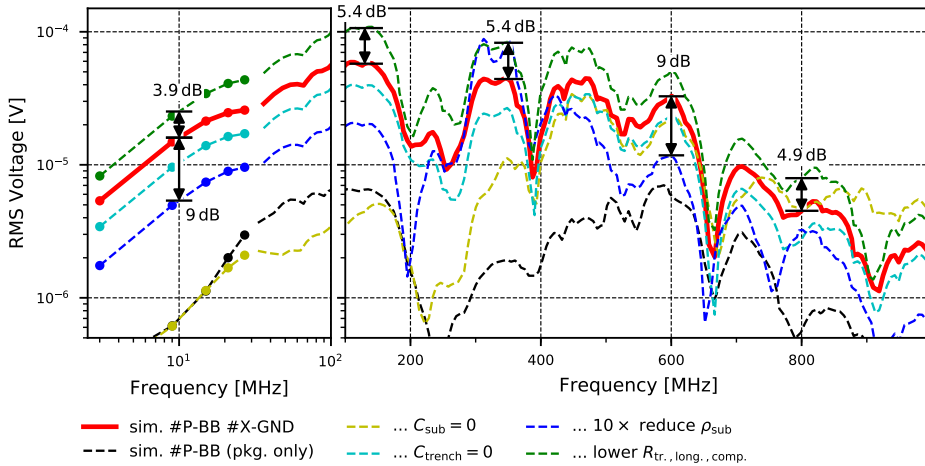


Figure 78: In the dashed yellow, cyan, green and blue curves, which are variants of the red curve (sim. #P-BB #X-GND), a subset of the substrate parasitics have been deleted or scaled. This graph compares various simulated RF-emissions at transceiver #0 (OFF), caused by the operation of the DC/DC converter in the packaging-variant #P1.

³⁷ Observe that, around 100 MHz, the C_{sub} -knockout (dashed yellow curve) is even below the package-emissions (dashed black curve). This could be ascribed to a coincidental destructive interference between substrate and package.

ing either C_{sub} (dashed yellow curve) or C_{trench} (dashed cyan curve) typically only decreases the RF-emissions by 3 dB – 6 dB. Conversely, removing both C_{sub} and C_{trench} is indistinguishable from a complete substrate knock-out (not shown for clarity). This shows that, above 380 MHz, the substrate noise transfer of n-epitaxial pockets is facilitated in roughly equal parts by C_{sub} and C_{trench} .

Relevance of $R_{\text{TR},\text{LONG},\text{COMP}}$. Usually, the composite longitudinal trench resistance (table 1) is dominated by the overlying connecting metal strip, if present (sec. 2.2). In the dashed green curve in fig. 78, the $R_{\text{tr},\text{long},\text{int.}}$ was strongly reduced, such that the $R_{\text{tr},\text{long},\text{comp.}}$ decreases at least by a factor of 200. For the sample with die-backside grounding, a *lower* composite longitudinal trench resistance is predicted to significantly *increase* the RF-emission from 3 MHz to 1 GHz: For example, at 130 MHz the predicted increase was 5.4 dB, whereas at 10 MHz and at 800 MHz the increase was only 3.9 dB and 4.9 dB, respectively. This may be counterintuitive because one may erroneously associate a decreased composite longitudinal trench resistance with a better overall grounding – reasons for this effect will be addressed in sec. 6.5.4. Note that this also implies that a precise modeling of the deep trenches is of certain importance. However, the modeling of the deep trenches is complicated by the fact that there is a strong motivation to remove a large number of deep trenches from the model, for reasons of simulation efficiency (sec. 6.3.1 and sec. 5.2.2).

Relevance of ρ_{sub} The dashed blue curve in fig. 78 shows the impact of a ten-fold more conductive wafer-substrate. In the case of die-backside grounding, a reduction of the RF-emissions of 9 dB were predicted 10 MHz as well as at 600 MHz. This clearly shows that, even at low frequencies, the wafer-substrate may not be approximated as a perfect conductor. Because one usually regards the conductivity $\sigma_{\text{SUB}} := 1/\rho_{\text{SUB}}$ as a parasitic parameter that should ideally be zero, it is counterintuitive that an *increase* in σ_{SUB} leads to *lower* RF-reductions. In fact, the impact of ρ_{SUB} is *reversed* in case of a non-connected die-backside as well as at some frequencies, e.g. 5.4 dB at 350 MHz. This will be analyzed in more detail in sec. 6.6.2.

Substrate Parasitics with low Relevance for the DC/DC RF-emissions

Many other substrate parasitics have a rather small or entirely negligible impact on the simulation result: For example, a strong reduction of the vertical trench resistance $R_{\text{trench},z}$ did not affect the predicted RF-emissions. Moreover, idealizing n-sinkers and n-contacts ($R_{\text{ncont}} = R_{\text{nsink}} = 0$), and neglecting the sheet resistivities of the n-buried layer ($R_{\text{nepi}} = 0$), resulted in deviations by

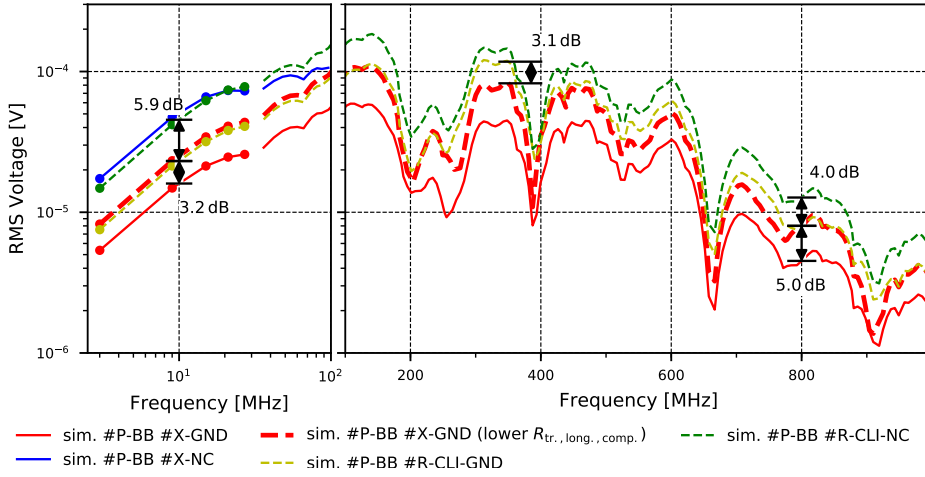


Figure 79: The dashed green and yellow curves demonstrate the low-dimensional substrate models. This graph shows various simulated RF-emissions at transceiver #0 (OFF), caused by the operation of the DC/DC converter in the packaging-variant #P1.

less than 3 dB. This confirms that the n-buried layer can be approximated as equipotential (see sec. 5.1).

Accuracy of the Low-Dimensional Substrate Model based on the CLI-boundary condition Fig. 79 evaluates the low-dimensional substrate models #R-CLI-*, which use CLI-boundary conditions at the wafer-substrate surface below the n-epitaxial layer (sec. 5.1.2). The low-dimensional substrate model #R-CLI-GND (dashed yellow curve) predicts higher RF-emissions than the substrate extraction model (solid red curve) by typically +3 dB to +6 dB, which is an additional error. A similar offset was previously observed in the case where $R_{tr, long, comp.}$ is neglected. The presence of this offset in the used low-dimensional substrate models is not surprising since they also neglect the composite longitudinal trench resistance (sec. 6.3.1). In fact, setting $R_{tr, long, comp.} = 0$ leads to a prediction (dashed red curve in fig. 79) that is well aligned with the dashed yellow curve.³⁸ This confirms that the CLI boundary condition is indeed very applicable, but #R-CLI-* remain to have another deficiency, which is the use of PCV boundary conditions at the deep trenches.

³⁸ An exception is found near 350 MHz, where the dashed red curve deviates from the dashed yellow curve by 3.1 dB.

6.5.4 The Interplay of the $R_{tr,long,comp.}$ and Die-Backside Grounding: Discussion using a Simplistic Circuit Model

At 10 MHz, the neglect of $R_{tr,long,comp.}$ causes an offset of 3.2 dB in the case of die-backside grounding (solid red and dashed yellow curves in fig. 79). Conversely, with a non-connected die-backside, the offset is almost negligible (solid blue and dashed green curves). Therefore, at 10 MHz, the benefit of die-backside grounding is underestimated if the $R_{tr,long,comp.}$ is neglected (5.9 dB in fig. 79 and 11 dB in fig. 77). In contrast, at 800 MHz, #R-CLI-GND and #R-CLI-NC are both shifted by roughly the same offset. Thus here, the benefit of die-backside grounding is correctly predicted, despite the $R_{tr,long,comp.}$ is neglected (4.0 dB in fig. 79 versus 5.5 dB in fig. 77).

In the following, it is explained how neglecting $R_{tr,long,comp.}$ can result in these offsets of 3.2 dB and 5.0 dB, and why, at low frequencies, this offset depends on the presence of die-backside grounding. Fig. 80 (a) shows a highly simplistic circuit that is used to estimate the impact of $R_{tr,long,comp.}$ on the parasitic connection between the DC/DC's high-side switch and the seal ring. The mean voltage of the wafer-substrate surface below the DC/DC's high side switch is represented by the node CS-EPI-HS. $R_{seal,HS}$ is the resistance between CS-EPI-HS and the deep trenches computed under the approximation $R_{tr,long,comp.} = 0$, and $R_{HS,0}$ is the resistance to the die-backside. The quantities $R_{seal,HS}$ and $R_{HS,0}$ will be further described in sec. 6.7 (see also table I3 in sec. 6.7). As shown in fig. 80 (a), the resistor $R_{seal,HS}$ is subdivided into four

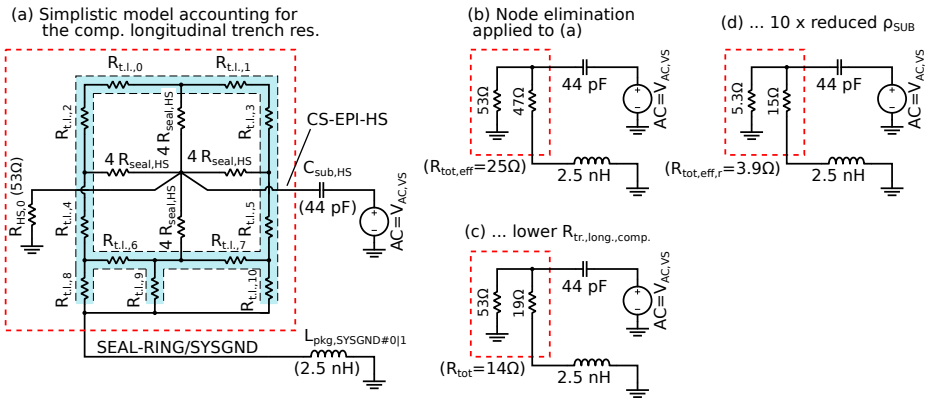


Figure 80: Simplistic approach to understand the impact of the composite longitudinal trench resistance on the RF-emissions qualitatively. The cyan regions in (a) symbolize the trenches and their re-enforcing metal-strips. Part (b) shows the result of node elimination applied to the dashed red box in (a). Part (c) and (d): The nodes were eliminated as in (a), but in case (c), all resistors $R_{t,l,0}$, $R_{t,l,1}$, ..., $R_{t,l,10}$ were neglected, whereas in case (d), $R_{seal,HS}$ and $R_{HS,0}$ were reduced by a factor of 10.

partial resistors, and the additional resistors $R_{t,l,0}$, $R_{t,l,1}$, ..., $R_{t,l,10}$ heuristically account for the composite longitudinal trench resistance. By eliminating all circuit nodes in the dashed red box in fig. 80 (a), the equivalent circuit in fig. 80 (b) is obtained: The resulting resistor $R_{\text{seal,HS,eff}} = 47 \Omega$ represents the *effective resistance* between CS-EPI-HS and SEAL-RING, in which $R_{\text{tr,long,comp}}$ is included. This resistance is roughly 2.5-fold larger than $R_{\text{seal,HS}} = 19 \Omega$, as shown in fig. 80 (c), which corresponds to $R_{\text{tr,long,comp}} = 0$.

$C_{\text{sub,HS}}$ is the wafer-substrate capacitance of the DC/DC's high-side switch, and $V_{\text{AC,VS}}$ represents the voltage ripple of the inner VS node to the PCB ground³⁹. Now consider frequencies above the corner frequency $f_{\text{corner,HS}} = (2\pi R_{\text{tot,eff}} C_{\text{sub,HS}})^{-1} \approx 145 \text{ MHz}$, where $R_{\text{tot,eff}} = R_{\text{HS},0} \parallel (R_{\text{seal,HS,eff}} + 2\pi f L_{\text{pkg,SYSGND}\#0\parallel 1}) \approx R_{\text{HS},0} \parallel R_{\text{seal,HS,eff}}$ is the total impedance from CS-EPI-HS to the PCB-ground. In this frequency range, $C_{\text{sub,HS}} = 44 \text{ pF}$ can be mostly considered as shorted, and hence, the AC-voltage $V_{\text{AC,VS}}$ can be thought to be applied directly to CS-EPI-HS. Here, the AC-current over the inductance of the system ground pin $L_{\text{pkg,SYSGND}\#0\parallel 1} = 2.5 \text{ nH}$ is proportional to $R_{\text{seal,HS,eff}} = 47 \Omega$. Hence, neglecting $R_{\text{tr,long,comp}}$ increases the AC voltage ripple at SEAL-RING and SYSGND by $20 \log_{10}(R_{\text{seal,HS,eff}}/R_{\text{seal,HS}}) \approx 8 \text{ dB}$. As will become clear from the discussion in sec. 6.7, this offset will transfer one-to-one to the RF-emission curve. Conversely, at frequencies below the corner frequency of $f_{\text{corner,HS}} = 145 \text{ MHz}$, the current forced over $C_{\text{sub,HS}}$ roughly equals $i2\pi f C_{\text{sub,HS}} V_{\text{AC,VS}}$. Here, the dashed red box in fig. 80 (b) may be regarded as a current divider. Therefore, the difference of the seal-ring's AC voltage in (b) and (c) is $20 \log_{10}((R_{\text{tot,eff}} R_{\text{seal,HS}})/(R_{\text{tot}} R_{\text{seal,HS,eff}})) \approx 3 \text{ dB}$. These predictions are roughly in agreement with the previously-discussed simulation results (5.0 dB and 3.2 dB, respectively, from fig. 79). Nevertheless, the circuit model in fig. 80 (a) is clearly based on a very crude heuristic, and is not recommended for quantitative predictions: For example, the trench-oxide capacitances were not accounted for, the AC currents across which may be subject to similar current dividers.

These considerations justify the counterintuitive view that the subsystem formed from the deep trenches, the overlying metal strips and the seal ring *enhances* the transport of RF-emissions from the DC/DC-converter to the transceivers. Observe that for $f \gg f_{\text{corner,HS}}$, the offset in the AC voltage at SEAL-RING/SYSGND is independent on the presence of the backside resistor $R_{\text{HS},0} = 53 \Omega$. Conversely, for $f \ll f_{\text{corner,HS}}$, if $R_{\text{HS},0}$ is dropped, the complete AC current across $C_{\text{sub,HS}}$, which is independent of $R_{\text{seal,HS,eff}}$, flows

³⁹ As will be shown in sec. 6.7, at high frequencies, $V_{\text{AC,VS}}$ is the voltage drop caused by I_{VS} flowing over the VS-PGND pin-loop inductance. Note that by exchanging the quantities and labels one may also re-interpret fig. 80 (a) as a representation of the DC/DC's low-side switch at low frequencies.

into the seal ring. Thus, below $f_{\text{corner,HS}}$, for a non-connected die-backside, the RF-emissions are independent of $R_{\text{tr,long,comp.}}$, whereas for a grounded die-backside, neglecting $R_{\text{tr,long,comp.}}$ causes an offset. This explains why, if neglecting $R_{\text{tr,long,comp.}}$, the RF-emission reductions achieved by die-backside grounding are underestimated at low frequencies but not at high frequencies.

6.5.5 The Relevance of Magnetic Shielding by the PCB-Ground Plane and Comparison between Different Package Models

Fig. 81 evaluates the IC-package models #P-HYB, #P-EXT, #P-EXT-NOR and #P-EXT-NOP (table 10). As explained in sec. 6.5.1, the ON-state, in particular in transceiver #2 (fig. 81 (b)), is the most suitable benchmark for RF-propagation via the IC-package. Recall that the substrate does *not* have a large impact on transceiver #0 (ON) and transceiver #2 (ON) below 50 MHz and 200 MHz, respectively. Nevertheless, in addition, substrate knock-out was enabled in all curves in fig. 81, in order to rule out any influence of the substrate in the following discussion. The lumped-element model obtained from the HFSS-simulation dataset (#P-HYB, dashed green curve) is in excellent agreement with the black-box instantiation in AC-simulation (#P-BB, red curve). Furthermore, a package model based on parasitic extraction tools (#P-EXT, dashed blue curve) is of sufficient accuracy as well. The dashed cyan curve is based on a variant of #P-EXT, in which the ground plane was deleted (#P-EXT-

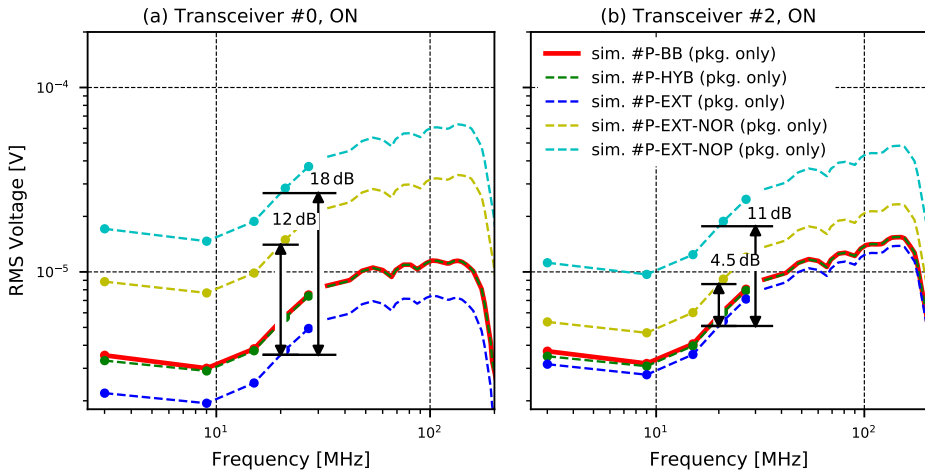


Figure 81: This graph shows the simulated RF-emissions at transceiver #0 (ON) and #2 (ON) below 200 MHz, caused by the operation of the DC/DC converter in the packaging-variant #P1. The dashed curves are simulation results for various alternative IC-package models – note that substrate knock-out was used in each case.

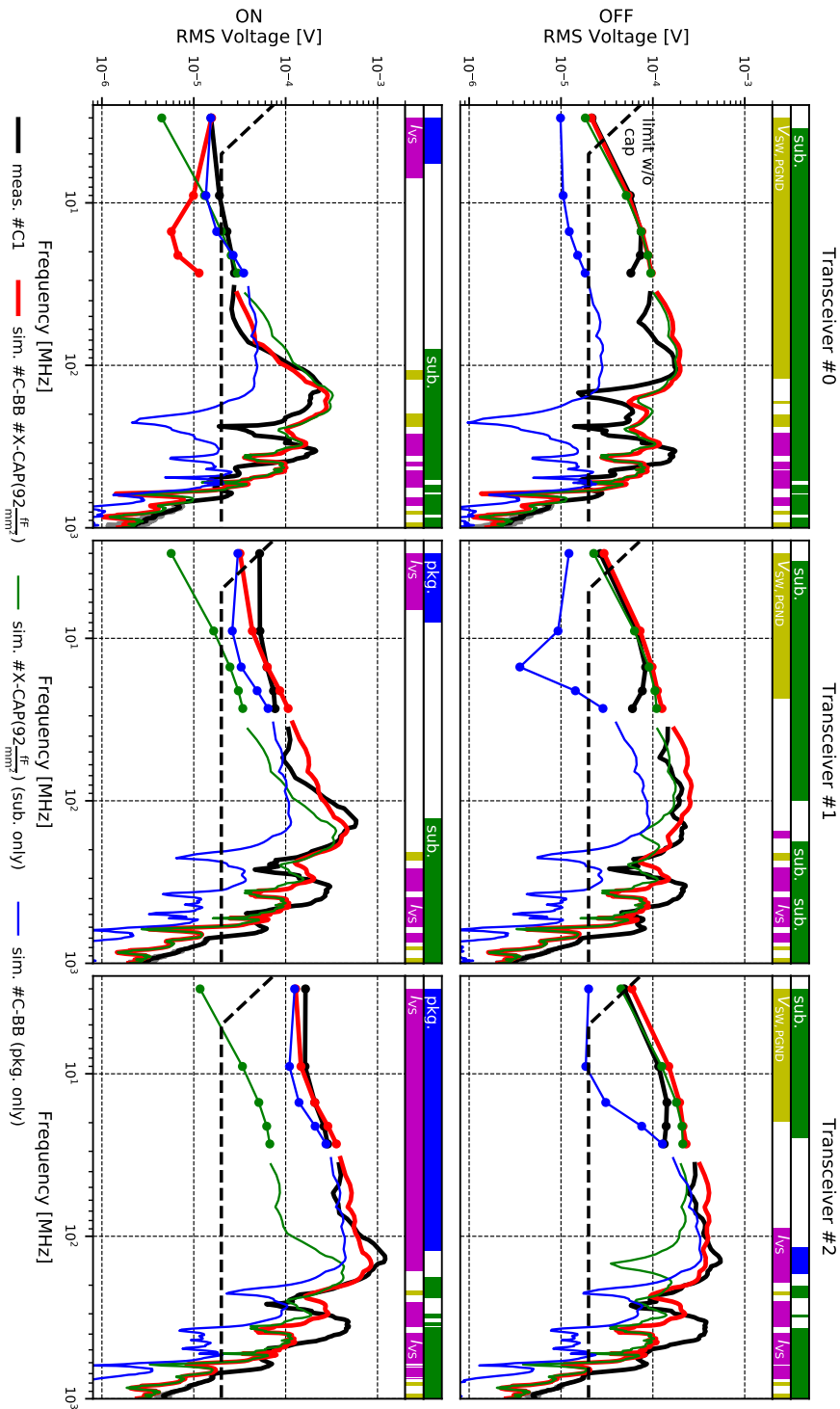


Figure 82: Counterpart to fig. 75 and fig. 76, in which instead the ceramic IC-package #C1 is investigated. It shows RF-emissions at the three different transceiver pins (columns) and in two different bus states (rows), caused by the operation of the DC/DC converter.

NOP in table 10). In transceiver #2, the deviation from #P-EXT is 11 dB, and in transceiver #0 it is even 18 dB. Presumably, the reason for the larger deviations in transceiver #0 is that magnetic shielding of the PCB-ground plane is more important at larger distances. In the dashed yellow curves, the eddy currents in the ground plane were included (#P-EXT-NOR in table 10). The deviation is less, i.e. 4.5 dB for transceiver #2 and 12 dB for transceiver #0. Nevertheless, the error introduced at transceiver #0 is considered very significant, and it clearly confirms that adding the ground plane as a floating conductor is not sufficient (sec. 3.3.1). Also note that the deviations at transceiver #0 obtained here (12 dB and 18 dB) are in excellent agreement with the prediction from sec. 3.3.4.

As demonstrated by fig. 82, the developed methodology can also successfully predict the RF-emissions in the ceramic IC-package. Moreover, the good alignment between measurement (black curve) and simulation (red curve) validates the construction that eliminates the floating-reference port (sec. 6.3.1, sec. 3.2.5). In comparison to the plastic IC-package (figs. 75 and 76), both, the substrate- and the package-emissions are increased. The increase of the substrate-emissions is due to the lack of die-backside grounding as well as presumably due to the increased inductance of the ground pins (sec. 6.6.3). Conversely, the package-emissions are increased because the larger pin-loops exhibit a larger mutual inductance.

6.5.6 Bonus Topic: The RF-Emissions Caused by the Digital Disturbance Source

Fig. 83 shows the RF-emissions of the digital disturbance source in the sample #P1. This sample features a separate digital ground and the EPI-DIG potential is connected to an IC-pin (see sec. 6.2). For simplicity, in the following, only the RF-emissions at transceiver #0 in the OFF-state will be considered. Different from the above discussion of the DC/DC-converter, in the graphs in this section, both *even and odd* harmonics of the clock frequency of 32 MHz are shown (see sec. 6.4). The measurement data (black curve) and the simulation result using RLC(.5,.5) (solid red curve) are in excellent agreement below 250 MHz. Conversely, between 250 MHz and 1 GHz, deviations are typically 15 dB, e.g. at 510 MHz. This is due to the employed small-signal equivalent of the digital part RLC(.5,.5) being overly simplistic (see sec. 6.3.1), as will be shown in the following.

Substrate- vs. Package-Emissions Across the entire frequency range, in simulation, the digital RF-emissions are *never* dominated by package couplings. This is shown by comparing the solid red to the solid green curve in

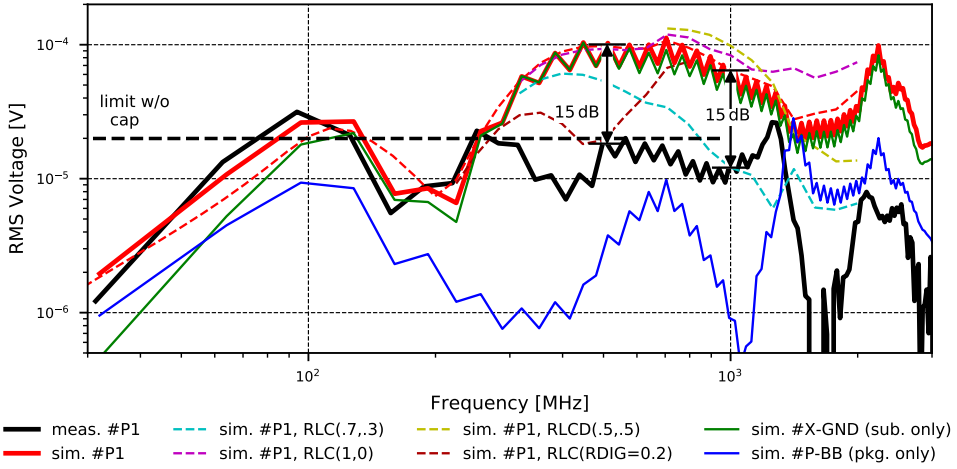


Figure 83: RF-emissions at transceiver #0 in the OFF-state, caused by the digital disturbance source. This data corresponds to the packaging variant #P1. In the dashed curves, the Dirac comb model was used for I_{DDIS} . All simulations use the substrate model #X-GND and the package model #P-BB. Unless labeled differently, the digital part is described by the small-signal equivalent RLC(.5, .5).

fig. 83.⁴⁰ With few exceptions, this applies to all transceivers in the ON- and in the OFF-state (not shown here for clarity), as well as in the samples with modified ground or n-buried layer connection (#P1-DNE and #P1-DNEG). In all samples considered here (#P1, #P1-DNE and #P1-DNEG), the digital RF-emissions are primarily transmitted via wafer-substrate parasitics. On the example of the sample #P1, this is shown by the comparing the solid red and solid blue curves in fig. 83. Different from the DC/DC-converter, pronounced minima do not occur in the disturber spectrum I_{DDIS} (sec. 6.5.1). Moreover, destructive interferences do not occur in the simulation of the digital emissions because there is only a single AC-source, and the package-couplings are mostly negligible. Hence, all pronounced extrema in the measured and simulated spectrum are instead associated with extrema in the transfer function.

Root cause analysis of the deviations above 250 MHz Note that the spectrum of I_{DDIS} obtained from transient simulation is well approximated by an ideal Dirac comb up to 1.5 GHz (see sec. 6.3.2). This allows to interpret the transfer function $I_{DDIS} \rightarrow V_{meas,*}$, scaled by $Q_{DDIS, rise-pulse} / T_{DDIS}$ (see eq. (100)), as an estimate of the RF-emission characteristic. This approach is used to construct the *dashed* curves in fig. 83: For example, observe the

⁴⁰ This is true despite transceiver #0, among all transceivers, has the *least* distance from the pins of the digital supply and ground.

good alignment between the solid and the dashed red curve. Thereby, the simulation result can be presented with an increased frequency resolution and devoid from the ripple between even and odd harmonics. The pronounced minimum in the measurement data near 400 MHz is missing in the simulation result with $\text{RLC}(1, 0)$ (dashed magenta curve). However, if the ESR is reduced from $1.11\ \Omega$ to $0.2\ \Omega$ (dashed brown curve), a pronounced minimum arises at the digital part's self-resonance frequency of 460 MHz (sec. 6.3.1). Thereby, the agreement with measurement is much increased. This is interpreted as follows: Above the resonance formed from CDIG and the IC-package inductance near 100 MHz, the disturbance current I_{DDIS} is mostly returned internally across CDIG, LDIG and RDIG (see fig. 67). This results in a supply drop at DVCC and a ground bounce at DGND and at PW-DIG. At the self-resonance frequency of 460 MHz, for sufficiently small RDIG, the series connection of CDIG, LDIG and RDIG has a comparatively small impedance, whereby the ground bounce at PW-DIG is reduced. Sec. 6.3.1 has suggested an explanation why RDIG might have been overestimated in the used model.

However, $\text{RLC}(\text{RDIG}=0.2)$ in fig. 83 does *not* resolve the deviation between measurement and simulation at yet higher frequencies, e.g. 15 dB at 1 GHz. In the following, $\text{RLC}(.7, .3)$ (dashed cyan curve), $\text{RLC}(1, 0)$ (dashed magenta curve) are compared to $\text{RLC}(.5, .5)$ (dashed red curve): It is clear that these curves are very similar below the self-resonance frequency of 460 MHz, where the impedance of the digital part is dominated by CDIG. At 1 GHz, $\text{RLC}(.7, .3)$ is in much better agreement with the measurement results than $\text{RLC}(.5, .5)$. This leads to the rather intuitive conclusion that already at twice the corner frequency of CDIG, LDIG and RDIG, these lumped elements must be fractured into an array of interconnected capacitances (sec. 6.3.1). Nevertheless, it can be argued that the small-signal equivalent $\text{RLC}(.5, .5)$ at least yields an *upper bound* of the RF-emission characteristic. This is supported by the measurement results shown in fig. 83.

In the dashed yellow curve in fig. 83, the capacitance of the digital disturbance source was included. The large deviation between the dashed yellow, magenta, red and cyan curves near 2 GHz again highlights the high importance of accounting for the distribution of the digital part's capacitance, inductance and resistance in this frequency range.

Altered Bonding Diagrams and Modified Grounding The solid and the dashed red curves in fig. 84 show the digital RF-emissions in the sample #P1, which features a separate digital ground, and which were discussed in detail above. The yellow curves correspond to the same sample (#P1), but the n-buried layer underneath of the digital core was biased to 4.5 V. The impact

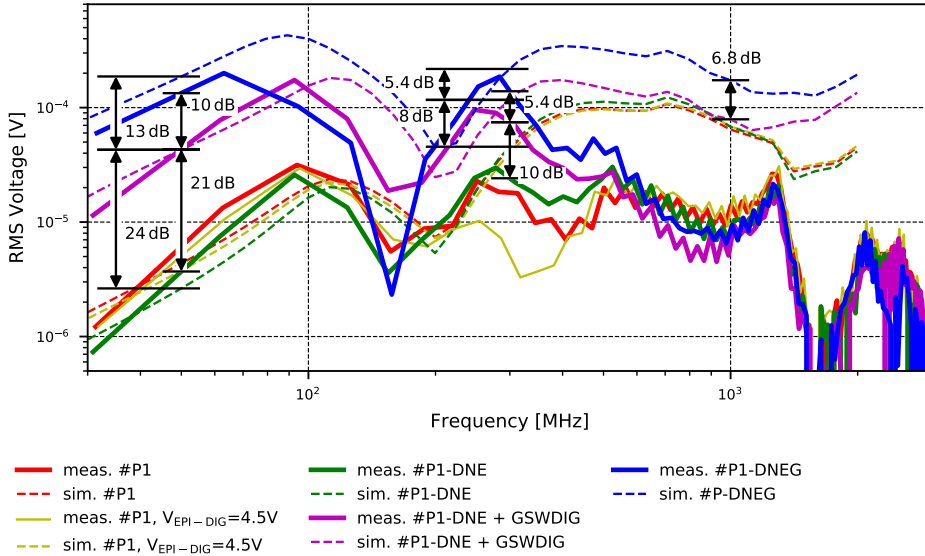


Figure 84: Digital RF-emissions at transceiver #0 in the OFF-state, in variants of the bonding diagram and with modified grounding, as well as for a non-zero bias voltage at EPI-DIG. In the simulation results depicted here (dashed curves), the Dirac comb model was used for I_{DDIS} . They use the substrate model #X-GND and the package model #P-BB, and digital part is described by the small-signal equivalent RLC(.5, .5).

on the RF-emissions is negligible, both in simulation and measurement ⁴¹. This may appear counter-intuitive because this change in the voltage of EPI-DIG reduces the capacitance between the digital part's n-epitaxial pocket and the wafer-substrate by roughly a factor of 1.6. However, in fact, this capacitance $C_{sub,DIG}$ is quite large, and behaves rather as an AC-short over most of the considered frequency range: Already at 100 MHz, its impedance is only 17.4Ω (table 14), whereas the wafer-substrate resistance to the deep trenches $R_{seal,DIG}$, which is in series to it, equals 33Ω (table 13). In the solid and dashed green curves in fig. 84, the bond wire that connects EPI-DIG was removed, and EPI-DIG was instead internally connected to DGND (see table 9, sample #P1-DNE). Above 100 MHz, the deviation from the red curves is mostly negligible. This shows that AC-grounding the n-buried layer below the digital core via a separate pin does *cannot* shield the RF-emissions in the relevant frequency range. This can be explained by comparing the connecting resistance of the n-buried layer ($RDNEPI$ from table 18) to the capacitive impedance between the n-buried layer and the logic implant ($CDLOG$ from

⁴¹ In measurement, there is an exception in the frequency range 250 MHz – 400 MHz.

table 18): Namely, for frequencies significantly above the corner frequency of 83 MHz, the logic-implant is roughly AC-shortened to the n-buried layer.

In contrast, a quite successful counter-measure is the separation of the digital ground from the system ground: The magenta curves in fig. 84 also correspond to the sample #PI-DNE, but here, these two grounds were connected on the die via the connection GSWDIG (see fig. 67). In measurement, at 50 MHz, the ground separation reduces the RF-emissions by 21 dB, and at 300 MHz, still 10 dB can be gained. This is found by comparing the solid magenta and the solid green curve. In simulation, the reductions are 24 dB and 8 dB at 50 MHz and 300 MHz, respectively. Albeit, on an absolute scale, the simulations are not very accurate above 250 MHz, they can nevertheless *precisely* predict the benefit of separating the digital from the system ground up to 1 GHz. An explanation why the RF-emissions are reduced if the two grounds are separated is provided in the following: As explained above, the n-buried layer underneath the digital core is rather AC-shortened to DGND than to EPI-DIG, and moreover, the p-n-junction to the wafer-substrate can be considered an AC-short. Thus, the RF-isolation between DGND and SYSGND is merely due to wafer-substrate resistances like $R_{\text{seal,DIG}} = 33 \Omega$ (table I3). Nevertheless, this RF-isolation is quite efficient because these resistances are much larger than the impedances that connect the system ground to the PCB-ground, e.g. 3Ω at 100 MHz (see $L_{\text{pkg,SYSGND\#0}}$ from table I6). Of course, this consideration is very simplistic because, on the one hand, there are other wafer-substrate resistances involved in the coupling between DGND and SYSGND as well, and, on the other hand, SYSGND is also AC-grounded via other paths. For example, alteration analysis (see also sec. 6.7) has shown that, near 800 MHz, also the coupling of SYSGND to the n-epitaxial pocket of the DC/DC's high-side switch lowers the impedance of SYSGND – a detailed discussion of this is beyond the scope of this work.

In the sample #PI-DNEG (blue curves), not only are SYSGND and DGND connected on the die, but, in addition, the digital ground pin is removed. Thus, the difference between the blue and magenta curves in fig. 84 shows the benefit of adding another ground pin to SYSGND that has a small mutual inductance to the original SYSGND-pins. Because of this alone, 10 dB are gained at 50 MHz in measurement (13 dB in simulation) and 5.4 dB at 300 MHz in measurement (5.4 dB in simulation).⁴² Therefore, firstly, introducing a new ground pin for the digital core and, secondly, separating it from SYSGND, yields a total of 31 dB at 50 MHz and 15 dB at 300 MHz in measurement.

⁴² Note that at 1 GHz, the difference between the blue and magenta curves is negligible in measurement (solid curves) but amounts to 6.8 dB in simulation. The reason for this prediction error is currently not understood.

6.6 Counter-Measures in Measurement and Simulation

6.6.1 Package-Coupled RF-Emissions

A common heuristical counter-measure against RF-emissions in transceivers is to increase their distance to the source of the disturbance. Fig. 85 (a) shows that this rather effectively diminishes the cross-coupling of noise via the IC-package: At 100 MHz, the package-emissions of transceiver #1 are reduced by 14 dB in comparison to transceiver #2, and roughly doubling the distance (transceiver #0) further reduces them by 8 dB. However, as shown in fig. 85 (b), the substrate-emissions are more weakly distance-dependent: With an edge-to-edge distance of only 50 μm , transceiver #0 is almost as close to the DC/DC-converter as possible, whereas transceiver #1 has an edge-to-edge distance of almost 0.8 mm from the DC/DC-converter. In spite of this, between 50 MHz and 100 MHz, the region in which the global maximum is found, the substrate-emissions at transceiver #1 are only 3–6 dB lower than at transceiver #2. Moreover, roughly doubling the distance (transceiver #0 vs. #1) provides almost no additional benefit regarding the substrate-emissions. Therefore, before a costly rearrangement of the IC's floor-plan is considered, the designers should at least determine whether the RF-emissions are predominantly substrate- or package-dominated. Also note that substrate-emissions beyond 200 MHz and package-emissions beyond 400 MHz are not significantly reduced by an

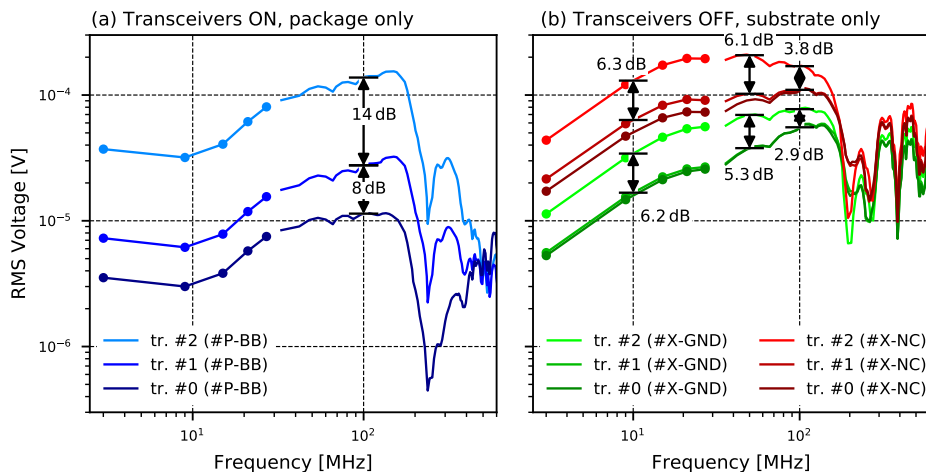


Figure 85: Reduction of the DC/DC's RF-emissions by means of increasing the distance of the transceiver (simulation only): (a) Substrate knock-out simulation using the #P-BB package model in the ON-state. (b) Package knock-out simulation using the #X-GND or #X-NC substrate model in the OFF-state.

increase in distance. The root cause of the weak distance-dependence of the substrate-emissions is elaborated in sec. 6.7.

Reducing inductive cross-coupling of noise via the IC-package can be achieved by rather intuitive means, provided that the receiving pin-loop, e.g. the pin-loop spanning the transceiver's ground-/supply and its output, has been identified: The receiving pin-loop and the pin-loop that carries the disturbance current are subject to optimization: IC-designers should minimize their area and increase their distance. For example, one should consider to add a dedicated ground- or supply-pin for each transceiver, in case of a pull-down or a pull-up bus, respectively. The bond wires and lead-frame parts of these two pins should be as close as possible. Moreover, the use of a more flat or smaller lead-frame can reduce the mutual inductance between these two pin-loops. Predictions of the expected benefit is possible with a modest computational effort (sec. 3.3 and eq. (104) from sec. 6.7).

6.6.2 Substrate-Coupled RF-Emissions: Technology, Layout and Packaging

In the following, it is attempted to reduce the substrate-transmitted RF-emissions by modifying technology parameters, the IC-layout or the IC-package.

Counter-measures targeting $R_{\text{TR, LONG, COMP}}$. As observed in sec. 6.5.3, an improved trench connection *unconditionally increases* the RF-emissions observed from 3 MHz to 1 GHz. This applies to ICs with a grounded die-backside (i.e. dashed yellow curve in fig. 79), as well as to the non-connected die-backside (dashed green curve). Therefore, in simulation, the replacement of the filling material inside the deep trenches (sec. 2.2) by an insulator was evaluated. This is depicted by the dashed green RF-emission characteristic in fig. 86 (a). This modification is only valid for the properly grounded die-backside (fig. 86 (a)) because otherwise the wafer-substrate would be rendered floating. These simulations have demonstrated that the use of isolating deep-trenches is a viable counter-measure from at least 3 MHz to 1 GHz: Specifically, the achieved reduction amounts to 13 dB at 100 MHz and still 10 dB at 450 MHz and 9 dB at 800 MHz.⁴³ The use of isolating deep-trenches is thought to improve the RF-emissions by eliminating the detrimental subsystem formed from the seal-ring, the deep trench and their metallization (sec. 6.5.4). Another counter-measure that targets the same RF-mediator is to

⁴³ At 3 MHz, the RF-emissions are reduced by more than 20 dB. However, this is of little relevance because here, the EMI limit values less strict and the RF-emissions are already rather low.

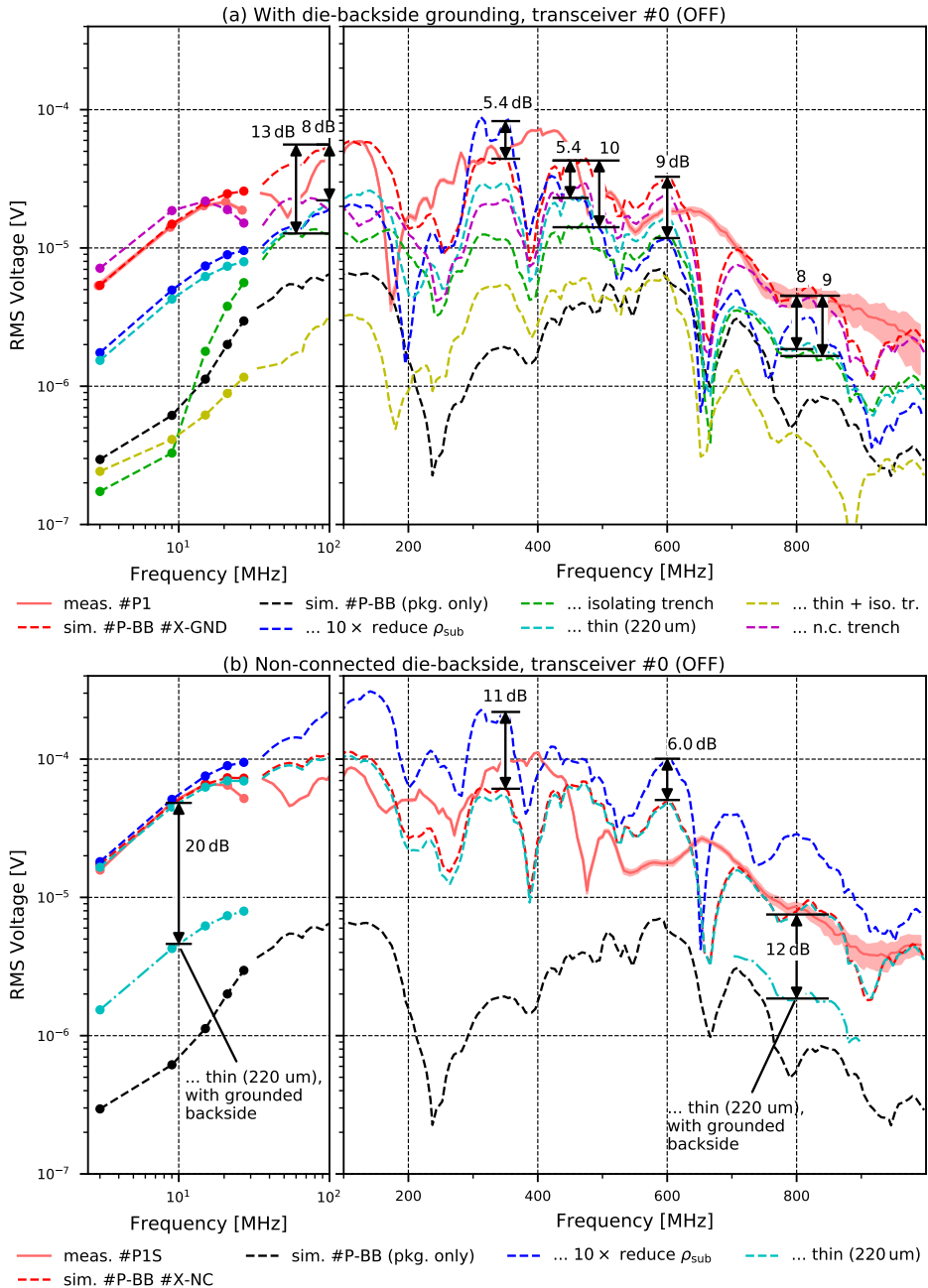


Figure 86: In the dashed blue, green, magenta and yellow curves, which are variants of the dashed red curve (sim. #P-BB #X-GND/#X-NC), a single technology- or IC-layout parameter has been altered in simulation. This graph shows various predicted/measured RF-emissions at transceiver #0 (OFF), caused by the operation of the DC/DC converter in the packaging-variant (a) #P1 and (b) #P1S.

merely eliminate all trench contacts to the above-lying metal-strips and to the seal-ring (dashed magenta curve, fig. 86 (a)). Also in this case, the die-backside must be galvanically connected to ground. This counter-measure, which essentially reduces the composite to the intrinsic longitudinal trench resistance, is more easily implemented because it does not require a modification of the BCD-technology. However, it is not as effective as the isolating deep-trenches, and outside the frequency range from 30 MHz to 350 MHz it was completely ineffective. Apparently, the intrinsic longitudinal trench resistance $R_{tr,long,int.}$ is still too low for this modification to attain its maximum benefit.

Die-Backside Grounding and Die Thickness Reduction Moreover, the effect of reducing the die-thickness under die-backside-grounding (dashed cyan curve in fig. 86 (a)) was predicted in simulation: Over the entire frequency range, this resulted in a significant reduction of the RF-emissions. At 100 MHz, the RF-emissions were reduced by 8 dB, while between 350 MHz and 1 GHz the reduction was still between 5–8 dB. Interestingly, in the case of a non-connected die-backside (dashed cyan curve in fig. 86 (b)), the benefit of a die-thickness reduction was virtually zero. In fig. 86 (b), it is observed that die-backside grounding is especially effective for thin dies: Here, a reduction of 20 dB is predicted at 10 MHz, and at 800 MHz the predicted reduction is still 12 dB. The combination of die-backside-grounding [50], reduced die-thickness and isolating deep-trenches is shown by the dashed yellow curve in fig. 86 (a): These counter-measures enhance each other, and on a major part of the frequency axis, the RF-emissions even dropped down to the package-emission noise floor (dashed black curve) ⁴⁴.

Exploiting ρ_{sub} : In the dashed blue curve in fig. 86 (a) and (b), the *conductivity* of the wafer-substrate was *increased* by a factor of 10. This might be implemented by using more strongly doped raw wafers. Note that, if the acceptor concentration is homogeneously increased, the capacitance C_{sub} (sec. 2.2) would change [12] ⁴⁵. This secondary effect, which may also affect the RF-emissions, was not accounted for in the simulations discussed here. Moreover, a strong reduction of ρ_{sub} might even affect the spectra of I_{VS} and $V_{SW,PGND}$ at high frequencies, which was also neglected.

If the die-backside was non-connected, decreasing ρ_{sub} ten-fold consistently increased the RF-emissions, e.g. by 11 dB at 350 MHz and by 6.0 dB at

⁴⁴ Near 100 MHz, 700 MHz and 900 MHz, the dashed yellow curve is even below the package-emission noise floor. This is presumably due to an incidental destructive interference between package and substrate.

⁴⁵ On the other hand, if a (p+)-substrate with a (p-)-epitaxial on top is used as a raw wafer, the capacitance to the n-buried layer would be unchanged.

600 MHz. Hence here, the wafer-substrate *resistivity* should be *maximized* in case of a non-connected die-backside. Quite the contrary, under die-backside-grounding fig. 86 (a), a *lowering* of ρ_{sub} often leads to a *reduction* of the RF-emissions. (This property was previously observed in sec. 6.5.3.) However, this does not apply to the entire frequency range – between 250 MHz and 450 MHz, the effect is small or even reversed. For example, at 350 MHz, a ten-fold reduction of ρ_{sub} instead *increased* the RF-emissions by 5.4 dB. The following explanation for this counterintuitive reduction of the RF-emissions under increased wafer-substrate conductivity is suggested: Under a ten-fold reduction of ρ_{SUB} , the backside-resistances are reduced by a factor of 10, whereas the effective resistance to the seal ring is not reduced as strongly, as shown in fig. 80 (c). This is due to the composite longitudinal trench resistance. Hence, for $f \ll f_{\text{corner,HS}}$, the fraction of the capacitively-injected substrate current that enters the seal-ring and the system-ground is reduced.⁴⁶ Beyond that, a reduction of ρ_{SUB} might also tilt other current dividers towards the die-backside, e.g., the current divider between, firstly, $R_{\text{HS},0}$ and, secondly, $R_{\text{INTER,HS}}$ in series with $C_{\text{sub,INTER}}$ and $L_{\text{pkg,SYSGND}\#*}$ (see fig. 91).⁴⁷ Moreover, another beneficial feature is the voltage divider between the seal-ring and the die-backside at the transceivers (e.g. $R_{\text{seal,t}\#0}$ and $R_{\text{t}\#0,0}$ in fig. 90), the impact of which is increased if ρ_{SUB} is reduced. On the other hand, reducing ρ_{SUB} may also increase the parasitic current flowing into the wafer-substrate, which motivates why, also under die-backside grounding, reducing ρ_{SUB} is not unanimously beneficial.

Conclusion Based on these results, regarding the RF-emissions, sole die-backside grounding is superior to trench-based substrate grounding, which might be leveraged in future technology developments. Of course, even more effective would be an SOI-technology. If isolating deep-trenches cannot be realized, one can still remove the metallization that connects the deep trenches in parts of the layout, as long as this does not render the wafer-substrate floating. Moreover, it is beneficial to reduce the die-thickness if the die-backside is grounded. It was observed that if one would be able to vary the wafer-substrate resistivity ρ_{SUB} , then additional RF-reduction might be achieved by optimizing ρ_{SUB} separately for each design. Beware that with a strongly altered ρ_{sub} , the skin-effect in the wafer-substrate or its dielectric constant might become relevant (sec. 5.2.1). Moreover, as discussed above, C_{sub} might change, and the $V_{\text{SW,PGND}}$ - and I_{VS} -spectra might become substrate-dependent.

⁴⁶ Note that, for reduced ρ_{SUB} , the corner frequency $f_{\text{corner,HS}}$, below which $R_{\text{seal,HS,eff,r}} = 15 \Omega$ and $R_{\text{HS},0,r} = 5.3 \Omega$ may be considered as a current divider, increases to almost 1 GHz.

⁴⁷ Note that in this current divider even the resistance of the n-sinkers may play a role. Thus, the relevance of R_{nsink} is conjectured to increase if ρ_{SUB} is strongly reduced.

6.6.3 Substrate-Coupled RF-Emissions: Circuit and Grounding

In the following, it is discussed how the circuitry and the ground-pinning can be optimized for low RF-emissions. In sec. 6.5.3 it was remarked that removing the C_{sub} and C_{trench} parasitics almost entirely eliminates the RF-emissions. Thus, circuit design should aim to disconnect noisy and sensitive nodes from the n-buried layer, if possible. In addition, the circumference of such pockets as well as the number of subdividing trenches should be reduced. For example, sec. 6.7 will predict that the IC's RF-emissions might be reduced by up to 5.5 dB at 300 MHz, by connecting the n-buried layer in some LV-pockets to SYSGND instead of VTR and VS.

The use of an “Isolated” low-side MOSFET Another example concerns the DC/DC's low-side switch ML (fig. 67), the n-buried layer of which is connected to the disturbed SW-node: Instead, one might use an isolated N-LDMOS (sec. 2.2), in which the n-buried layer can be connected to any node with a voltage greater than SW. If no new pins shall be introduced, the only choice is the internal battery voltage VS. The dashed magenta curves in fig. 87 (a) and (b) represent a simulation in which EPI-LS' in fig. 69 is disconnected from EPI-LS and reconnected to VS. This approximates the use of an isolated N-LDMOS for ML – however, the additional capacitance that would be introduced between VS and SW is neglected⁴⁸. Fig. 87 predicts that the reduction would be greater than 20 dB at 10 MHz. However, these gains rapidly diminish at higher frequencies – e.g., already at 100 MHz the reduction is less than 6 dB, and the peak RF-emissions at about 130 MHz are *not* significantly improved. This conclusion holds for a grounded die-backside (fig. 87 (a)) as well as for a non-connected die-backside (fig. 87 (b)). This discussion exemplifies the limitations of counter-measures merely on the circuit-design level: Due to the nonavailability of a sufficiently low-noise or low-impedance power-/ground-nodes, decoupling and shielding mechanisms that trivially work at sufficiently low frequencies often fail to make an improvement to the actual peak RF-emissions. A similar observation previously made in sec. 6.5.6 was that adding a dedicated pin for EPI-DIG is *ineffective* regarding the digital RF-emissions.

Separated Grounding of Deep-Trenches In the dashed yellow curves in fig. 87 (a) and (b), the deep trenches of each transceiver and of the DC/DC-converter were disconnected from the seal-ring in simulation. This is only

⁴⁸ Furthermore, given a sufficiently large isolated N-LDMOS and for sufficiently high frequencies, the AC voltage at its n-sinker terminal might differ from the AC voltage at the n-buried layer. This would require to alter the schematic in fig. 67 and even the device model might have to be improved, as was previously pointed out in sec. 6.3.1.

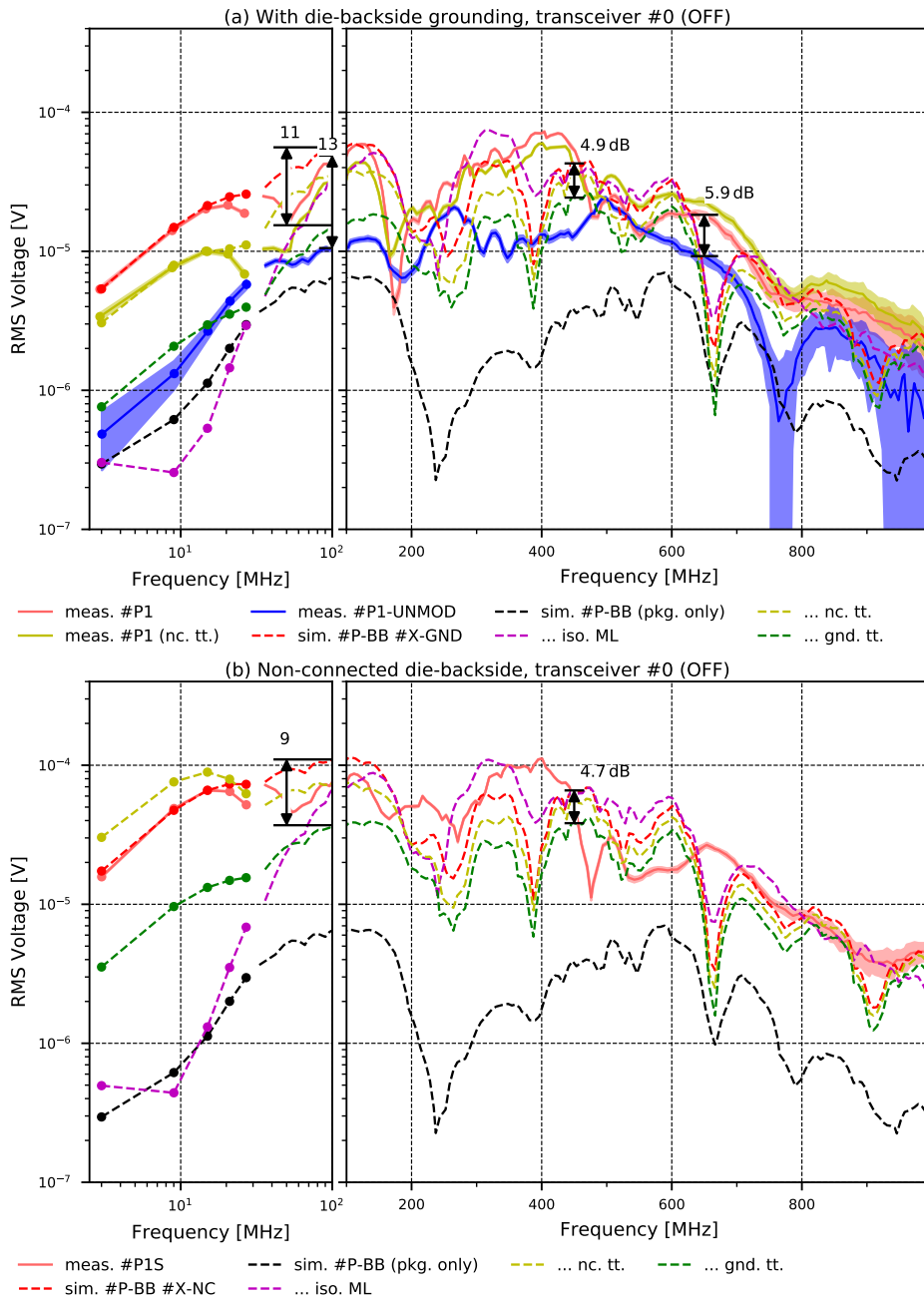


Figure 87: In the dashed magenta, dashed yellow and dashed green curves, which are variants of the dashed red curve (sim. #P-BB #X-GND/#X-NC), the circuit topology or the grounding via IC-pins has been altered in simulation. This graph shows various predicted/measured RF-emissions at transceiver #0 (OFF), caused by the operation of the DC/DC converter in the packaging-variant (a) #P1 and (b) #P1S.

possible because a gap of 25–50 μm is present between these modules and the seal-ring⁴⁹. Above 30 MHz, the reductions of the RF-emissions are rather insignificant and typically don't exceed 3 dB. The described modification was also realized in an experiment, the result of which is represented by the solid yellow curve in fig. 87 (a). This experiment confirmed that the benefit is only marginal above 30 MHz. However, if the trenches of the three modules are connected to additional ground pins, the RF-emissions might be reduced more strongly: A simulation has been conducted, in which two additional ground pins with a parasitic inductance of 5 nH were introduced⁵⁰. The first ground pin is connected to the trenches of the three transceivers, whereas the second ground pin is connected to the trenches of the DC/DC-converter. This is depicted by the dashed green curves in fig. 87 (a). The reduction is about 11 dB at 100 MHz, but the effectiveness is diminished to 4.9 dB at 450 MHz. It is not clear whether this effect should be understood as a local shielding measure or rather as a general improvement of the seal-ring and wafer-substrate grounding.

Improved Grounding of the System Ground and Seal-Ring In practice, it is hardly possible to connect the deep trenches of a module to a less disturbed ground node. Not only does this contradict the aim to compactify the layout, as explained above, but also typically there is no silent ground node readily available (see sec. 2.1). Conversely, if there is a willingness to invest into additional ground bonds for EMI reduction, it should be suggested that they are rather placed onto the system ground and the seal-ring. This is demonstrated by the blue curve in fig. 87 (a), which represents a measurement of the sample #PI-UNMOD: Here, as described in sec. 6.2, eight additional ground pins were added to SYSGND, TGND, SEAL-RING and some modules' deep trenches. As shown in fig. 87 (a), this achieves a reduction of 13 dB at 100 MHz, and it still yields 5.9 dB at 650 MHz. From this data one cannot distinguish the relative importance of the eight additional ground pins – in practice, fewer but more well-placed ground bonds may yield a comparable benefit. For example note that sec. 6.5.6 demonstrated experimentally that also a single well-placed additional SYSGND-pin could reduce the digital RF-emissions by 5.4 dB at 300 MHz. In order to maximize the impact at a minimum number of additional pins, it is recommended to use an iterative approach and apply the developed physically-based methodology.

⁴⁹ As pointed out in sec. 6.3.1, such spacers are typically omitted in a productive design to reduce die area.

⁵⁰ The mutual inductances between the IC-pins and these additional pins were neglected.

Conclusion It may be beneficial to reconnect the n-buried layer in some LV-pockets to the system-ground rather than to a supply voltage. The use of an isolated low-side switch in the DC/DC is predicted to be *ineffective*. It is also *not* recommended to connect deep-trenches of different modules to different ground nodes. Instead, additional ground bounds should rather be placed directly onto the system-ground or the seal-ring. In particular, one should consider down-bonds to grounded exposed die-pad rather than additional ground-pins: This would further reduce the parasitic inductance while keeping the pin count at a minimum. Yet more radical measures to improve the grounding of the seal-ring might be flip-chip packaging or the use of through-silicon vias [134] that connect the system ground directly to the die-pad.

6.7 Analysis of the Dominant Coupling Mechanisms and Parameterization of the Transfer Functions

This section exemplifies a procedure that automatically extracts simple circuits from models containing a large number of parasitic elements. These simplified circuits approximate a transfer function only from one source $S \in \{V_{SW,PGND}, I_{VS}\}$ and are limited to a frequency range $[f_0, f_1]$ as well as to a transceiver index k and transceiver state X . The starting point of this procedure is the low-dimensional substrate resistor network #R-CLI-GND (see sec. 5.1.2) in combination with the lumped-elements-based IC-package model #P-HYB (see sec. 3.3.3). Depending on the transfer mechanism to be described, either the substrate- or the package-coupling knock-out (sec. 6.3.2) is applied to this model. In the following, this model will be termed the *initial model*. The *error metric* of a simplified circuit shall be the RMS-deviation of the simplified transfer function (S, X, k) from the initial model's transfer function (S, X, k) in a double-logarithmic representation on the interval $[f_0, f_1]$. The goal of the simplification procedure is to achieve maximum simplification while the error metric may not exceed, e.g., 3 dB.

Firstly, using alteration analysis (sec. 2.3.3), a large number of variations of the transfer-function (S, X, k) is computed: In each alteration iteration, exactly one parasitic element in the initial model is knocked out, i.e. parasitic resistors and capacitors and mutual inductances are deleted, whereas parasitic inductors are shorted out. The error metric is evaluated for each of the multiple hundreds of alteration variants, and the resulting quantities are interpreted as the *relevance* of the associated parasitic elements. Subsequently, the parasitic elements are sorted by this relevance rating in decreasing order.

A simplified circuit is obtained from the initial model by discarding all parasitic elements that have a relevance rating below a certain threshold. The threshold should be maximized under the constraint that the resulting simplified circuit's error metric is less than the upper bound described above.⁵¹ In practice, this can be achieved using a binary search that repeatedly invokes SPICE-simulations. Alternatively, one might consider the deleted parasitics' individual errors as uncorrelated random numbers with a fixed amplitude but a random phase, and sum up their variances. Afterwards, further simplifications to the circuit must be performed manually and driven by simulation feedback. This is due to the fact that, firstly, the so-obtained circuit often exhibits dangling parasitic elements or other topological features that can be trivially reduced further. Secondly, the PCB-model and the integrated circuit is not reduced by the automated procedure described above.

This very structured approach yields a simplified circuit with a meaningful circuit topology, and the contained circuit elements and nodes have a well-defined semantics: For example, each parasitic $L_{pkg,...}$ represents the *loop inductance of a pin, in which the current is returned via the exposed pad and the PCB ground plane* (sec. 3.2.2). Moreover, the circuit nodes labeled CS-* represent the *average surface potential of the wafer-substrate* (sec. 5.1.2). As opposed to heuristical circuit models that are based on prior experience or empirical parameter fitting, the presented circuits enable a physically-based discussion of the leading-order EMI coupling path.

The described automated circuit reduction applies to the following classes of circuit elements:

- Wafer-substrate resistors (denoted by $R_{...,...}$).
- Junction-capacitances between n-buried layer and wafer-substrate (denoted by $C_{sub,...}$) and trench-oxide capacitances (denoted by $C_{trench,...}$).
- Pin-inductances (denoted by $L_{pkg,...}$) as well as their coupling coefficients (denoted by $\kappa_{...,...}$).
- Pin-resistances and capacitances. None of them were found to be relevant in the three considered cases (figs. 88, 89 and 91).

The relevant subset of these parasitics are listed in tables 13, 14, 15, 16 and 17. Table 18 lists further parameters used in the following circuit diagrams.

⁵¹ Sensitivity analysis (sec. 2.3.3), might also be used to obtain a similar relevance rating. However, this "tangential sensitivity" does erroneously associate a low rating to small resistors that are almost shorts. This can provoke a rather small threshold and hence hampers the ability to simplify the circuit.

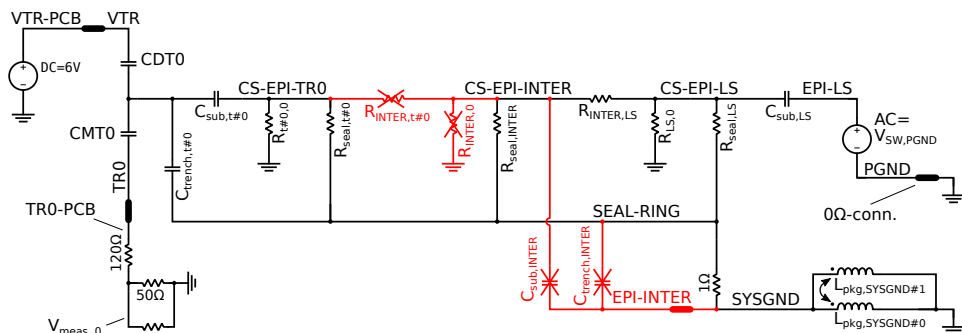


Figure 88: Simplified circuit that describes the transfer function from $V_{SW,PGND}$ to transceiver #0 in the OFF-state under package coupling knock-out. It is valid roughly up to 90 MHz. The elements crossed out in red exemplify parasitic elements that were deleted.

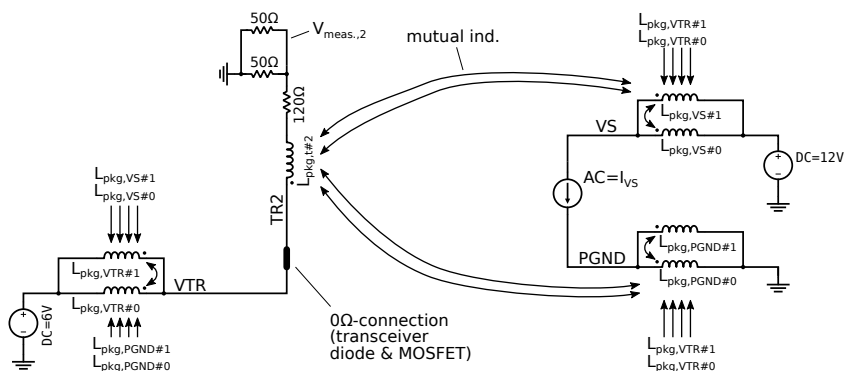


Figure 89: Simplified circuit that describes the transfer function from I_{VS} to transceiver #2 in the ON-state under substrate coupling knock-out. It is valid roughly up to 290 MHz.

Substrate-transfer of $V_{\text{SW,PGND}}$ below 90 MHz As observed in sec. 6.5.1, the RF-emissions at transceiver #0 in the OFF-state are $V_{\text{SW,PGND}}$ - and substrate-dominated. Hence, a simplified circuit that describes this EMI transfer in the low-frequency limit has been constructed. This is shown in fig. 88. Except for the SYSGND-pins, the pin-inductances are not required. As shown in fig. 90 (a), below 90 MHz, this simplified circuit deviates from the initial model by less than 3 dB. The disturbance $V_{\text{SW,PGND}}$ is capacitively coupled to the wafer-substrate surface via $C_{\text{sub,LS}}$, and the resulting parasitic current divides among SEAL-RING and the die-backside. The former fraction evokes a ground bounce in SEAL-RING, due to its imperfect grounding. The SEAL-RING's ground bounce is coupled to transceiver #0 via $C_{\text{trench,t\#0}}$ and $C_{\text{sub,t\#0}}$.

Surprisingly, if the SEAL-RING node in fig. 88 would be cut, then transceiver #0 (left) and the DC/DC-converter (right) would decouple: Direct substrate

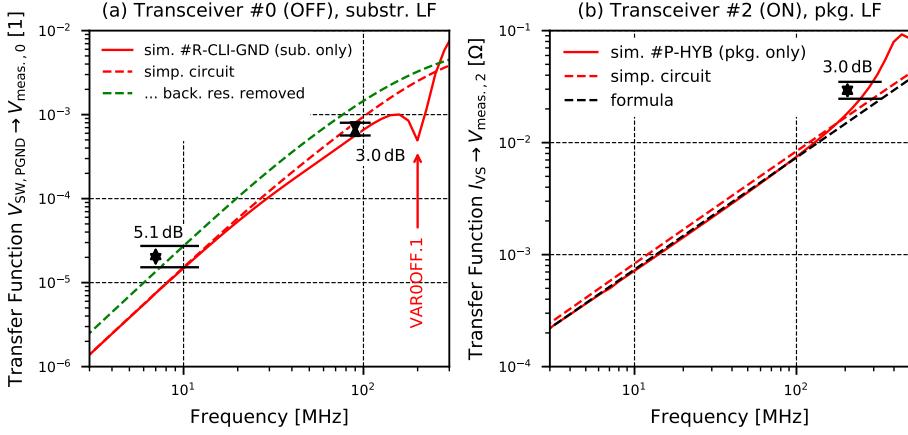


Figure 90: The dashed red curves in (a) and (b) depict the transfer functions $V_{SW,PGND} \rightarrow V_{meas,0}$ and $I_{VS} \rightarrow V_{meas,2}$ from the simplified circuits in fig. 88 and fig. 89, respectively. The solid red curves in (a) and (b) show the transfer functions from the corresponding initial models.

couplings to CS-EPI-TRO, e.g. $R_{INTER,t\#0}$ (fig. 88, crossed out in red), play only a minor role and can be neglected. Moreover, the n-buried layer of the intermediate region EPI-INTER and the associated substrate capacitances $C_{sub,INTER}$ and $C_{trench,INTER}$ can be neglected. This exemplifies that, in this frequency range, the disturbance in SYSGND and SEAL-RING is only due to currents picked up galvanically from the wafer-substrate. Note that the SEAL-RING node may not be confused with the actual chip seal ring (sec. 2.2) since it also encompasses the filling material of the deep trenches, approximated as perfect conductors (sec. 6.3.1). Thus, the parasitic resistors $R_{seal,...}$ may not be misunderstood as the wafer-substrate resistance to the chip seal ring, but rather as resistances to the deep trench connections. However, $R_{seal,...}$ not only account for the *immediately adjacent* deep trench: For example, using the data from sec. 5.1.1, a nearest-neighbor resistance of $50\ \Omega$ was estimated for MH. This is roughly 2.6 times larger than $R_{seal,HS}$ from table I3.

Backside grounding acts on the wafer-substrate resistances in two different ways: Firstly, as opposed to a non-connected die-backside, resistors connecting the wafer-substrate surface to the PCB-ground are present, e.g. $R_{LS,0}$ in fig. 90. The value of these backside resistors can be easily and precisely predicted given the device area A and the substrate height h , i.e. $R = \rho_{SUB}A/h$. Secondly, the presence of a grounded die-backside acts as a shield, and hence it increases resistances that interconnect wafer-substrate surface nets. For example, as shown in table I3, $R_{INTER,HS}$ is decreased two-fold in #R-CLI-NC. Both effects help to reduce the transfer function, e.g. by diverting more para-

sitic current through the die-backside. The shielding effect is not pronounced in the discussed low-frequency model, which can be verified using fig. 88 and table 13.⁵² Thus, the disadvantage of a non-connected die-backside can be predicted by merely deleting all backside resistors in fig. 88. The resulting transfer function is depicted by the dashed green curve in fig. 90. It predicts that backside grounding gains of 5.1 dB at 10 MHz, which is consistent with simulation results of #R-CLI-GND and #R-CLI-NC from sec. 6.5.3 (difference 5.9 dB, fig. 79). However, note that the experimentally observed gain is actually 11 dB (fig. 77). The discrepancy from measurement is due to the fact that these simplified circuits have inherited the neglect of $R_{tr,long,comp}$ from the low-dimensional resistor models, as explained in sec. 6.5.4.

Inductive package-coupling of I_{VS} below 290 MHz The RF-emissions at transceiver #2 in the ON-state are I_{VS} - and package-dominated (see sec. 6.5.1). Fig. 89 depicts a simplified circuit that covers this EMI transfer mechanism. As shown in fig. 90 (b), it is valid even up to 290 MHz, with a deviation from the initial model by less than 3 dB. It was found that in the ON-state, the transceiver diode and MOSFET (i.e. DT2, MT2) can be approximated by an ideal short, as shown in fig. 89. In this circuit, the current I_{VS} flows through the VS-PGND pin-loop⁵³, and it induces a voltage across the VTR-TR2 pin-loop. The 150 Ω decoupling network approximately acts as a voltage divider, and hence the measured voltage $V_{meas,2}$ is smaller by a factor of 25/145 than this induced AC-voltage. Since the two VTR-pins are very close to each other, one may as well drop VTR#1 without affecting the mutual inductance between the VS-PGND and the VTR-TR2 pin-loops. Moreover, for the same reason, one may delete PGND#1 and VS#1. This leads to the following simple solution:

$$\frac{V_{meas,2}}{I_{VS}} = \frac{25}{145} i\omega (M_{VTR\#0,VS\#0} - M_{VTR\#0,PGND\#0} - M_{t\#2,VS\#0} + M_{t\#2,PGND\#0}) \quad (104)$$

where $M_{i,j} := \kappa_{i,j} \sqrt{L_{pkg,i} L_{pkg,i}}$ is the mutual ground-return inductance (see sec. 3.2.2). Eq. (104) is depicted by the dashed black curve in fig. 90 (b). The good alignment between the dashed black and red curve validates the IC-package coupling mechanism presumed in sec. 3.1.

⁵² Conversely, e.g. in $R_{INTER,HS}$, this shielding effect causes a reduction by a factor of two, and for a smaller die thickness this reduction factor is presumably even larger. Note that $R_{INTER,HS}$ occurs in the high-frequency model fig. 91.

⁵³ The fraction of the current flowing over SW was found to be negligible, and hence, the corresponding part of the IC-package model was removed.

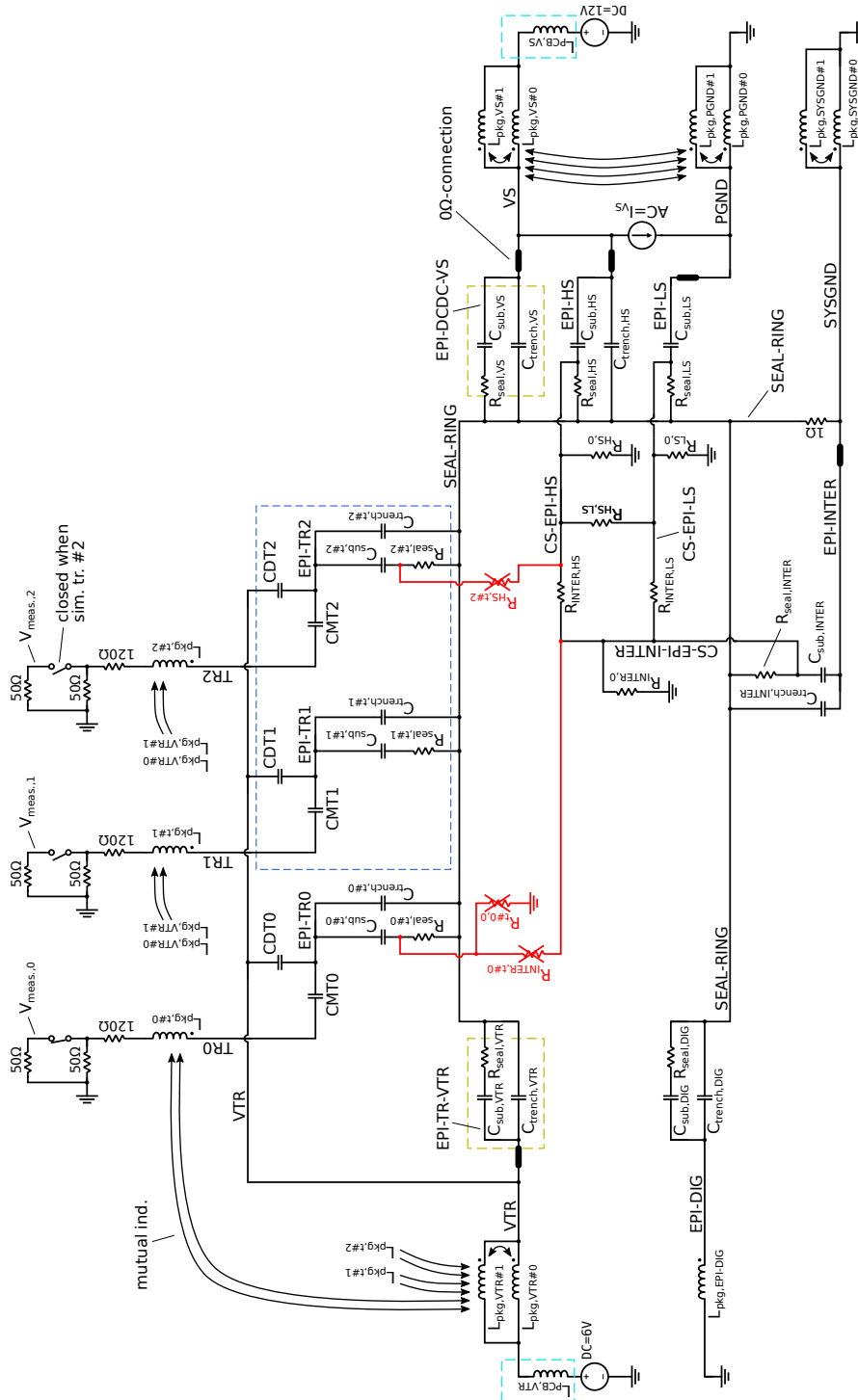


Figure 91: Simplified circuit that describes the transfer function from I_{VS} to transceivers #0, #1 and #2 in the OFF-state under package coupling knock-out. It is valid at least in the range from 100 MHz to 1 GHz. The elements crossed out in red exemplify parasitic elements that were deleted.

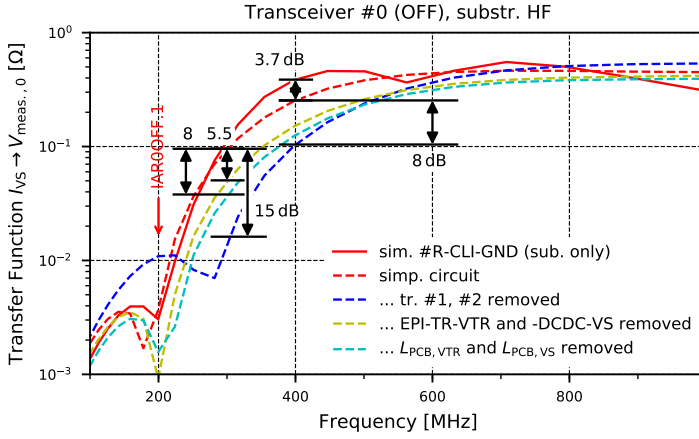


Figure 92: The dashed red curve depicts the transfer function $I_{VS} \rightarrow V_{\text{meas},0}$ from the high-frequency model in fig. 91. The solid red curve show the transfer functions from the corresponding initial model. In the dashed blue, yellow and cyan curves, the parts of fig. 91 marked in blue, yellow and cyan, respectively, were removed.

Substrate-coupling of I_{VS} above 100 MHz The circuit model in fig. 88 describes the substrate noise transfer only up to 90 MHz. However, secondary substrate-coupling-induced maxima in the RF-emission spectrum, which can even exceed the first maximum at 100 – 200 MHz, were observed up to 500 MHz. Thus, it is desirable to understand the substrate noise transfer at higher frequencies, i.e. significantly above 90 MHz. As noted in sec. 6.5.1, at higher frequencies, the RF-emissions are dominated by an indirect coupling of I_{VS} involving the substrate. Fig. 91 shows a circuit that describes this high-frequency RF-transfer. This circuit was simplified to a great extent.⁵⁴ The simplification reduced the accuracy by only 3.7 dB, which is revealed by comparing the solid and the dashed red curve in fig. 92. It is immediately apparent that this high-frequency model is much more complex than the low-frequency model in fig. 88.

A great part of the AC-current I_{VS} in fig. 91 is forced across the VS-PGND pin-loop. This results in voltage-ripples at VS and PGND, which cause parasitic currents across $C_{\text{sub,LS}}$, $C_{\text{sub,HS}}$ and $C_{\text{sub,VS}}$, as well as across the corresponding trench-oxide capacitances. These parasitic currents can be galvanically transferred to the SEAL-RING node, or they can couple capacitively to the SYSGND node via EPI-INTER. It may appear counterintuitive that SW, and hence EPI-LS, in fig. 91 are shorted to PGND: This follows from the formalism

⁵⁴ Recall that the DC/DC's low-side switch is surrounded by a floating trench ring (sec. 6.3.1). Therefore, the trench-oxide capacitor $C_{\text{trench,LS}}$ does not exist in fig. 92. This is also thought to be the reason why $R_{\text{seal,LS}}$ is significantly larger than $R_{\text{seal,HS}}$ in table 13.

using the substitution theorem (sec. 6.3.2), and from the fact that one must equate $V_{\text{SW,PGND}} = 0 \text{ V}$ in order to predict the I_{VS} -transfer-function.

It is striking that all three transceivers exclusively decouple the disturbance from the SEAL-RING node, via $C_{\text{trench,t\#*}}$, $C_{\text{sub,t\#*}}$ and $R_{\text{seal,t\#*}}$: Similar to the previously discussed low-frequency model, other couplings like $R_{\text{INTER,t\#0}}$ can be neglected. This results in a symmetry among the transceivers, which explains why the observed substrate-emissions above 100 MHz were mostly distance-independent (see sec. 6.6.1).⁵⁵ Note that even the direct wafer-substrate cross-talk between the pass device of transceiver #2 and the high-side switch of the DC/DC converter, which is represented by $R_{\text{HS,t\#2}}$, is negligible. This is despite the fact that these two HV-devices have an edge-to-edge distance of only 50 μm . The observed difference of the substrate-emissions between transceiver #1 and #2 of about 3–6 dB between 50 MHz and 100 MHz (sec. 6.6.1) is *not* related to the neglect of $R_{\text{HS,t\#2}}$: Rather, since this difference is also not present in simulations using the complete #R-CLIGND substrate model, it is presumed that this is rather brought about by the composite longitudinal trench resistance. It can be concluded that the dominant substrate transfer mechanism is due to the trench/seal-ring/system-ground-subsystem, both, at low and at high frequencies. This motivates why improving the grounding of SYSGND and SEAL-RING results in sizeable reductions of the RF-emissions (sec. 6.6.3).

The dashed blue curve in fig. 92 depicts the transfer function to transceiver #0, in the case that transceivers #1 and #2 are removed from the high-frequency model. Specifically, the circuit elements encapsulated in the dashed blue rectangle in fig. 91 were deleted. At 400 MHz, this results in a decrease of the RF-emissions by 8 dB. Furthermore, a frequency-shift of the anti-resonance IAR0OFF.1 is observed. A detailed discussion thereof is beyond the scope of this thesis. At 300 MHz, the error introduced to the transfer function was even 15 dB, due to the close proximity to this anti-resonance. This shows that, at frequencies beyond 200 MHz, the neglect of seemingly unrelated neighboring modules can cause significant mispredictions. Observe that even the package inductances of these neighboring transceivers must be included. This is in contrast to the low-frequency model discussed previously (fig. 89), in which transceivers #1 and #2 could be entirely neglected.

In the dashed yellow transfer function in fig. 92, the parasitic connections from the SEAL-RING to the EPI-DCDC-VS and EPI-TR-VTR nodes were inhibited (yellow rectangles in fig. 91). EPI-TR-VTR and EPI-DCDC-VS refer to

⁵⁵ In addition, the higher the frequency the more TR0–2 are coupled via CMT0–2 and via the common power rail VTR. This also contributes to the distance-independence of the substrate emissions in this particular IC.

rather small fragments of the n-epitaxial layer located in the areas marked by *1) and *2), respectively, in fig. 66. Despite they exhibit quite small substrate capacitances of less than 6 pF (see $C_{\text{sub,VTR}}$, $C_{\text{sub,VS}}$, $C_{\text{trench,VTR}}$ and $C_{\text{trench,VS}}$ in tables 14 and 15), they amount for an increase of the RF-emissions by 5.5 dB at 300 MHz in this model. The n-epitaxial layer fragments connected to EPI-TR-VTR and EPI-DCDC-VS might as well be connected to SYSGND instead because they are part of LV-pockets (sec. 2.2) in which this connection is arbitrary. However, often, the highest potential is connected to the n-epitaxial layer, in order to minimize C_{sub} . These results suggest that this may be a poor heuristic because thereby the overall coupling from these noisy or sensitive nodes to SEAL-RING, SYSGND and EPI-INTER is increased. Thus, in small LV-pockets, re-connecting the n-epitaxial layer to SYSGND should be considered, in case simulations predict that this would reduce the RF-emissions.

It is remarkable that the removal of two very small parasitic inductances on the PCB resulted in a decrease of the transfer function by 8 dB at 300 MHz. This is shown by the cyan curve in fig. 92. These parasitic inductances $L_{\text{PCB,VTR}}$ and $L_{\text{PCB,VS}}$ mostly represent the ESL of the first decoupling capacitors of VTR and VS, respectively. This does *not* imply that the RF-emissions could be reduced by up to 8 dB using a PCB-redesign: If the ESL of the decoupling capacitor at VS was reduced, also the spectra of $V_{\text{PGND,SW}}$ and I_{VS} would be altered, which might partly cancel this improvement. Nevertheless, this highlights that the modeling of the PCB, especially the impedance attached to multi-bonded, low-inductance power supply and ground pins, should be given more attention. Since an $L_{\text{PCB,VTR}}$ of only 0.6 nH (table 18) is already significant, the question arises why it was not necessary to include the on-die routing inductance of the VTR-net: Presumably, this is due to the fact that the VTR-net was routed in the form of a roughly 500 μm wide and 2200 μm long power metal plate, which is contacted by four bond wires approximately attach at its center.⁵⁶ However, it is recommended that future EMI-simulations account for such inductances by applying RLCK parasitic extraction to low-ohmic power and ground routings (chapter 4).

Conclusion The presented approach to obtain simple circuits might be useful in the conceptual design phase. One might even go one step further and attempt to use fig. 88 and fig. 91 as a kind of template, in which the parasitic elements are further parameterized by geometric properties of the design. However, it must be stressed that, because these circuits may deviate up to 3 dB from the “initial model”, they merely capture the *leading-order* substrate coupling mechanism that is present in the analyzed IC: Thus, with pessimistic assumptions, one might suspect a secondary coupling mechanism that is only

⁵⁶ This routing style is also found in some productive ICs.

about 8 dB weaker, but which was completely erased during the simplification. For example, if the impedance of the system-ground is significantly reduced, e.g. by using multiple down-bonds (sec. 6.6.3), such a secondary coupling mechanism might turn into leading order, which would render such templates inappropriate. In conclusion, the presented approach to obtain simple circuits is very useful for in-depth root-cause analyses. However, the compactness of fig. 88 and fig. 91 might suggest a false sense of simplicity and generality. Moreover, they inherently neglect the composite longitudinal trench resistance and hence don't completely cover the impact of die-backside-grounding-, distance- and ρ_{SUB} -variations. Thus, it is strongly recommend to cross-check such conceptual considerations against AC-simulations of more complete models based on substrate extraction.

Parameter	Val. [Ω] *	Val. n.c. [Ω] **	Parameter	Val. [Ω] *	Val. n.c. [Ω] **
$R_{\text{seal},t\#0}$	40	39	$R_{\text{INTER},\text{HS}}$	319	162 ($\times 2.0$)
$R_{\text{seal},t\#1}$	44	43	$R_{\text{INTER},\text{LS}}$	83	64 ($\times 1.30$)
$R_{\text{seal},t\#2}$	42	41	$R_{\text{HS},\text{LS}}$	123	86 ($\times 1.43$)
$R_{\text{seal},\text{VTR}}$	47	46	$R_{\text{HS},t\#2}$	540	320 ($\times 1.69$)
$R_{\text{seal},\text{DIG}}$	33	32	$R_{\text{INTER},t\#0}$	174	133 ($\times 1.31$)
$R_{\text{seal},\text{INTER}}$	3.9	3.9	$R_{t\#0,0}$	168	–
$R_{\text{seal},\text{VS}}$	55	55	$R_{\text{INTER},0}$	28	–
$R_{\text{seal},\text{HS}}$	19	19	$R_{\text{HS},0}$	53	–
$R_{\text{seal},\text{LS}}$	49	46	$R_{\text{LS},0}$	64	–
* Low-dimensional resistor network with a grounded die-backside, which uses the CLI boundary condition below n-epitaxial pockets and PCV boundary conditions below deep trenches (#R-CLI-GND) ** Variant of * in which the die-backside is non-connected (#R-CLI-NC). The values in brackets are the quotients between the columns * and **.					

Table 13: Effective wafer-substrate resistors between relevant n-epitaxial pockets.

Parameter	Val. [pF]	Parameter	Val. [pF]	Parameter	Val. [pF]
$C_{\text{sub},t\#0}$	17.3	$C_{\text{sub},\text{VTR}}$	5.4	$C_{\text{sub},\text{VS}}$	4.0
$C_{\text{sub},t\#1}$	17.3	$C_{\text{sub},\text{DIG}}$	91.0	$C_{\text{sub},\text{HS}}$	44.0
$C_{\text{sub},t\#2}$	17.3	$C_{\text{sub},\text{INTER}}$	237.9	$C_{\text{sub},\text{LS}}$	45.1

Table 14: Junction capacitance of selected n-epitaxial pockets to the wafer substrate.

Parameter	Val. [pF]	Parameter	Val. [pF]	Parameter	Val. [pF]
$C_{\text{trench},t\#0}$	3.7	$C_{\text{trench},VTR}$	3.0	$C_{\text{trench},VS}$	2.1
$C_{\text{trench},t\#1}$	3.7	$C_{\text{trench},DIG}$	5.9	$C_{\text{trench},HS}$	8.3
$C_{\text{trench},t\#2}$	3.7	$C_{\text{trench},INTER}$	45.8	–	

Table 15: Trench-oxide capacitances of selected n-epitaxial pockets.

Parameter	Val. [nH]	Parameter	Val. [nH]	Parameter	Val. [nH]
$L_{\text{pkg},PGND\#0}$	2.9757	$L_{\text{pkg},SYSGND\#0}$	5.0822	$L_{\text{pkg},t\#0}$	4.6399
$L_{\text{pkg},PGND\#1}$	2.9442	$L_{\text{pkg},SYSGND\#1}$	4.5415	$L_{\text{pkg},t\#1}$	4.4778
$L_{\text{pkg},VS\#0}$	3.3526	$L_{\text{pkg},VTR\#0}$	3.8482	$L_{\text{pkg},t\#2}$	4.9538
$L_{\text{pkg},VS\#1}$	4.0772	$L_{\text{pkg},VTR\#1}$	3.9070	$L_{\text{pkg},EPI-DIG}$	4.1427

Table 16: Ground-return inductances of selected pins.

Parameter	Val. [I]	Parameter	Val. [I]
$\kappa_{PGND\#0,PGND\#1}$	$4.8971 \cdot 10^{-1}$	$\kappa_{VTR\#1,PGND\#1}$	$5.8165 \cdot 10^{-3}$
$\kappa_{VS\#0,VS\#1}$	$4.1725 \cdot 10^{-1}$	$\kappa_{VTR\#0,VS\#0}$	$8.0318 \cdot 10^{-3}$
$\kappa_{SYSGND\#0,SYSGND\#1}$	$1.5311 \cdot 10^{-1}$	$\kappa_{VTR\#0,VS\#1}$	$8.6747 \cdot 10^{-3}$
$\kappa_{VTR\#0,VTR\#1}$	$4.7090 \cdot 10^{-1}$	$\kappa_{VTR\#1,VS\#0}$	$9.3380 \cdot 10^{-3}$
$\kappa_{VS\#0,PGND\#0}$	$1.3396 \cdot 10^{-1}$	$\kappa_{VTR\#1,VS\#1}$	$1.0154 \cdot 10^{-2}$
$\kappa_{VS\#1,PGND\#0}$	$9.1318 \cdot 10^{-2}$	$\kappa_{t\#0,PGND\#0}$	$2.9256 \cdot 10^{-3}$
$\kappa_{VS\#0,PGND\#1}$	$1.8374 \cdot 10^{-1}$	$\kappa_{t\#0,PGND\#1}$	$3.2491 \cdot 10^{-3}$
$\kappa_{VS\#1,PGND\#1}$	$1.2141 \cdot 10^{-1}$	$\kappa_{t\#1,PGND\#0}$	$7.1690 \cdot 10^{-3}$
$\kappa_{VTR\#0,t\#0}$	$1.9101 \cdot 10^{-1}$	$\kappa_{t\#1,PGND\#1}$	$8.2543 \cdot 10^{-3}$
$\kappa_{VTR\#1,t\#0}$	$1.3675 \cdot 10^{-1}$	$\kappa_{t\#2,PGND\#0}$	$1.5069 \cdot 10^{-2}$
$\kappa_{VTR\#0,t\#1}$	$1.4957 \cdot 10^{-1}$	$\kappa_{t\#2,PGND\#1}$	$1.7878 \cdot 10^{-2}$
$\kappa_{VTR\#1,t\#1}$	$2.0665 \cdot 10^{-1}$	$\kappa_{t\#0,VS\#0}$	$4.8335 \cdot 10^{-3}$
$\kappa_{VTR\#0,t\#2}$	$4.2339 \cdot 10^{-2}$	$\kappa_{t\#0,VS\#1}$	$5.1202 \cdot 10^{-3}$
$\kappa_{VTR\#1,t\#2}$	$5.2538 \cdot 10^{-2}$	$\kappa_{t\#1,VS\#0}$	$1.4032 \cdot 10^{-2}$
$\kappa_{VTR\#0,PGND\#0}$	$4.5195 \cdot 10^{-3}$	$\kappa_{t\#1,VS\#1}$	$1.5623 \cdot 10^{-2}$
$\kappa_{VTR\#0,PGND\#1}$	$5.0967 \cdot 10^{-3}$	$\kappa_{t\#2,VS\#0}$	$3.4201 \cdot 10^{-2}$
$\kappa_{VTR\#1,PGND\#0}$	$5.1330 \cdot 10^{-3}$	$\kappa_{t\#2,VS\#1}$	$4.0462 \cdot 10^{-2}$

Table 17: Coupling coefficients of Ground-return inductances of selected pins.

Parameter	Description	Value
CDT0/1/2	Effective capacitance across DT0/1/2 in the OFF-state	74.5 pF
CMT0/1/2	Effective capacitance across MT0/1/2 in the OFF-state	37.1 pF
$L_{\text{PCB,VTR}}$	Effective parasitic ind. of PCB power supply network of VTR at 300 MHz	0.6 nH
$L_{\text{PCB,VS}}$	Effective parasitic ind. of PCB power supply network of VS at 300 MHz	0.8 nH
CDIG	The total capacitance between DVCC and DGND in the digital core	0.416 nF
RDIG	The ESR the digital core's capacitance (CDIG)	1.11 Ω
CDLOG	Total capacitance between the logic-implant and the n-epitaxial layer in the digital core	0.21 nF
RDNEPI	Effective connecting resistance of the n-buried layer in the digital core	9.1 Ω

Table 18: Auxiliary effective parasitics occurring in the simplified circuit diagrams.

6.8 Summary

- To predict the RF-emissions, a system model was created that comprises the PCB, the IC-package, the substrate, as well as the relevant semiconductor devices. The IC-layout had to be simplified manually, in order to keep the substrate model's complexity at a reasonable level. Also the integrated circuitry was strongly simplified – for example, the digital core was replaced by a single lumped capacitor with ESR/ESL. Moreover, the central functions and the transceiver gate drivers were highly abstracted.
- The substrate model typically neglects wells inside the n-buried layer, and it does not cover implants above the logic-implant. It includes the n-sinker resistance, the longitudinal trench resistance and an RC-model of the metallization that connects the n-sinkers and deep trenches. Moreover, it includes the trench oxide capacitance.
- The DC/DC-converter was simplified and replaced by two small signal sources $V_{SW,PGND}$ and I_{VS} , which allows to predict the RF-emissions using AC-simulations. The spectra of $V_{SW,PGND}$ and I_{VS} can be determined using a preceding transient simulation. $V_{SW,PGND}$ and I_{VS} were shown to be roughly unaffected by substrate parasitics, and, in contrast to the RF-emission spectrum, small long-range mutual inductances have a negligible impact on them. Thus, the preceding transient simulation can be performed on the schematic level, and the complete simulation process is accelerated by orders of magnitude.
- The measurement and simulation results are visualized in an unusual representation, which allows to abstract from phase-noise, clock jitter and inaccuracies of the duty cycle: Firstly, the spectrum is measured using an RMS-detector, and the power under each peak is integrated. Secondly, above 30 MHz, only the maximum of each pair of subsequent even and odd harmonics is shown.
- For the DC/DC's RF-emissions, the developed methodology typically achieves an accuracy of ± 6 dB up to 1 GHz, which is considered sufficient. However, spurious destructive interference constitute a problem, and, in one case, this caused an error > 10 dB in the rather wide frequency band of 15 MHz to 45 MHz. A related issue are spurious local minima in the current spectrum I_{VS} . Heuristic solutions include the use of hull curves for I_{VS} and $V_{SW,PGND}$, and discarding the transfer function phase. A more general countermeasure against coincidental parameter matching might be a Monte-Carlo procedure.
- This section exemplified a procedure that automatically extracts simple circuits from models containing a large number of parasitic elements. These simple circuits are even amenable to pencil-and-paper calculations. This is achieved by using alteration analysis to rate the relevance of each parasitic element. Two circuit models were constructed that predict the substrate noise transfer of $V_{SW,PGND}$ and I_{VS} , respectively. It is striking that all three transceivers exclusively decouple the disturbance from the SEAL-RING node. This explains why the RF-emissions above 200 MHz, as well as the substrate-emissions in general, were mostly independent of the distance from the DC/DC-converter.

CHAPTER 7

Conclusion and Outlook

In this thesis, a methodology for the EMC-compliant design and verification of Automotive System ICs was developed. It is based on novel physically-based techniques for IC-package- and substrate-modeling. These physically-based techniques are tailored towards the stringent requirements of EMC-simulations regarding efficiency and accuracy. In addition, the inductances and RF-losses in on-die power routing were experimentally investigated in a proprietary BCD-technology. The methodology was verified using very detailed measurements on a test-IC that was specifically developed for this purpose.

The accuracy requirements on IC-package models for the use in EMC-simulations go far beyond what is usually needed in functional verification. This was exemplified by the fact that mutual pin-loop inductances of only 5.4 pH, i.e. three orders of magnitude below typical pin-inductances, can cause EMI-violations. A large number of these small long-range mutual inductances must be accurately represented in the model. However, such a high accuracy was barely achievable if the IC-package model is based on passivity-enforced vector fitting of S-parameters. As an alternative to reduced-order macromodels, it was proposed to synthesize lumped-element models that contain ground-return inductances. This can be achieved using parasitic extraction techniques, but different from the conventional approach, an array of terminals must be added to the ground plane. These are needed in order to correctly model magnetic shielding by the PCB-ground plane. For example, it was shown that an error of up to 19 dB can occur in the prediction of the DC/DC's RF-emissions if the PCB-ground plane is entirely neglected – this is exactly confirmed in the simulations of the test-IC. Similar lumped-elements models can be also obtained by decomposing the port-based H-parameter representation of an electromagnetic field simulation result. Despite the lumped-element models are merely based only on data from a single frequency point, by adding heuristic ladder-models, the skin-effect can be reintroduced retrospectively. It was shown that this construction does not disturbing the subtle matching among mutual ground-return inductances, which is important for EMC-simulations.

Inductances in on-die power routing may affect the RF-emissions as well as the RF-immunity. For example, the additional on-die resistance and inductance may become a concern if a supply- or ground-pin is shared among multiple modules. Moreover, in future high-frequency extensions of DPI-

testing, resonances in low-voltage internal power domains may increase in relevance. To study these effects experimentally, in the course of this thesis, test-wafers were developed and fabricated using a simplified process. The quality factor of on-die resonances is rather difficult to predict. In this thesis, the inductive RF-losses in the power routing, which affect the quality factor, were exhaustively quantified. It was demonstrated how eddy-current losses in the metallization can be exploited to dampen these resonances. Moreover, the eddy-current losses in the n-buried layer were characterized in measurement and simulation. They were shown to be significantly larger than the losses due to the skin effect. This thesis introduces the notion of a critical distance, beyond which coplanar strips magnetically decouple into two transmission lines, which are alike to microstrip lines over the n-buried layer. For example, measurements have revealed a critical distance of only 130 μm at 8 GHz. Numerical calculations of the TEM-mode have revealed that the critical distance is roughly proportional to $f^{-0.85}$. In this thesis, the limitations of RLCK-extraction tools in EMC-simulations were explored, and concepts for tool-qualifications were developed. It was demonstrated how RLCK-extraction tools can be used to obtain efficient and precise EMC-simulation models: If the considerations in this thesis are taken into account, these models correctly describe the emergent Metal-Insulator-Semiconductor slow-wave transmission lines, eddy-current losses in the metallization as well as small long-range couplings.

It was illustrated that approximating the n-buried layer as equipotential allows to create very compact *low-dimensional* substrate models. After further simplification using alteration or sensitivity analysis, these models even facilitate pencil-and-paper calculations, and enable a physically-based discussion of the leading-order EMI coupling mechanism. The underlying approximation is justified for n-epitaxial pockets smaller than a certain critical area A_c , as well as for HV-devices with a finger-pitch below $\sqrt{A_c}$. Traditionally, field simulations of the wafer-substrate based on the PCV-boundary condition were sometimes used. However, this thesis has shown that, for rather low frequencies like 100 MHz, this can strongly misjudge the substrate resistors emanating from large-area n-epitaxial pockets. For example, the substrate resistors to the surrounding deep trenches can be underestimated by up to a factor of 8. As a remedy, this thesis introduces the novel CLI boundary condition, which alters the boundary current distribution such that it correctly reflects the capacitive current injected by the n-buried layer. The electrical nodes in the resulting resistor network can be interpreted as the *average surface potential* of the wafer-substrate.

However, these low-dimensional substrate models cannot easily incorporate the inductance of the seal-ring, the n-sinker resistance and their metal routing. Moreover, further software automation is needed for the seamless integration with metal parasitics, and in order to account for the composite longitudinal trench resistance. To overcome these limitations, in the course of this thesis, a novel substrate extraction tool was implemented. This tool was developed in C++ and is based on 1st-order FEM. The tool is highly customizable and unique in the aspect that the precise semantics of the field model are transparent and available to the user. It was estimated that a four-fold refinement of the 2D mesh resolution increases the simulator run time by up to a factor of 256, even though an optimized non-uniform 3D mesh is used for the wafer-substrate. Thus, it is of paramount importance to interactively control the model's "level of detail". This can be achieved by a novel approach using marker layers. 2D FEM-elements in the n-buried layer can be easily coarsened up $A_c/2$. On the other hand, to enable a reduction of the 3D mesh, a new technique (S-EHRFEM), which preserves the accuracy of shallow current paths, e.g. in the vicinity of deep trenches, was invented. Its performance is expected to be similar to fast-Multipole BEM, but S-EHRFEM furthermore allows to use direct linear solvers as well, and the circuit simulator source code doesn't need to be modified. In practice, additional improvements of the run time might be achieved by using iterative linear solvers. It was shown that the generated substrate model is passive, reciprocal, charge-conserving and reference-independent. For use in technologies with an increased wafer-substrate resistivity, support for displacement currents could be added easily.

A test-IC was developed in the course of this thesis specifically for the purpose of evaluating the developed methodology. It contains a DC/DC-converter running at 3 MHz and a digital disturber clocked at 32 MHz, both of which can act as disturbance sources. The RF-emissions are measured at three transceiver pins, in each case in the recessive- and dominant bus state. Since each of the transceivers is located at a different distance from the DC/DC-converter, their RF-coupling paths differ. To predict the RF-emissions, a system model was created that comprises the PCB, the IC-package, the substrate, as well as the relevant semiconductor devices. Care must be taken when integrating the IC-package-model and the substrate-model because parasitic currents can leave the backside of the wafer-substrate through the exposed pad. The IC-layout had to be simplified manually, in order to keep the substrate model's complexity at a reasonable level. Furthermore, by exploiting AC-simulations, the simulation was accelerated by orders of magnitude: To this end, the DC/DC-converter was simplified to two small signal sources $V_{SW,PGND}$ and I_{VS} . The errors introduced by this approximation were mostly negligible.

Note that the used DC/DC-converter design, in addition to the capacitively-injected parasitic currents (majority carriers), also injects small *minority*-carrier currents into the wafer-substrate. However, these minority carrier currents are apparently a negligible contributor to the RF-emissions. This was shown by the good alignment between measurement with the simulation, in which minority carriers were completely neglected.

In all transceivers, in both bus states and from 3 MHz to 1 GHz, a good accuracy was achieved in the prediction of the DC/DC's RF-emissions, with deviations typically less than ± 6 dB. Singular special cases with a higher deviation were meticulously investigated: For example, they could be attributed to spurious destructive interferences between substrate- and package-coupling, and to missing local minima in the I_{VS} -spectrum at very high harmonics. Possible solutions include the use of fitted hull-curves, discarding of certain phase information, and Monte-Carlo simulations. Carefully-designed *package knock-out* models and *substrate knock-out* models were studied. Thereby, it was shown how, depending on the frequency range, the bus state and the distance, the RF-emissions can be substrate- or package-dominated. It was found that substrate can be the dominant coupling mechanism even down to 3 MHz. Moreover, the substrate model cannot be trivialized: The p-n-junction below the n-buried layer must be treated as a continuum, and the resistivity of the wafer-substrate has a large impact. Moreover, the trench-oxide capacitances, the intrinsic longitudinal trench resistance and the metallization that connects deep trenches are relevant. It is counterintuitive that a deterioration of the deep-trench-based wafer-substrate grounding can actually improve the RF-emissions. This is due to the fact that the capacitively injected disturbance current is divided between the die-backside and the on-die ground. Further research should investigate whether the seal-ring inductance might become relevant if it was grounded at the far side of the transceivers. This might be investigated using a future test-ICs.

The RF-emissions of the digital disturbance source were measured and simulated up to 3 GHz. With few exceptions, the RF-emissions are primarily coupled via the wafer-substrate. It was found that the simplistic small-signal equivalent of the digital core, termed RLC(.5, .5), is only accurate up to 250 MHz. At higher frequencies, a more detailed model of the digital core, which accounts for the distribution of its capacitance, the inductance, the resistance and the switching currents, is apparently required. Nevertheless, it is thought that using RLC(.5, .5) always yields an upper bound to the actual RF-emissions, and can hence be employed for conservative estimates. Moreover, using RLC(.5, .5), one can precisely predict the benefit of separating the digital ground up to 1 GHz. Firstly, introducing a new ground pin for the

digital core and, secondly, separating it from the system ground reduces the RF-emissions by a total of 31 dB at 50 MHz and 15 dB at 300 MHz in measurement – but note that above 500 MHz the benefit was negligible. However, this ground separation also comes at a cost: It was estimated that the required level shifters alone increase the area of the digital core by at least 8%. Thus, at the concept phase IC-designers should carefully weigh the costs and benefits, e.g. an alternative might be to add more pins to the system ground.

Chip design counter-measures against RF-emissions fall into two categories: Suppression of the RF-coupling and shaping of the source spectrum. An increase in distance between the DC/DC-converter and the transceiver is *very effective* against inductive package-couplings, but were *almost completely ineffective* against substrate-coupled RF-emissions. This is due to the fact that these substrate-emissions are predominantly transmitted indirectly, where the seal-ring and the system ground form the mediator. It was predicted that, for a die-thickness of 220 μm , die-backside grounding can reduce the DC/DC's RF-emissions by up to 20 dB or 12 dB at low or high frequencies, respectively. Conversely, in measurements- and simulations of the DC/DC's RF-emissions, for a die-thickness of 600 μm , reductions of 11 dB (LF, 10 MHz) or 5.5 dB (HF, 800 MHz) were found. Note that in some ICs the die-backside may be electrically undefined – in practice, this can entail that the die-backside connection is only effective above a certain corner frequency. Moreover, it was predicted that the use of a more thin die and isolating deep trenches can easily gain another 10 dB to 20 dB on top of the reductions achieved by mere die-backside grounding. However, this would require a respective technology. Besides die-backside grounding, another effective counter-measure against substrate-coupling is to improve the grounding of the seal-ring. Circuit modifications that shield the DC/DC-converter or the digital core were *not* very useful because sufficiently low-noise and low-impedance ground nodes are not available at high frequencies, and because the connection resistance of the n-buried layer was too large. Reducing the RF-emissions by shaping the source spectrum is a very different approach: For example, reducing the DC/DC-converter's slew rate or the gate charge time can be effective, but there may be trade-off between slew-rate reduction and power-efficiency. The analysis implies that simultaneous reductions in the $V_{\text{SW,PGND}}$ - and the I_{VS} -spectrum result in exactly proportional reductions in the RF-emissions. In the considered DC/DC-design, beyond 100 MHz, the I_{VS} -spectrum was the more dominant parameter. In contrast to the RF-emissions, the $V_{\text{SW,PGND}}$ - and I_{VS} -spectra can be conveniently predicted on the schematic level, and require only a rudimentary package model. However, it must be taken into account that, at least from the 100-th harmonic onwards, these spectra are

not easily calculated using simple formulas, even if the precise rise-, fall- and gate-charge-timing is accounted for. In addition, e.g. the internal ringing at the DC/DC-converter must be considered, and thus, in this case, it is advisable to rather use an engineering process with transient simulation feedback.

In principle, the developed methodology could be extended to RF- and pulse-immunity. For example, to protect analog circuitry against a disturbance at their internal LV power domains, the transfer functions from RF-injection point can be predicted by the same means. Note that also pulses can be easily propagated using AC-simulations and the convolution theorem, except if strong non-linear distortions occur, e.g. if an ESD-diode is opened. In general, it should be assumed that transfer functions to internal LV power domains depend on the substrate model as well. Firstly, in many cases, the LV power domains or the pre-regulated voltage are connected to a part of the n-buried layer. Secondly, the ground bounce will be equally reflected as a disturbance of the voltage difference between the internal battery voltage and the internal system ground. Since large parts of the n-buried layer are grounded, the parasitic currents it draws from the wafer-substrate can cause a significant ground bounce, as has been shown. The substitution theorem is applicable to RF- and pulse-immunity as well, except that here, the surrounding system is replaced by time-controlled sources. In the future, a test-IC should be designed to exercise the methodology on RF-immunity. This test-IC should also evaluate the proposed novel approach to dampen on-die resonances.

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Own Publications

- A. Schade, F. Klotz, S. Jahn, and R. Weigel, "Modeling and measurement of RF-emissions at transceiver pins in automotive system ICs caused by integrated DC/DC-converters," in *International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020. DOI: 10.1109/EMCEurope48519.2020.9245833
- A. Schade, F. Klotz, S. Jahn, and R. Weigel, "Modellierung und Messung von Emissionen an Transceiverpins in Automotive-System-ICs, verursacht durch integrierte DC/DC-Wandler," in *Internationale Fachmesse und Kongress für Elektromagnetische Verträglichkeit*, 2020. DOI: 10.15488/10047.
- A. Schade, F. Klotz, S. Jahn, and R. Weigel, "S-EHRFEM – Substrate extraction using highly reduced FEM-meshes for transient SPICE-simulation with iterative linear solvers," in *International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2019 (Best paper award nominee in the regular category). DOI: 10.1109/EMCEurope.2019.8872008.

In the recent decades, automotive electronics has undergone a rapid evolution towards highly complex multi-function chips. So-called Automotive System ICs can integrate multiple DC/DC-converters, a logic core, linear regulators, smart switches, sensor interfaces and transceivers on a single die. If electromagnetic compatibility (EMC) issues are discovered late, the complex investigations and the required rework can significantly prolong the time-to-market. The methodology developed in this thesis employs novel physically-based modeling techniques for IC-package and substrate parasitics. The presented modeling techniques cope with the accuracy requirements of EMC-simulations.

Mutual pin-loop inductances of three orders of magnitude below typical pin-inductances can already cause noncompliance with the EMC-requirements. It will be shown that, if magnetic shielding by the PCB-ground plane is neglected, errors in the predicted RF-emissions of the DC/DC-converter can be up to 19 dB. The presented novel approach can take a large number of small mutual pin-loop inductances into account at a high accuracy. In this thesis, the inductances as well as the inductive RF-losses in the on-chip power routing will be quantified experimentally and reproduced by means of field simulation and parasitic extraction. In future high-frequency extensions of DPI-testing, internal resonances, the quality factor of which depends on the RF-losses, may increase in relevance. It was demonstrated how eddy-current losses in the metallization can be exploited to dampen these resonances. Furthermore, in this thesis, a flexible substrate extraction tool is developed. A novel marker layer concept and a novel 3D mesh compression technique (S-EHRFEM) helps to drastically reduce the simulator run time.

In the course of this thesis, a test-IC was developed, which contains a DC/DC-converter running at 3 MHz and a digital disturber clocked at 32 MHz, both of which can act as disturbance sources. The RF-emissions are evaluated at three different transceiver pins, in each case in the recessive and dominant bus state. In the frequency range from 3 MHz to 1 GHz, the simulations achieved a good accuracy in the prediction of the DC/DC's RF-emissions, with deviations typically less than ± 6 dB. The involved RF-coupling mechanisms are analyzed in detail and various counteractive measures, which attempt to suppress the RF-coupling path, are developed and tested experimentally.

