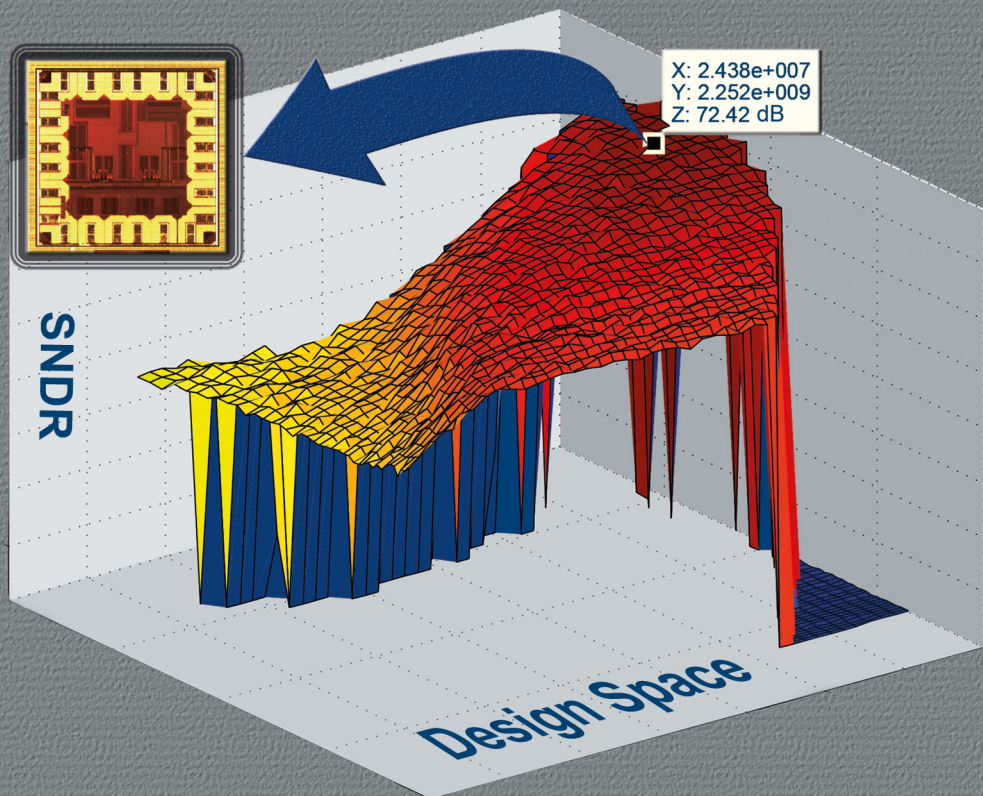




Sebastian Zeller

Wide-Bandwidth Single-Bit
Continuous-Time-Sigma-Delta-Modulation
for Area- and Power-Efficient A/D Conversion
with Low Jitter Sensitivity

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Breitbandige zeitkontinuierliche
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leistungseffiziente A/D-Umsetzung mit geringer
Jitter-Empfindlichkeit

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der Friedrich-Alexander-Universität
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Kurzfassung

Stetig steigender Bandbreitenbedarf, wachsende Systemkomplexität und hoher Kostendruck erfordern es, intelligente Konsumerprodukte mit Analog Mixed Signal (AMS)-Systems on Chip (SoCs) zu realisieren, die in modernen Ultra Deep Sub-Micron (UDSM) CMOS-Halbleitertechnologien hergestellt werden. Continuous-Time (CT)- $\Sigma\Delta$ -Analog-to-Digital Converters (ADCs) wurden zu einem wichtigen Baustein dieser SoCs, da sie einen exzellenten Kompromiss aus Dynamikbereich, Bandbreite und Verlustleistung bieten. Diese Eigenschaften machten CT- $\Sigma\Delta$ -ADCs zur ersten Wahl für Radio-schnittstellen in Smartphones.

Weitere Anstrengungen zur Reduktion von Chipfläche und Verlustleistung in dieser Klasse von ADCs sind jedoch für zukünftige Mobilgeräte, wie z.B. tragbaren Computern und intelligenten Sensorschnittstellen für das Internet of Things (IoT) erforderlich, die lange Batterielaufzeiten und trotz hoher Komplexität geringe Produktionskosten aufweisen müssen. Darüberhinaus sind solche Verbesserungen unter den sich stetig verschlechternden Eigenschaften analoger Bauteile aufgrund kleiner werdender Strukturgrößen in digitalen CMOS-Technologien zu erzielen.

In dieser Arbeit werden mehrere neuartige Entwurfstechniken zur Reduktion der Chipfläche und der Verlustleistung sowie zur Verbesserung der Eigenschaften und der Robustheit gegenüber Takt-Jitter von CT- $\Sigma\Delta$ -ADCs auf Architektur- und Transistorebene im Hinblick auf Implementierungen in UDSM-CMOS vorgeschlagen.

Zwei Testchips wurden entworfen und hergestellt, um die Wirksamkeit dieser Konzepte zu verifizieren: Ein robuster, im Wesentlichen analoger Single-Bit-CT- $\Sigma\Delta$ -ADC neunter Ordnung mit einer sehr hohen Maximum Stable Amplitude (MSA) als ein erster Demonstrator und schließlich ein im Wesentlichen digitaler 0.039 mm^2 , 1.82 mW CT- $\Sigma\Delta$ -ADC dritter Ordnung in 65 nm CMOS mit 10 MHz Bandbreite und 68.6 dB Peak Signal to Noise

and Distortion Ratio (SNDR_p). Mit einem minimalistischen aktiven Analogteil, der aus nur zehn Invertern besteht, ist dieser zweite Testchip einer der kompaktesten und leistungseffizientesten breitbandigen CT- $\Sigma\Delta$ -ADCs, die bisher publiziert wurden.

Abstract

Ever-increasing bandwidth demand, growing system complexity and cost pressure require to implement smart consumer devices with Analog Mixed Signal (AMS) Systems on Chip (SoCs) that are manufactured in state of the art Ultra Deep Sub-Micron (UDSM) CMOS semiconductor technologies. Continuous-Time (CT)- $\Sigma\Delta$ -Analog-to-Digital Converters (ADCs) have become an important interface building block of these SoCs as they provide an excellent compromise of dynamic range, bandwidth and power dissipation. These properties made CT- $\Sigma\Delta$ -ADCs the preferred choice for radio interfaces in smartphones.

However, efforts to further reduce the area and power consumption of this class of data converters are needed for future mobile devices such as wearable computers and smart sensor interfaces for the Internet of Things (IoT) that require a long battery lifetime and low production cost despite high complexity. Moreover, this improvement has to be achieved under steadily degrading properties of analog components due to shrinking feature size in digital CMOS technologies.

In this work, several novel design techniques that reduce the chip size and power consumption and improve the performance and clock jitter robustness of CT- $\Sigma\Delta$ -ADCs on architectural and transistor level are proposed with an emphasis on UDSM CMOS implementations.

Two testchips have been designed and manufactured to prove these concepts: A robust mostly-analog ninth order single-bit CT- $\Sigma\Delta$ -ADC with a very high Maximum Stable Amplitude (MSA) as a first test vehicle and finally a mostly-digital 0.039 mm^2 , 1.82 mW third order CT- $\Sigma\Delta$ -ADC in 65 nm CMOS with 10 MHz bandwidth and 68.6 dB Peak Signal to Noise and Distortion Ratio (SNDR_p). Using a minimalistic active analog section that consists of only ten inverters, this second testchip is one of the most compact and power-efficient wideband CT- $\Sigma\Delta$ -ADCs published so far.

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List of Acronyms

3D	3-Dimensional
A/D	Analog-to-Digital
A	Ampere
ABE	Analog Backend
AC	Alternating Current
ADC	Analog-to-Digital Converter
AFE	Analog Frontend
AM	Amplitude Modulation
AMS	Analog Mixed Signal
ASIC	Application Specific Integrated Circuit
BW	Bandwidth
C	Capacitor
Class-D	Class-Digital
CMOS	Complementary Metal Oxide Substrate
CMRR	Common Mode Rejection Ratio
CT	Continuous-Time
D/A	Digital-to-Analog
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition
dB	Decibel
dBc	dB Referred to Carrier Level
dBFS	dB Full Scale
DC	Direct Current
DDS	Direct Digital Synthesis
DEM	Dynamic Element Matching
DfT	Design for Testability
DLL	Dynamic Linked Library
DMM	Digital Multimeter

List of Acronyms

DNL	Differential Non-Linearity
DR	Dynamic Range
DR	Dynamic Range
DSP	Digital Signal Processing
DT	Discrete-Time
DUT	Device Under Test
DWA	Data Weighted Averaging
ECL	Emitter Coupled Logic
ELD	Excess Loop Delay
ENOB	Effective Number of Bits
FIR	Finite Impulse Response
FM	Frequency Modulation
FoM	Figure of Merit
FPGA	Field Programmable Gate Array
GBW	Gain Bandwidth
GUI	Graphical User Interface
HDL	Hardware Description Language
HiFi	High Fidelity
Hz	Hertz
I²C	Inter-Integrated Circuit
IC	Integrated Circuit
IIR	Infinite Impulse Response
IIT	Impluse-Invariant Transformation
INL	Integrated Non-Linearity
IO	Input/Output
IoT	Internet of Things
IQ	In-Phase Quadrature
ISI	Intersymbol Interference
ITRS	International Technology Roadmap for Semiconductors
J/conv.-step	Joule per Conversion Step
J	Joule
JNR	Jitter Noise Reduction
L	Inductor
LC	Inductor Capacitor
LF	Loop Filter
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling

m	Meter
MatLab	Mathworks Matrix Laboratory
MIM	Metal Isolator Metal
MISO	Multiple Input Single Output
MSA	Maximum Stable Amplitude
MSB	Most Significant Bit
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OBG	Out of Band Gain
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PID	Proportional Integral Differential
PLL	Phase Locked Loop
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PVT	Process Voltage Temperature
R	Resistor
R₂R	R/2R
RC	Resistor Capacitor
RF	Radio Frequency
RMS	Root Mean Square
RMS	Root Mean Square
RZ	Return-to-Zero
s	Second
SC	Switched Capacitor
SCR	Switched Capacitor Resistor
$\Sigma\Delta$	Sigma-Delta
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNDR_p	Peak Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SNR_p	Peak Signal to Noise Ratio
SoCs	Systems on Chip
SPI	Serial Pheripheral Interface
SQNR	Signal to Quantization Noise Ratio

List of Acronyms

SQNR_p	Peak Signal to Quantization Noise Ratio
STF	Signal Transfer Function
TF	Transfer Function
THD	Total Harmonic Distortion
TIE	Time Interval Error
μC	Micro Controller
UDSM	Ultra Deep Sub-Micron
USB	Universal Serial Bus
V	Volt
VCO	Voltage Controlled Oscillator
W	Watt
XTAL	Crystal
ZOH	Zero Order Hold

List of Symbols

A	DC gain
a	Ratio of Values of Unit Resistor R and Resistor in Feedback Network
$A(s)$	Opamp Open Loop Gain in Laplace Domain
A_{boost}	Opamp DC Open Loop Gain Boost Factor
A_{dc}	Opamp DC Open Loop Gain
A_{OL,f_0}	Open Loop Gain of Opamp
A_0	Integrator Gain Scaling Parameter
a_n	Denominator Coefficients of DT Filter Transfer Function
A_{out}	DAC Output Signal
α_N	Continuous Time Loop Filter Coefficients
α_N^*	Discrete Time Loop Filter Coefficients
α_{ELD}	ELD Compensation Coefficient
B	Number of Quantizer Bits
b	Ratio of Values of Capacitor in Feedback Network and Unit Capacitor C
b_n	Numerator Coefficients of DT Filter Transfer Function
BW	Bandwidth
C	Unit Capacitor
C_f	Capacitance of Direct-Coupled RC Feed-in Path
$c_{ideal}(t)$	Ideal Square Wave Clock Signal
C_{par}	Parasitic Capacitor
C_x	Capacitance of Cross-Coupled RC Feed-in Path
C_c	Compensation Capacitor
C_h	Capacitor of RC -Opamp Assistance
$c_j(t)$	Square Wave Clock Signal with Jitter
C_Σ	Total Capacitance
$crect(x)$	Causal Rectangular Function

List of Symbols

$D(z)$	Digital Output Signal
D_{cm}	Common Mode Digital ADC Output Signal
D_{out}	Differential Digital ADC Output Signal
$\Delta A(t)$	Momentaneous Amplitude Noise
$\Delta t(t)$	Momentaneous Clock Jitter
$\Delta t[n]$	Time Interval Error
Δ	LSB Step Size
$\delta(t)$	Dirac Impulse
DR	Dynamic Range
$E(z)$	Quantization Error
$ENOB$	Effective Number of Bits
$F(z)$	FIR Filter Transfer Function
f_x^*	Shifted Frequency of First Zero in Laplace-Domain
f_{180}	Frequency where Transfer Function has 180 Phase Shift
f_0	Resonance Frequency
f_1	Parameter Defining Intrinsic Zero of High Order Integrator
f_2	Parameter Defining Intrinsic Zero of High Order Integrator
f_c	Corner Frequency
f_f	Frequency of Second Zero in Laplace-Domain
f_n	Nose Corner Frequency
f_s	Samling Frequency
f_T	Transit Frequency
f_x	Frequency of First Zero in Laplace-Domain
f_z	Frequency of Intrinsic Zero in Laplace-Domain
FoM	Figure of Merit
$G(s)$	Loop Gain Boost Factor
g_m	Transconductance
h	Number of Harmonic
$H(s)$	Continuous Time Filter Transfer Function
$H(z)$	Discrete Time Loop Filter Transfer Function
$H_{biquad}(s)$	Biquadratic Transfer Function
$H_{BP}(s)$	Bandpass Transfer Function
$H_{BP}(s)$	Bandpass Transfer Function
$H_{DAC}(z)$	DAC Transfer Function
$H_{ELD}(s)$	ELD Compensated Loop Filter Transfer Function
$H_{IQ}(s)$	Complex Transfer Function
$H_{JNR-DAC}(s)$	JNR-DAC Transfer Function

$H_{LP}(s)$	Lowpass Transfer Function
$H_{opt}(s)$	Loop Filter Transfer Function with Optimized Zeros
$H_p(s)$	Transfer Function of Resonator with Bypass
$H_{QI}(s)$	Complex Transfer Function
H_{X,f_0}	Resonator Peak Gain
$H_0(s)$	First Order Integrator Transfer Function
$H_1(z)$	Feed-in Transfer Function
$H_2(z)$	Feedback Transfer Function
H_∞	Out-of Band Noise Gain
$H_n(s)$	Transfer Function of n -th Resonator
$H_X(s)$	Transfer Function of Resonator
$I(s)$	Integrator Feed-In Current in Laplace Domain
$I_o(s)$	Opamp Output Current in Laplace Domain
k	Quantizer Gain
L_{cm}	Common Mode Loop Filter Transfer Function
L_{diff}	Differential Loop Filter Transfer Function
$\mathcal{L}(f)$	One-Sided Phase Noise
LSB	Least Significant Bit
$\mathcal{F}$	CT Fourier Transform Operator
$\mathcal{F}_d$	DT Fourier Transform Operator
MSA	Maximum Stable Amplitude
N	Order of Loop Filter
n	Sample Index
$N_a(f)$	PSD of Amplitude Modulated Noise Signal
$n_a(t)$	Amplitude Modulated Noise Signal
$N_j(f)$	PSD of Jitter Induced Noise Signal
$n_j(t)$	Jitter Induced Noise Signal
$n_j[n]$	Sampled Jitter Induced Noise Signal
N_Q	Quantization Noise Power
$NTF(z)$	Noise Transfer Function
OBG	Out-of-Band-Gain
OSR	Oversampling Ratio
P_{diss}	Power Dissipation
$\phi'(t)$	Momentaneous Excess Phase of Fundamental Tone
$\phi(t)$	Momentaneous Excess Phase of Fundamental Tone with Twice the Frequency

List of Symbols

$\phi[n]$	Sampled Momentaneous Excess Phase of Fundamental Tone with Twice the Frequency
PSD	Power Spectral Density
Q	Quality Factor
$Q(z)$	Quantizer Input Signal
$R_{ }$	Output Resistance of Feed-Forward Compensation Network
R_f	Resistance of Direct-Coupled RC Feed-in Path
R_{fb}	Feedback Resistance
R_{fi}	Feed-In Resistance
R_{neg}	Negative Resistor
R_x	Resistance of Cross-Coupled RC Feed-in Path
R_0	DC Resistance of Feedback Network
R_h	Resistor of RC -Opamp Assitance
R_i	Feed-in Resistor
s	Complex Argument of Laplace-Domain Functions
$S_{\phi'}(f)$	Double-Sided PSD of Momentaneous Excess Phase of Fundamental Tone
$S_{\phi}(f)$	Double-Sided PSD of Momentaneous Excess Phase of Fundamental Tone with Twice the Frequency
$SFDR$	Spurious Free Dynamic Range
σ_j	RMS Phase Jitter
$sinc$	Cardinal Sine Function
$SNDR$	Signal to Noise and Distortion Ratio
$SNDR_p$	Peak Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SNR_p	Peak Signal to Noise Ratio
$SQNR$	Signal to Quantization Noise Ratio
$STF(z)$	Signal Transfer Function
T_p	Period of RZ DAC
T_s	Sampling Clock Period
T_w	Pulse Width of RZ DAC
τ	Time Constant
THD	Total Harmonic Distortion
V_a	ADC Input Voltage
V_{bulkn}	Global Bulk Potential of Digital NMOS Transistors
V_{bulkp}	Global Bulk Potential of Digital PMOS Transistors
V_{cmp}	Comparator Reference Voltage

V_{dd}	Supply Voltage
V_{gmtest}	Programmable Reference Voltage
$V_{in,noise}(f)$	Integrator Input Referred Noise Spectral Density
$V_{in}(s)$	Input Voltage in Laplace Domain
$V_{noise}(f)$	Opamp Input Referred Noise Spectral Density
$V_{out}(s)$	Output Voltage in Laplace Domain
V_{ref}	Reference Voltage
V_{trip}	Inverter Trip Point Voltage
V_n	Virtual Ground Node
V_t	MOS Threshold Voltage
V_{DD}	Supply Voltage
$Y(z)$	z-Domain Representation of Data Sequence
$y_{even}(t)$	Even Indexed Samples of Non-Modulated NRZ Data Signal
$y_{ideal}(t)$	Non-Modulated NRZ Data Signal
$y_j(t)$	NRZ DAC Output Signal with Jitter
$y_{odd}(t)$	Odd Indexed Samples of Non-Modulated NRZ Data Signal
$y_{RZ}[n]$	RZ Data Sequence
$y[n]$	Data Sequence
z	Complex Argument of z-Domain Functions
Z_{dac}	DAC Output Impedance
$Z_{f0,k}$	Differential Impedance of Feedback Network
$Z_{LF}(s)$	Loop Filter V/I Transfer Function
$Z_{OP,f0}$	Differential Output Impedance of Opamp
Z_b	Impedance of Feedback Network

1 Introduction

1.1 Motivation

The continuing success in CMOS technology scaling enabled the integration of increasingly complex digital processing in consumer electronics over the past decades. One example where this trend becomes apparent is the evolution of mobile phones in recent years. Another example is the advent of the so called Internet of Things (IoT) which leads to more and more highly complex digital circuits being present in an increasing number of large volume consumer products.

The rapid growth in digital processing capacity led to the wide adoption of intelligent Digital Signal Processing (DSP) algorithms such as speech and image recognition and coding techniques that dramatically increased the communication bandwidth in consumer devices. An essential building block in these devices are data converters that provide interfaces for the digital algorithms to the physical world. Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) are required to interact with sensors and actuators and to access wired and wireless communication channels.

However, even the smartest and most powerful DSP algorithms fail, if the interfaces to the analog circuits introduce significant impairments to the analog signal such as aliasing, noise or distortion products. Therefore, with further evolution in DSP the requirements for the bandwidth, noise, and linearity of ADCs and DACs are also increasing continuously.

Besides the performance criteria that are relevant to the signal processing task, a small chip size and a low power consumption are also important requirements for ADCs and DACs. This becomes apparent in applications such as smartphones or wireless sensor networks in the IoT where long battery lifetime and low production cost are crucial.

1. Introduction

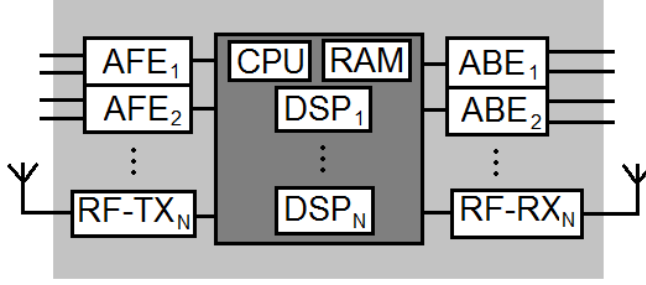


Figure 1.1.: Typical system-on-chip [1].

Mobile phone evolution requires to increase the hardware performance and complexity with every new product generation. Limited Printed Circuit Board (PCB) space, increasing bandwidth demand and high cost pressure forces the component suppliers to steadily increase the level of integration in Integrated Circuits (ICs). PCB circuits with numerous digital and analog ICs in early mobile phones have been replaced by a small number of highly complex Analog Mixed Signal (AMS) Systems on Chip (SoCs) (Fig. 1.1) that consist of DSP units, data converters and interfacing elements such as Analog Frontends (AFEs), Analog Backends (ABEs) and Radio Frequency (RF) transmitters and receivers. High production volume and large digital subsystems mandate implementing SoCs in leading edge Ultra Deep Sub-Micron (UDSM) CMOS processes to exploit technology scaling for minimized production cost.

However, analog building blocks now tend to become the limiting factor for cost minimization of SoCs, because the chip area of analog circuits scales much worse than for digital circuits due to the area dependence of analog non-idealities such as device mismatch and flicker noise. Since ADCs are among the most area occupying blocks in many state of the art SoCs, one goal of this work has been to find new concepts on architecture and circuit level to reduce the impact of these non-idealities in ADCs.

Implementing high performance analog building blocks becomes more and more challenging with technology scaling due to decreasing intrinsic transistor gain at smaller CMOS feature size and decreasing headroom for signal swing because according to the International Technology Roadmap for Semiconductors (ITRS) the supply voltage continues to decrease while

the transistor threshold voltages tend to remain constant [2, 3]. At smaller feature size, exploiting the improved timing resolution [4, 5] and the diminishing cost of digital gates for digitally assisted analog circuits [6] are ways to mitigate this problem. In this work, the approach to cope with weak analog properties of modern semiconductor processes has been to minimize the analog section using novel inverter-based analog circuit concepts combined with digital assistance.

In mobile applications it is important to minimize the power consumption of integrated circuits. Improved battery lifetime has become a key selling point in mobile electronic devices. An IC that consumes significantly more energy for the same task than the competition is very unlikely to become a successful product on the market. In many applications high performance ADCs are strong contributors to the total power consumption of SoCs.

1.2 Concept of Thesis

Among the various ADC concepts, Continuous-Time (CT)- $\Sigma\Delta$ -ADCs stand out with a very attractive compromise of power consumption, resolution and bandwidth as will be discussed in the next chapter.

Hence, this work focuses on improving CT- $\Sigma\Delta$ -ADCs in UDSM CMOS at MHz bandwidths on architectural and circuit level towards maximizing their area- and power-efficiency. Several novel concepts and techniques that concern many aspects of designing and implementing optimized CT- $\Sigma\Delta$ -ADCs have been derived and silicon-verified by the author during the course of this work.

The diversity of the proposed concepts and techniques mandates to deviate from the classical outline of most dissertation theses. Instead of describing the theory and the state of the art at the beginning of the thesis, these items have been grouped together with the individual contributions of this work into consecutive chapters per research topic such that continuous reading is possible without unnecessarily jumping between topics.

A more detailed outline of these topics will be given in the last section of the next chapter which covers the fundamentals of $\Sigma\Delta$ modulation.

2 Theory of $\Sigma\Delta$ -Modulation

Although known for more than 60 years [7, 8], $\Sigma\Delta$ -modulation has become popular with the advent of the compact disc in the 1980s. Its beauty lies in the fact that it naturally fits the weaknesses and strengths of modern integrated circuit fabrication: Without expensive production trimming, the precision of analog components is low in CMOS technology, while the capacity to implement complex digital circuits became very large in the past decades of successful feature size miniaturization. Fittingly, $\Sigma\Delta$ -modulation requires complex digital stages, but no precision analog stages to obtain highly precise Analog-to-Digital (A/D) and Digital-to-Analog (D/A) conversion.

The intention of this chapter is to give only a brief overview of the fundamentals of $\Sigma\Delta$ modulation. The interested reader is referred to [9–12] for a more comprehensive overview.

2.1 Oversampling and First Order Noise Shaping Using $\Sigma\Delta$ -Modulation

The basic idea behind $\Sigma\Delta$ -modulation is to suppress errors (Fig. 2.1) that are introduced by the inherently non-linear operation of a quantizer by means of linear feedback and filtering (Fig. 2.2). The ideal quantizer's staircase-shaped transfer characteristic is a result of the finite number of comparators with equidistant decision thresholds that are used to convert a continuous voltage into a limited number of fixed point bits in the digital domain. The voltage difference between two neighboring comparator thresholds corresponds to one Least Significant Bit (LSB) and determines the finite voltage resolution of the quantizer.

A mathematical model (Fig. 2.3) of the $\Sigma\Delta$ -modulator shown in Fig. 2.2 can be derived by replacing the quantizer by a gain factor k and an additive quantization error signal $E(z)$.

2. Theory of $\Sigma\Delta$ -Modulation

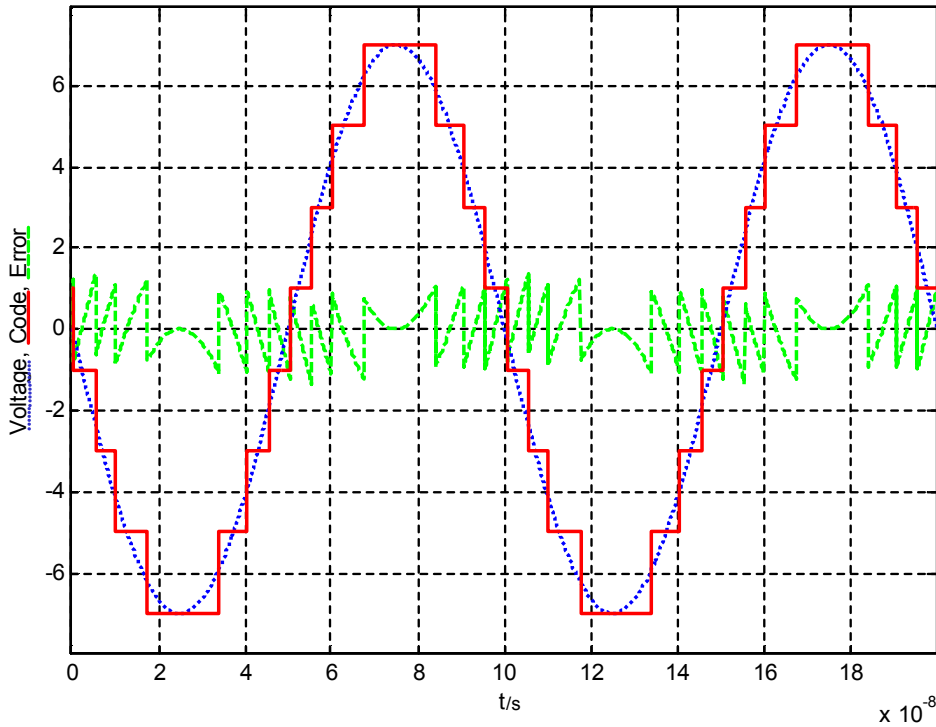


Figure 2.1.: Quantization of sinusoidal signal.

In an exact representation of the value discretization within the quantizer, the input signal of the quantizer and $E(z)$ are correlated. It is important to note that this system is still non-linear with the non-linearity of the quantizer being hidden in the error signal $E(z)$. In order to arrive at a linear approxima-

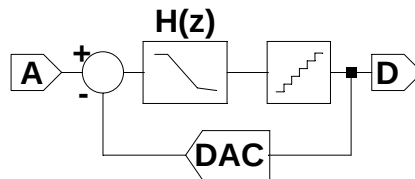


Figure 2.2.: $\Sigma\Delta$ -modulator.

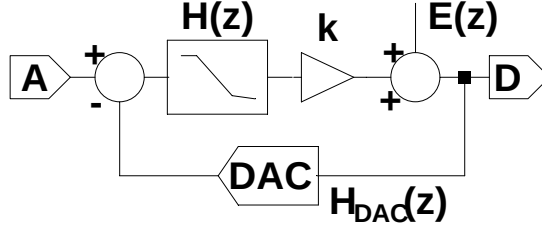


Figure 2.3.: Linearized $\Sigma\Delta$ -modulator.

tion of the system, the error signal $E(z)$ can be modeled by a random noise signal even though it is in reality a deterministic signal, i.e. it can be predicted at any time for a known input signal. This approximation yields good results for large and fast changing quantizer input signals that are typically present at modulator orders larger than two.

However, for lower modulator orders $E(z)$ may deviate significantly from a random signal. To put it another way, the larger the number of quantization levels and the more complex the input signal at the quantizer, the less correlated the error signal and the input signal become. A sufficiently weak correlation lets the error signal resemble a random signal with a total power N_Q that depends only on the size of the quantizer LSB step Δ and not on the input signal [13]:

$$N_Q = \frac{\Delta^2}{12} \quad (2.1.1)$$

For this reason the quantization error signal is usually called quantization noise. The spectrum of these uniformly distributed errors is white, i.e. the quantization noise is spread equally over the whole frequency range from $-f_s/2$ to $f_s/2$ at the quantizer output.

Note that (2.1.1) does not depend on the sampling frequency. Hence, the Power Spectral Density (PSD)

$$E(z) = N_Q/f_s \quad (2.1.2)$$

is inversely proportional to the sampling frequency f_s . This relation can be exploited to lower the quantization noise within the bandwidth of interest by means of so called oversampling, i.e. the input signal is sampled at an

2. Theory of $\Sigma\Delta$ -Modulation

Oversampling Ratio (OSR) times higher rate than required by Nyquist's theorem to avoid aliasing [14].

However, oversampling alone does not help much for increasing the resolution of a Nyquist-ADC due to a fundamental trade-off in real world ADCs: High resolution requires precise analog stages such as comparators and amplifiers, but precise stages are typically slow. Offset for example needs to be well controlled which results in large transistors and unless excessive power consumption is acceptable, large transistors result in low current densities in the transistors, which in turn means low speed.

Also the required digital signal processing demands a lot of power due to high sampling clock rates even though large portions of the Nyquist spectrum are almost empty and contain only quantization noise.

In addition to oversampling, a concept called noise shaping can be applied in order to shift quantization noise from the band of interest that contains the input signal into the portions outside that band. This not only significantly reduces the quantization noise within the band of interest but also improves the utilization of the out-of-band portions of the spectrum. In this way less out-of-band frequency range is required to distribute the total quantization noise power N_Q . This translates into a smaller sampling frequency f_s and alleviates the speed/resolution trade-off.

Noise shaping allows to obtain a much higher resolution improvement for a given OSR than pure oversampling. The most prominent implementation of such a noise shaper is the $\Sigma\Delta$ -modulator [7, 8].

For a discrete-time modulator (Fig. 2.2) with a DAC reference voltage of 1 V the DAC transfer function $H_{DAC}(z)$ becomes unity and for a maximum input signal amplitude that is limited to 1 V a unity quantizer gain k can be assumed [15]. With these assumptions, the so called Noise Transfer Function (NTF) and Signal Transfer Function (STF) become

$$NTF(z) = \frac{D(z)}{E(z)} = \frac{1}{1 + H(z)} \quad (2.1.3)$$

and

$$STF(z) = \frac{D(z)}{A(z)} = \frac{H(z)}{1 + H(z)}. \quad (2.1.4)$$

From (2.1.3) and (2.1.4) it becomes apparent that the input signal and the quantization noise are transferred differently to the output of the modulator.

Let the loop filter transfer function be a delaying discrete-time first order integrator with

$$H(z) = \frac{1}{z - 1}, \quad (2.1.5)$$

then the NTF becomes a first order high-pass transfer function

$$NTF(z) = 1 - z^{-1} \quad (2.1.6)$$

and the STF a unit delay

$$STF(z) = z^{-1}. \quad (2.1.7)$$

This means that the signal is unchanged while the quantization noise is shaped such that the noise within the bandwidth of interest is reduced significantly.

2.2 $\Sigma\Delta$ -ADC Performance Metrics

Nyquist-ADCs have a static transfer characteristic. Every output code is mapped time-invariantly to an input voltage range. This allows to characterize a Nyquist-ADC via its static transfer characteristic using parameters such as Integrated Non-Linearity (INL) or Differential Non-Linearity (DNL).

$\Sigma\Delta$ -modulators include memory elements such as integrators within a feedback loop. Thus, there is no static mapping of codes, because only the time average of the output codes corresponds to a certain input voltage range. Instead of a static transfer characteristic, they are characterized in the frequency domain via the spectral response to sinusoidal test signals. To quantify their spectra, the following specifications are used:

- **Signal to Noise Ratio (SNR).** The SNR specifies the ratio of the input signal power and the total noise power within the band of interest. If the SNR is plotted over the input signal power (Fig. 2.4) it typically rises to the so called Peak Signal to Noise Ratio (SNRp) and drops due to quantizer overload afterwards. SNR numbers are usually specified in Decibel (dB). An SNR that refers signal power to quantization noise only is often abbreviated with Signal to Quantization Noise Ratio (SQNR).

2. Theory of $\Sigma\Delta$ -Modulation

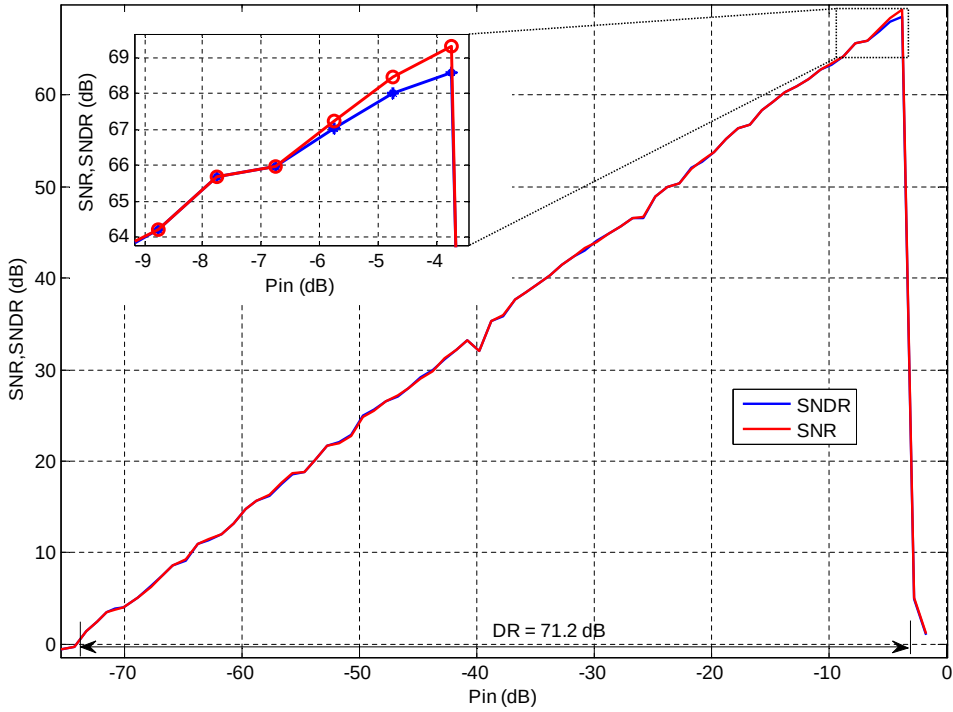


Figure 2.4.: Typical plot of the bitstream SNR and SNDR versus the level of an analog test signal at the ADC input.

- **Signal to Noise and Distortion Ratio (SNDR).** The SNDR specifies the ratio of the input signal power and the total power of both the noise floor and all distortion components. Hence, in real world circuits that are always non-linear to some extent, the Peak Signal to Noise and Distortion Ratio (SNDR_p) is always lower than the SNR_p.
- **Effective Number of Bits (ENOB).** The ENOB specifies the number of usable bits for a given SNDR_p. It is calculated by equating the SNDR_p with the expression for the SNR of an ideal quantizer and solving for the number of bits of the ideal quantizer:

$$ENOB = (SNDR_p - 1.76 \text{ dB}) / 6.02 \text{ dB} \quad (2.2.1)$$

- **Dynamic Range (DR).** The DR specifies the ratio of the maximum input signal power that can be applied to the ADC while the SNDR remains larger than 0 dB and the minimum detectable signal level, i.e. the smallest signal level where the SNDR is 0 dB.
- **Total Harmonic Distortion (THD).** The THD specifies the ratio of the power of all harmonics and the power of the fundamental tone in dB or as the ratio of the effective voltages in percent.
- **Spurious Free Dynamic Range (SFDR).** The SFDR specifies the ratio of the power of the fundamental tone and the power of the largest spurious spectral component in dB.
- **Figure of Merit (FoM).** The FoM specifies the power efficiency of the converter. There are various definitions for the FoM [16]. The most commonly used definition is the so called Walden FoM

$$FoM = \frac{P_{diss}}{2^{ENOB+1}BW}, \quad (2.2.2)$$

where P_{diss} is the total power dissipation and BW is the bandwidth of interest. However, the so called Schreier FoM allows a more fair comparison of ADCs that are resolution-limited by thermal noise, because it takes into account that for a given set of performance parameters halving the thermal noise voltage of a stage requires to quadruple its power dissipation. The Schreier FoM is expressed in dB:

$$FoM_2 = SNDR_p + 10\log_{10} \left(\frac{BW}{P_{diss}} \right) \quad (2.2.3)$$

2.3 $\Sigma\Delta$ -ADCs with High Order Noise Shaping

Higher order integration in the loop filter of $\Sigma\Delta$ -modulators yields higher order noise shaping [17]. The theoretical peak SNR of an ideal N -th order $\Sigma\Delta$ -modulator becomes

$$SNR_p = \frac{3\pi}{2} (2^B - 1)^2 (2N + 1) \left(\frac{OSR}{\pi} \right)^{2N+1} \quad (2.3.1)$$

where B is the number of bits in the quantizer [18, p. 34].

2. Theory of $\Sigma\Delta$ -Modulation

For loop filter orders N larger than 2 this theoretical SNR is only achievable with cascaded modulators, because single-loop modulators suffer from instability at such aggressive noise shaping. However, cascaded modulators are used mainly in the digital domain, because they require a very precise matching of the individual stages that is not available in the analog domain without expensive calibration measures [19–22]. For this reason most $\Sigma\Delta$ -ADCs rely on a single modulator loop.

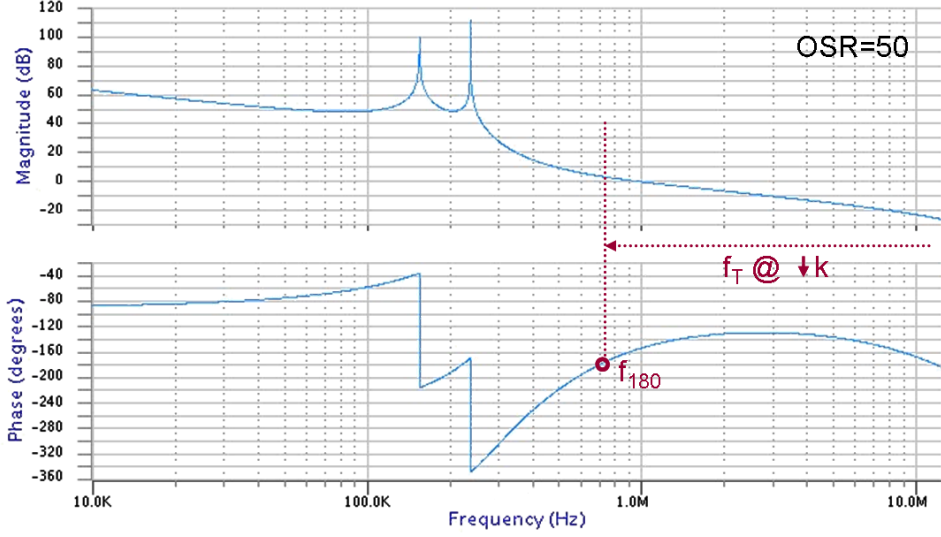


Figure 2.5.: Open loop transit frequency f_T versus quantizer gain k for a fifth order modulator.

Such modulators require compensation measures to obtain stability at orders larger than two [23]. In analogy to linear feedback systems, it must be ensured that there is sufficient phase margin at the transit frequency f_T of the linearized open loop modulator transfer function $kH(z)$ according to Fig. 2.3. This can be achieved by gradually reducing the slope of the loop filter transfer function

$$H(z) = \frac{z^{-1}(\alpha_{N-1}^* z^{-(N-1)} + \dots + \alpha_1^* z^{-1} + \alpha_0^*)}{(1 - z^{-1})^N} \quad (2.3.2)$$

until it approaches first order integration around the transit frequency (Fig. 2.5).

Finding optimum coefficients $\alpha_{N-1}^*, \dots, \alpha_0^*$ for the numerator polynomial in (2.3.2) can be challenging, because the quantizer gain k and therefore, also f_T is reduced with increasing quantizer input signal amplitude due to the compressive transfer characteristic of the fundamentally non-linear quantizer[24–26]¹. This makes the optimal coefficients depend on the input signal amplitude. As a reasonable compromise, the coefficients are determined for a so called Maximum Stable Amplitude (MSA) and the input signal amplitude is limited accordingly in order to guarantee a minimum phase margin taking non-idealities of the circuit implementation such as coefficient mismatch into account.

Due to compensation measures and limited MSA, the maximum achievable SNR for higher order modulators deteriorates significantly from (2.3.1). Unlike (2.3.1) there is no analytical expression for the maximum SNR of a stable high order single-loop modulator. Instead, Fig. 2.6 shows some empirical SNR limits of B -bit single-loop modulators of order N .

It is important to note that small signal stability analysis is not fully reliable when it comes to ensuring the stability of a $\Sigma\Delta$ -loop due to the strong non-linearity of the quantizer that causes a quasi-chaotic behavior of the system. Small signal stability analysis provides valuable insights, but it cannot replace extensive transient simulations to verify the stability of a modulator for various test signals.

There are numerical design tools such as Schreier's $\Sigma\Delta$ -Toolbox [27] that allow to find optimum loop filter transfer functions $H(z)$ for a given specification of quantizer bits B , loop filter order N , OSR and the Out of Band Gain (OBG) denoted by H_∞ , which determines the aggressiveness of the

¹ A quantizer with more than one bit must have a limited input voltage range in order to become a realizable electronic circuit. Any signal outside that range causes distortion due to clipping, which is also called quantizer overload. Clipping is a compressive phenomenon, because the output signal amplitude saturates with increasing input amplitude. For a single-bit quantizer the condition for overload is not immediately obvious. A single-bit quantizer can be modeled by an B -bit quantizer that is preceded by a gain stage with infinite gain. This forces all B output bits to become identical to the output of the single-bit quantizer. However, the infinite gain also means that the input referred voltage range of the single-bit quantizer becomes zero. Hence, a single-bit quantizer always operates in overload and therefore, its quantizer gain k always depends on the amplitude of the input signal.

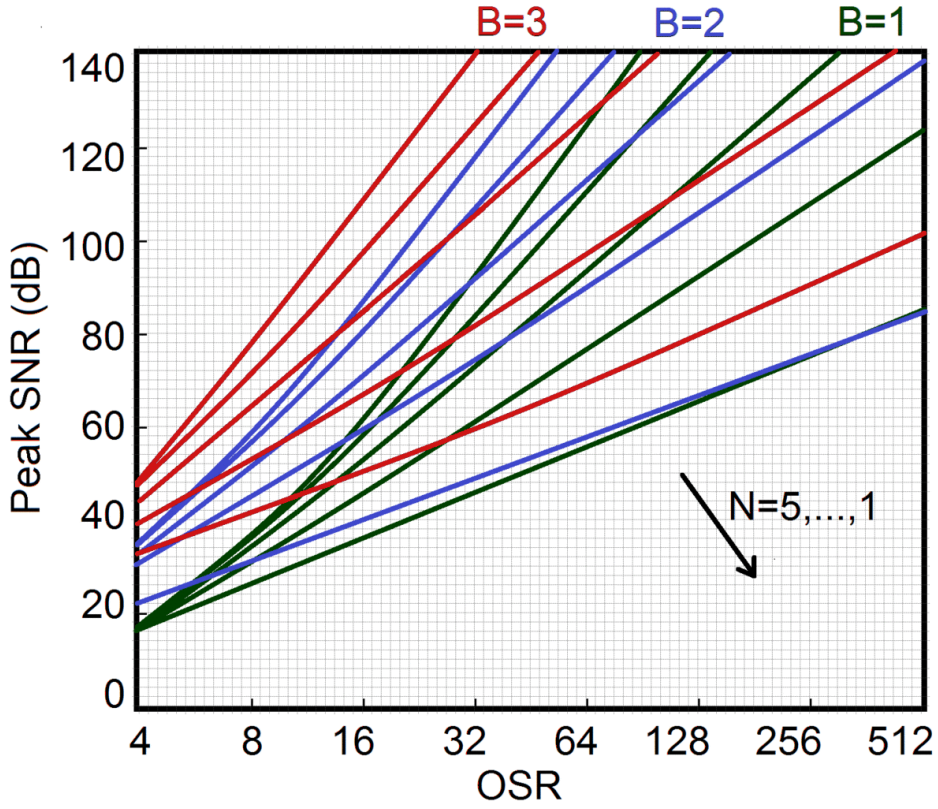


Figure 2.6.: Empirical SNR limit of B -bit single-loop $\Sigma\Delta$ -modulators of order N [10, pp. 112–113].

noise shaping, i.e. the higher H_∞ , the more of the quantization noise power concentrates at high frequency and the lower the MSA. These tools are also able to determine the maximum SNR and the MSA by time domain simulation.

2.4 Implementation of $\Sigma\Delta$ -ADCs

The implementation of the various building blocks of a $\Sigma\Delta$ -ADC will be briefly discussed in this section. For each of these building blocks a short

overview of the state of the art and directions to the relevant chapters of this thesis are given.

The loop filter $H(z)$ of a $\Sigma\Delta$ -modulator (Fig. 2.3) is responsible for the spectral shaping of the quantization noise; it must have high gain within the band of interest and low gain outside that band to obtain the desired suppression of the coarse quantizer's error signal. If the band of interest starts at DC, the modulator is of the low-pass type. In radio receivers, which is a major field of application for wideband $\Sigma\Delta$ -ADCs, it may be beneficial to directly digitize the radio frequency signal from the antenna or in case of heterodyne receiver architectures the intermediate frequency respectively. Such band-pass signals can be digitized with band-pass modulators that have a band of interest centered around the desired signal. However, for high performance receivers digitizing at low or zero intermediate frequency with low-pass ADCs is often a better choice². Therefore, this work focuses on low-pass modulators, although many of the discussions in this thesis can be applied to band-pass modulators as well.

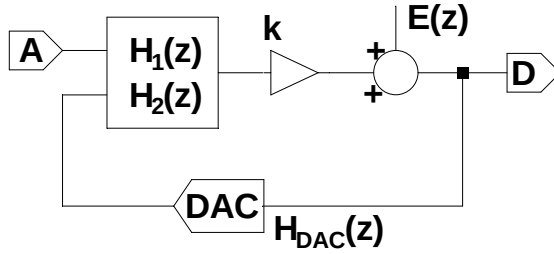


Figure 2.7.: $\Sigma\Delta$ -modulator with independent STF and NTF.

From (2.1.3) and (2.1.4) it becomes apparent that the STF cannot be chosen independently of the NTF. In order to reduce power consumption and circuit complexity it may be desirable to implement a low-pass or band-pass STF instead of using a dedicated preceding low-pass or band-pass filter in order

² This of course depends strongly on the radio standard. For example, in applications such as car radio, choosing between band-pass and low-pass digitization is mostly a trade-off between linearity and image rejection. In contrast to linearity, image rejection can be robustly improved by digital post processing which makes low-pass digitization the natural choice.

2. Theory of $\Sigma\Delta$ -Modulation

to apply analog filtering within the signal processing chain³. This can be achieved using a filter that has two separate inputs, a feed-in input $H_1(z)$ and a feedback input $H_2(z)$ (Fig. 2.7).

Both the single-input as well as the dual-input loop filter can be implemented in many different ways, e.g. as

- switched capacitor [28–30],
- gm-C [31–33],
- LC [34, 35],
- passive RC [36–38],
- active RC filter [39–43]
- or combinations of these structures [22, 44–48].

For high-resolution, broadband, low-power, low-pass $\Sigma\Delta$ -ADCs continuous-time active RC loop filters are a very good choice, because they offer high linearity and high bandwidth even at low supply voltage. Moreover, they can be implemented with much lower speed opamps than comparable switched capacitor loop filters that require fast settling times in order to complete the charge transfer within half a sampling clock period. As a further benefit, continuous-time loop filters offer inherent anti-alias filtering, because high frequency alias signals are strongly suppressed by the loop filter before they reach the quantizer [49, 50]. For this reason, this work focuses on continuous-time $\Sigma\Delta$ -ADCs with active-RC loop filter implementations.

In order to obtain the desired NTF, the coefficients $\alpha_{N-1}^*, \dots, \alpha_0^*$ of the discrete-time loop filter transfer function (2.3.2) need to be mapped onto the coefficients $\alpha_{N-1}, \dots, \alpha_0$ of the continuous-time transfer function

$$H(s) = \frac{\alpha_{N-1}s^{N-1} + \dots + \alpha_1s + \alpha_0}{s^N}. \quad (2.4.1)$$

Similar to the discrete-time transfer function (2.3.2), this filter approximates Nth order integration at low frequency and first order integration at

³ Such an analog filter could be used as a coarse channel filter in radio receivers for example.

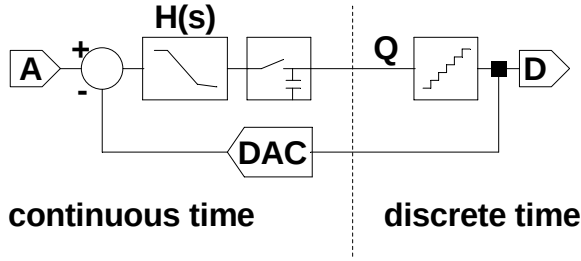


Figure 2.8.: CT- $\Sigma\Delta$ -modulator.

near loop transit frequencies, i.e. all poles except one are canceled by $N-1$ zeros that must be located sufficiently far below $f_s/2$ to obtain a stable loop.

The obvious condition for this mapping is that a Dirac impulse that enters the DAC in Fig. 2.8 must result in the same impulse response after the sampler as for the corresponding discrete-time loop filter $H(z)$, i.e. the condition

$$Q(z)/D(z) = H(z) \quad (2.4.2)$$

must hold. For Non-Return-to-Zero (NRZ) DAC pulses that are either undelayed or delayed by integer multiples of the sample period this mapping is equivalent to the so called Impulse-Invariant Transformation (IIT)⁴. There are numerical tools such as Mathworks Matrix Laboratory (MatLab) with the `d2cm()` function that can perform this transformation.

For delayed rectangular pulses where the delay and the pulse length are rational fractions of the sampling period, the IIT can be applied in a multi-rate approach together with an upsampling of the impulse response such that both the delay and the pulse length become integer multiples of the sampling period [39].

DAC pulses that are shorter than the sampling period allow to compensate for so called Excess Loop Delay (ELD) that is caused by non-idealities such as finite opamp Gain Bandwidth (GBW) [11, pp. 128–134] or digital propagation delay in front of the feedback DAC. Apart from these parasitic root

⁴ For non-rectangular pulses other transformations need to be applied [51, 52].

2. Theory of $\Sigma\Delta$ -Modulation

causes, ELD is also often inserted deliberately by delayed clocks to minimize distortion of the DAC output pulses due to quantizer metastability [53].

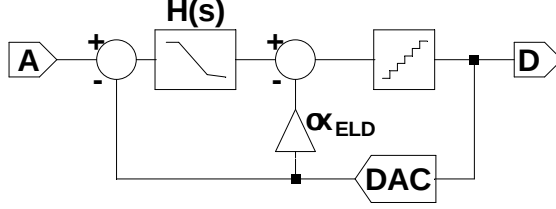


Figure 2.9.: $\Sigma\Delta$ -modulator with ELD compensation.

Besides ELD also the causality and the shape of the (rectangular) feedback DAC pulse imply a delay and a (*sinc*) low-pass filtering that have an impact on the open loop phase margin in a continuous-time implementation. Insufficient phase margin requires to compensate the remaining first order integration at high frequency by an additional zero that is usually implemented by a feedback coefficient α_{ELD} that bypasses the loop filter with a direct loop around the quantizer (Fig. 2.9) [39, 54, 55]. With no impact on the NTF and only minor impact on the STF, this so called ELD compensation can be merged into the loop filter [41] resulting in a loop filter transfer function

$$H_{ELD}(s) = H(s) + \alpha_{ELD} \quad (2.4.3)$$

with both a numerator and denominator polynomial of order N^5 .

Active RC loop filters are traditionally implemented as state variable filters (Fig. 2.10) that consist of a chain of integrators and a feedback and/or a feed-forward compensation network. This filter architecture requires one opamp per loop filter order⁶. In state of the art ADCs with MHz bandwidths, these opamps typically contribute significantly to both the power consumption and

⁵ For NRZ pulse delays that extend beyond half a sampling clock cycle the order of the loop filter becomes larger than N and additional compensation efforts are required [56, 57].

⁶ In some publications an additional opamp is used to sum up the feed-forward coefficients and to drive the capacitive input impedance of the quantizer [58].

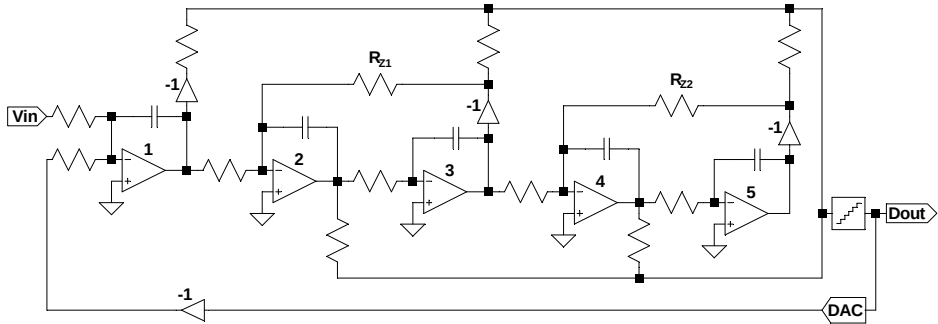


Figure 2.10.: Single-ended fifth order modulator with optimized NTF zeros.

the chip area. For example, the opamps in [41] require 41 % of the total power consumption and 30 % of the total area on the chip. Therefore, one goal of this work has been to derive and analyze novel loop filter architectures with reduced number of opamps for increased power- and area-efficiency.

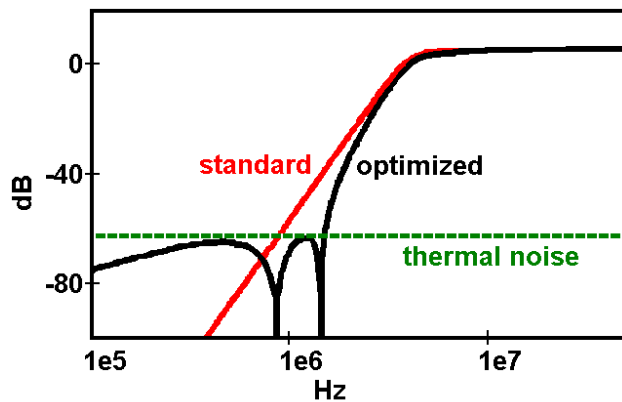


Figure 2.11.: Standard versus zero-optimized NTF of a fifth order modulator.

$\Sigma\Delta$ -ADCs are typically designed with medium to low OSR to achieve MHz bandwidths at technically feasible and in terms of power consumption reasonable sampling frequencies. Medium to low OSR requires to spread the NTF zeros optimally with respect to the input referred thermal noise floor of

2. Theory of $\Sigma\Delta$ -Modulation

the ADC over the band of interest (Fig. 2.11). Shifting NTF zeros from DC to a higher frequency requires using resonators instead of integrators in the loop filter.

The traditional resonator configuration consists of two opamps in a feedback configuration (e.g. opamps 2 and 3 in Fig. 2.10). Using a single-opamp resonator instead allows to reduce the number of opamps. In Chapter 3 this concept along with a novel class of single-opamp resonators is discussed in more detail and in Chapter 4 the concept is extended such that it enables implementing high order loop filters with a reduced number of opamps.

According to (2.3.1) and Fig. 2.6, a higher resolution of the quantizer in Fig. 2.2 yields a higher achievable SNR. On the other hand, single-bit quantization also has an important advantage: it is intrinsically linear. This is because component mismatch results in offset in single-bit DACs and single-bit quantizers, whereas it results in non-linearity in multi-bit DACs and multi-bit quantizers.

At the quantizer, a moderate non-linearity can be tolerated, because any distortion products are shaped by the NTF in the same way as the quantization noise. As a rule of thumb, quantizer non-linearity is not a problem as long as the non-linearity is weak enough so that no missing codes, no non-monotonicity, or a significant reduction of the input voltage range occurs at the quantizer. As the number of quantization bits is increased and the supply voltage is reduced, the more stringent the offset requirements become for the individual comparators within the quantizer.

This translates into large transistors that increase the power consumption of the quantizer and the capacitive load of the loop filter. Comparator offset calibration [39] and/or passive integration in front of the quantizer [47] can be employed to mitigate excessive power consumption of the quantizer and the loop filter.

However, in high bandwidth ADCs, the multi-bit quantizer typically is still the largest contributor to the total power dissipation. Moreover, large transistors and high circuit complexity results in large chip area that is occupied by multi-bit quantization.

On the contrary, single-bit modulators are insensitive to comparator offset, which translates into significantly lower power consumption and chip area of the quantizer due to smaller transistors and lower circuit complexity. In order to obtain the same SNR of the ADC, the lower quantizer resolution needs to be compensated by a higher OSR. For example, according to Fig. 2.6 an

80 dB-SNR third order modulator requires an OSR that is three times higher using a single-bit instead of a three bit quantizer.

The three times higher sampling clock frequency f_s partly antagonizes the lower power consumption not only in the quantizer itself, but also in the feedback DAC and the subsequent decimation filter. Fortunately, at the same time, the input bus width at the DAC and the decimation filter are reduced by a factor of three, which mitigates the excess power consumption due to the higher f_s . Moreover, as an added benefit the anti-alias filtering is improved, because at higher frequencies the bands around multiples of f_s are suppressed more effectively by the loop filter before the sampling operation of the clocked quantizer folds them into the band of interest.

Hence, unless ultra high sampling frequencies are required that cannot be implemented conveniently in a given semiconductor technology, single-bit quantization is a very attractive choice for high performance $\Sigma\Delta$ -ADCs that fits nicely to the constantly reducing analog precision and improving timing resolution in state of the art UDSM CMOS semiconductor technologies.

And yet in recent years the vast majority of these ADCs has relied on multi-bit quantization, because its lower quantization noise power relaxes significantly both the loop filter linearity requirements [59] and the very high sensitivity to sampling clock jitter of the CT- $\Sigma\Delta$ -ADC [53].

Therefore, besides novel loop filter concepts this work focuses on single-bit quantization, the analysis of sampling clock jitter folding mechanisms (Chapter 5) and ways to suppress sampling clock jitter-induced noise (Chapter 6).

In Chapter 7, a 350 nm CMOS implementation of a CT- $\Sigma\Delta$ -ADC that served as a test vehicle for novel mostly analog circuit concepts is discussed. In Chapter 8 a second testchip in 65 nm CMOS that uses further novel techniques such as integrator loss compensation and pseudo-differential quantization to minimize the active analog section in order to enable a mostly digital implementation of CT- $\Sigma\Delta$ -ADCs is presented.

3 RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

In recent publications techniques that allow to shrink the chipsize of the feedback DAC and the quantizer within wideband CT- $\Sigma\Delta$ -ADCs have been employed [39, 41, 60, 61]. This leaves the loop filter as the largest block in many designs. Also from a power dissipation point-of-view, the loop filter is often the largest contributor unless very high sample rates are used where the power dissipation of the quantizer typically becomes dominant.

In conventional active-RC loop filter topologies the total number of opamps equals at least the order of the noise shaping. Within the loop filter these opamps dominate both chip area and power dissipation. Therefore, in this chapter the fundamentals of loop filter implementation with resonators are discussed and a single-opamp resonator concept that allows to reduce the number of opamps within such loop filters for improved power- and area-efficiency is proposed.

3.1 Zero-Optimized Loop Filter

The generic loop filter transfer function (2.4.1) for an N -th order modulator has N poles at the origin of the s -plane that translate into N DC zeros in the NTF due to the quantized discrete-time feedback around the loop filter. These DC zeros provide N -th order high-pass shaping of the quantization noise at low frequency. However, for maximum SNR it is necessary to optimally spread these NTF zeros across the band of interest (Fig. 2.11). Optimum frequencies of NTF zeros for modulator orders of up to eight can be found in [10, pp. 107–111].

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

Poles on the imaginary axis of the s -plane are required to realize NTF zeros. These poles must be conjugate complex, i.e. they must be located symmetrically on the imaginary axis, because otherwise the result would be a complex loop filter transfer function, which requires In-Phase Quadrature (IQ) signal processing and often prohibitively precise matching of analog components [40].

Always a pair of two poles must be shifted symmetrically from the origin of the s -plane to the same positive and negative frequency on the imaginary axis in the s -plane. The resulting conjugate imaginary pole-pair represents a resonator. Such a resonator can be described with the biquadratic transfer function

$$H_{biquad,k}(s) = \frac{\alpha_{2,k}s^2 + \alpha_{1,k}s + 1}{s^2 + (2\pi f_{0,k})^2} \quad (3.1.1)$$

where $f_{0,k}$ is the resonance frequency.

The loop filter transfer function of a modulator with optimized NTF zeros can be synthesized by a cascade of those biquad blocks [62]¹:

$$H_{opt}(s) = \frac{\alpha_0}{s} \prod_{k=1}^{(N-1)/2} H_{biquad,k}(s) \quad (3.1.2)$$

For a low-pass modulator, it is usually desirable to keep one of the poles at the origin to have high quantization noise suppression also at very low frequencies. For this reason and without sacrificing generality only odd loop filter orders are considered here.²

3.2 Loop Filter Resonators

The traditional approach in realizing (3.1.2) is to expand its numerator product and interpret the resulting polynomial coefficients as feed-forward or feedback coefficients of a state variable filter:

¹ This is because any N -th order polynomial with real coefficients can be expressed as a product of first and second order polynomials with real coefficients.

² For even orders N' substitute $\alpha_0 = s\alpha'_0$ and $N = N' + 1$ in (3.1.2).

$$H_{opt}(s) = \frac{\alpha_{N-1}s^{N-1} + \dots + \alpha_1s + \alpha_0}{s \prod_{k=1}^{(N-1)/2} (s^2 + (2\pi f_{0,k})^2)} \quad (3.2.1)$$

An example of such a filter with feed-forward coefficients is depicted in Fig. 2.10. There are two resonant structures in this example that consist of local feedback loops around integrators 2/3 via R_{Z1} and around integrators 4/5 via R_{Z2} .

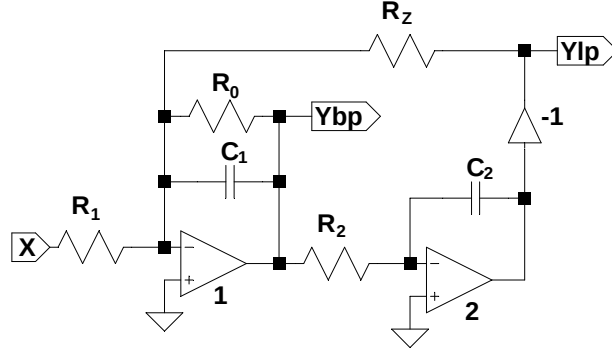


Figure 3.1.: Single-ended Tow-Thomas biquad resonator.

These structures can be identified as Tow-Thomas biquad resonators according to Fig. 3.1.³ The additional damping resistor R_0 determines the quality factor of the filter. If it is omitted the Tow-Thomas biquad becomes a perfect resonator. In this undamped biquad filter, feedback via R_Z turns a chain of two integrators into a resonator and moves two poles from the origin to

$$s = \pm j2\pi f_0. \quad (3.2.2)$$

³ The inverting unity gain stage is necessary only due to the simplified single-ended representation. The real circuits are usually differential, where inverted signals of all nodes are available without extra hardware.

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

The Tow-Thomas filter has two outputs, a band-pass

$$H_{BP}(s) = \frac{Y_{BP}(s)}{X(s)} = -\frac{R_Z}{R_1} \frac{sR_2C_2}{s^2/(2\pi f_0)^2 + 1} \quad (3.2.3)$$

and a low-pass terminal

$$H_{LP}(s) = \frac{Y_{LP}(s)}{X(s)} = \frac{R_Z}{R_1} \frac{1}{s^2/(2\pi f_0)^2 + 1} \quad (3.2.4)$$

with the resonance frequency

$$f_0 = \frac{1}{2\pi\sqrt{R_Z R_2 C_1 C_2}}. \quad (3.2.5)$$

Above the resonance frequency $H_{BP}(s)$ and $H_{LP}(s)$ approximate single and double integration (Fig. 3.2). For this reason such a resonator structure is also called a second order integrator in some publications⁴. While the phase is correct for $f > f_0$, the magnitude deviation is more than 1 dB for $f < 3f_0$. Hence, the impact of the zero optimization on the loop stability of the modulator is not significant if the transit frequency of the open modulator loop is always above $3f_0$ of the resonator with the highest f_0 .

Unless very low OSR is required, this allows to apply the zero optimization to (2.4.1) without adjusting the numerator coefficients; it even allows to make the zeros programmable by switching the value of R_Z in order to dynamically trade resolution versus bandwidth of the ADC.

In the feed-forward compensated state variable loop filter topology in Fig. 2.10 both outputs Y_{BP} and Y_{LP} are used. Accordingly, in a feedback compensated loop filter two virtual grounds to inject currents with independent transfer functions are required. Since a single-opamp resonator cannot have more than one low impedance output and one virtual ground it is impossible to directly substitute the two-opamp Tow-Thomas resonator by a single-opamp resonator [63].

⁴ In general, N -th order filters that approximate N -th order integration within the high frequency portion of the Bode-plot are called N -th order integrators in these publications.

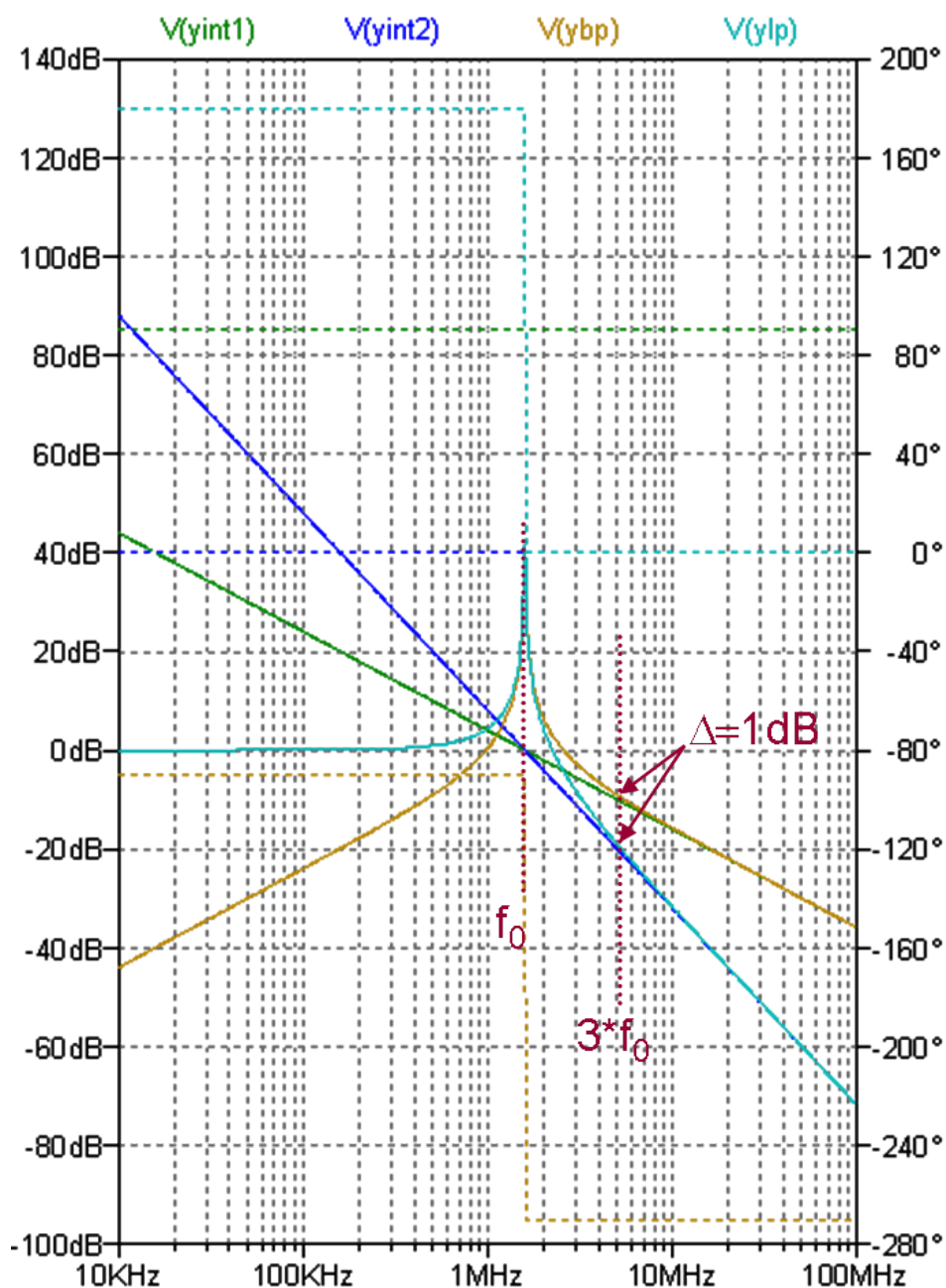


Figure 3.2.: Bode-plot of Tow-Thomas resonator.

However, a single-opamp resonator with a second order numerator transfer function (3.1.1) can be used to synthesize the total transfer function by cascading according to (3.1.2). In this way, a feed-forward compensation network, a dedicated summation opamp and additional feedback compensation DACs that would be required in standard loop filter topologies can be omitted for reduced power consumption.

3.3 Twin-T Resonator

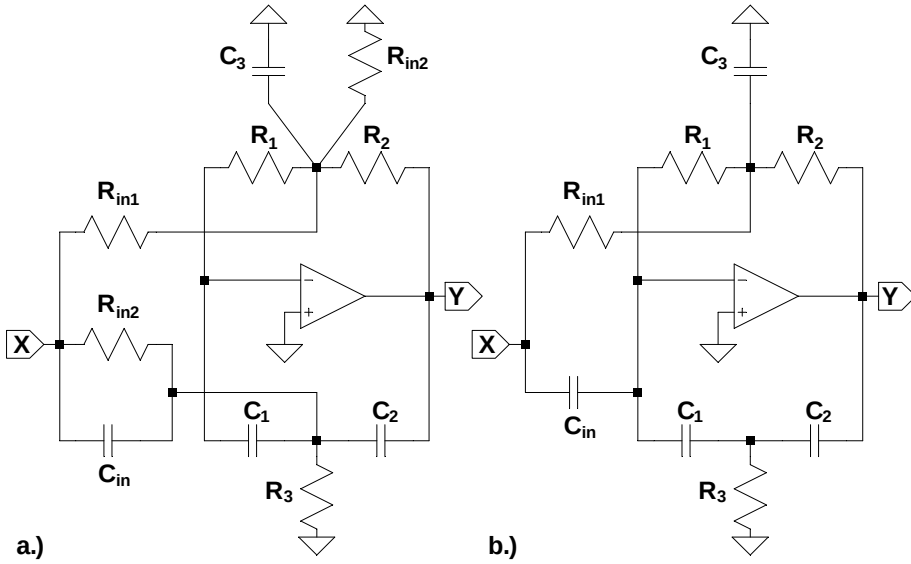


Figure 3.3.: (a) "Versatile Resonator" [64] (b) "Simplified Versatile Resonator" [65].

CT- $\Sigma\Delta$ -ADCs with Twin-T [66] based Single-opamp resonators [67] have been proposed in [64, 65], where the standard Twin-T resonator has been modified (Fig. 3.3) to obtain an arbitrary second order polynomial in the numerator of its transfer function (3.1.1), which allows to implement a modulator with reduced number of opamps.

However, there are some issues with these resonators:

- **Sensitivity to parasitic coupling between opamp input and output:** Parasitic capacitance between these nodes represents a path par-

allel to the Twin-T notch filter in the feedback of the opamps in Fig. 3.3 and consequently limits the quality factor of the resonators.

- **Increased distortion:** Passgate switches for RC-calibration must be placed at non-silent nodes in Fig. 3.3.
- **Large area:** The total capacitance becomes large for low bandwidth modulators.
- **Modification of Twin-T degrades matching:** The quality factor of the resonance is sensitive to component mismatch within the Twin-T network. Modification of the Twin-T network in Fig. 3.3 results in large non-integer component ratios and consequently reduces their matching.
- **Increased power consumption in preceding stage due to loading:** The load for preceding stages in Fig. 3.3 is partly capacitive and the input signal is not injected at the virtual ground, which results in significant coupling between the opamp output and the preceding stage.
- **Thermal noise gain:** Neglecting capacitors in Fig. 3.3 at low frequencies reveals that the thermal noise of resistor R_1 is amplified in the same way as the input noise of the opamp. Thus, either the noise of the opamp or the impedance level of the filter has to be reduced to compensate the amplified noise of R_1 at the cost of increased power dissipation.

In the following sections, a novel cross-coupled differential single-opamp resonator and methods for obtaining arbitrary second order numerator polynomials are proposed. Compared to modified Twin-T resonators, the new resonator is

- **more robust to mismatch** due to integer component ratios,
- **more robust to parasitic coupling** due to an inherent capacitor in parallel to the parasitic capacitor,
- **more compact** due to reduced total capacitance,
- **more linear** due to calibration switches at silent nodes,

- **and more power-efficient** due to reduced thermal noise and reduced loading of both the opamp itself and the preceding stage.

3.4 Cross-Coupled Single-Opamp Resonator

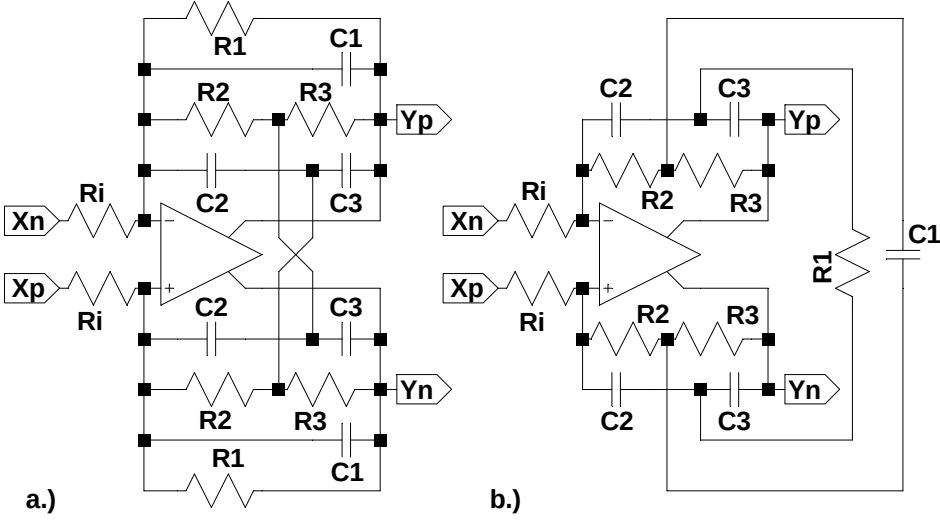


Figure 3.4.: (a) Cross-coupled resonator (b) Differential Twin-T resonator.

A novel class of cross-coupled single-opamp resonators (Fig. 3.4a) that has been first proposed by the author in [68] and applied in [69, 70] allows to overcome the issues of the modified Twin-T resonators. Originally, these resonators were derived from complex two-stage polyphase notch filters according to Appendix A.1.

Mapping such a network from complex to real with opposite phase rotation in each stage after some simplifications yields the notch filter network comprising resistors R_1 - R_3 and capacitors C_1 - C_3 in Fig. 3.4a [71]. It can be shown that one of the variants of this resonator, the RCX configuration, can also be derived from the Twin-T-resonator by T-to-II transformation as shown in Appendix A.2.

3.4. Cross-Coupled Single-Opamp Resonator

If this notch filter is placed in the feedback loop of an ideal opamp, a perfect resonance at the frequency

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{\frac{1}{R_1 R_2} + \frac{1}{R_1 R_3} + \frac{1}{R_2 R_3}}{C_1 C_2 + C_1 C_3 + C_2 C_3}} \quad (3.4.1)$$

is obtained under the condition:

$$\frac{C_2}{R_3} + \frac{C_3}{R_2} = \frac{C_1}{R_3} + \frac{C_1}{R_2} + \frac{C_2}{R_1} + \frac{C_3}{R_1} \quad (3.4.2)$$

With the DC resistance of the feedback network

$$R_0 = \frac{R_1(R_2 + R_3)}{R_1 + R_2 + R_3} \quad (3.4.3)$$

the transfer function becomes

$$H_X(s) = \frac{R_0}{R_i} \frac{s / (2\pi f_Z) + 1}{s^2 / (2\pi f_0)^2 + 1} \quad (3.4.4)$$

with a real zero at:

$$f_Z = \frac{R_2 + R_3}{2\pi(C_2 + C_3)R_2 R_3} \quad (3.4.5)$$

Since (3.4.2) leaves degrees of freedom in choosing the component values, the network can be optimized for low number of components, reasonable component values, low load on the preceding stage and low load on the opamp by the differential impedance of the feedback network itself, which is at the resonance frequency

$$Z_{f_0,k} = \frac{C_2 + C_3 - \frac{j}{2\pi f_0} \left(\frac{1}{R_2} + \frac{1}{R_3} \right)}{\frac{C_3}{R_2} + \frac{C_2}{R_3} + \frac{2C_k}{R_k}}. \quad (3.4.6)$$

The parameter k in (3.4.6) is 2 or 3 depending on whether the impedance is observed from the left side where R_2 and C_2 are located or from the right side where R_3 and C_3 are located when looking into the cross-coupled feedback network in Fig. 3.4a.

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

In case of a real opamp, the peak gain at the resonance frequency H_{X,f_0} is determined by the open loop gain A_{OL,f_0} , the differential output impedance Z_{OP,f_0} of the opamp at this frequency and $Z_{f_0,k}$.

Since there is no feedback at f_0 , $Z_{f_0,2}$ forms a voltage divider with R_i ⁵ at the input of the opamp and $Z_{f_0,3}$ forms a voltage divider with Z_{OP,f_0} ⁶ at the output of the opamp. The total peak gain becomes

$$H_{X,f_0} = A_{OL,f_0} \frac{Z_{f_0,2}}{2R_i + Z_{f_0,2}} \frac{Z_{f_0,3}}{Z_{OP,f_0} + Z_{f_0,3}}. \quad (3.4.7)$$

Hence, minimum requirements for the GBW, the DC gain and the output impedance of the opamp are imposed by the required peak gain.

The structure of the notch network also influences the peak gain: Due to the symmetry of the notch network in Fig. 3.4a, it is always possible to exchange R_2 with R_3 and C_2 with C_3 without violating (3.4.2) or altering (3.4.4). In contrast to these equations, (3.4.7) changes unless $2R_i \neq Z_{OP,f_0}$ if these components are swapped: For example, if $2R_i > Z_{OP,f_0}$ then $C_2/R_2 < C_3/R_3$ results in a higher peak gain than $C_2/R_2 > C_3/R_3$.

Moreover, the peak gain can be increased by adjusting R_1 to a slightly higher value, because similar to the case of an integrator, limited opamp DC-gain is equivalent to a resistor in parallel to the feedback network. Hence, the perfect resonance can be restored if the adjusted R_1 in parallel to the equivalent resistor equals the desired R_1 . However, this technique yields good results only, if the dominant pole of the opamp is well above the resonance frequency f_0 and if the opamp DC gain is sufficiently well defined.

The peak gain can be further degraded by non-perfect notch filtering due to mismatch of R_1 and R_3 or due to mismatch of C_1 and C_3 ⁷. This mandates optimizing the network for a small number of components with small integer component ratios.

⁵ R_i may also represent the source impedance of a more complex feed-in network.

⁶ Any load impedance that the integrator has to drive can be merged into Z_{OP,f_0} .

⁷ The same limitations for the peak gain apply to the Twin-T resonator.

Table 3.1.: Normalized Solutions for the Cross-Coupled Notch/Resonator

Type	R_1	R_2	R_3	C_1	C_2	C_3	C_Σ	$\frac{f_Z}{f_0}$	$\frac{Z_{f_0,2}}{R_i}$	$\frac{Z_{f_0,3}}{R_i}$
RCXX	2	1	1	$\frac{1}{2}$	1	1	5	1	$\frac{1-j}{2}$	$\frac{1-j}{2}$
CXX	∞	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{2}{\sqrt{3}}$	$\frac{2}{\sqrt{3}}$	$\frac{2}{\sqrt{3}}$	$4\sqrt{3}$	$\sqrt{3}$	$\frac{1-j\sqrt{3}}{4}$	$\frac{1-j\sqrt{3}}{4}$
RXX	$\frac{3}{2}$	$\frac{3}{2}$	$\frac{3}{2}$	0	$\frac{2}{\sqrt{3}}$	$\frac{2}{\sqrt{3}}$	$\frac{8}{\sqrt{3}}$	$\frac{1}{\sqrt{3}}$	$\frac{3-j\sqrt{3}}{4}$	$\frac{3-j\sqrt{3}}{4}$
CYY	∞	$\frac{1}{2}$	$\frac{1}{2}$	$\sqrt{2}$	$2\sqrt{2}$	0	$6\sqrt{2}$	$\sqrt{2}$	$\frac{1-j\sqrt{2}}{4}$	$\frac{1-j\sqrt{2}}{2}$
RYY	1	$\frac{1}{2}$	∞	0	$\sqrt{2}$	$\sqrt{2}$	$4\sqrt{2}$	$\frac{1}{\sqrt{2}}$	$\frac{2-j\sqrt{2}}{2}$	$\frac{2-j\sqrt{2}}{6}$
Chh	∞	$\frac{1}{2}$	$\frac{1}{2}$	$\sqrt{2}$	0	$2\sqrt{2}$	$6\sqrt{2}$	$\sqrt{2}$	$\frac{1-j\sqrt{2}}{2}$	$\frac{1-j\sqrt{2}}{4}$
Rhh	1	∞	$\frac{1}{2}$	0	$\sqrt{2}$	$\sqrt{2}$	$4\sqrt{2}$	$\frac{1}{\sqrt{2}}$	$\frac{2-j\sqrt{2}}{6}$	$\frac{2-j\sqrt{2}}{2}$
RCX	1	∞	$\frac{1}{2}$	1	2	0	6	1	$\frac{1-j}{2}$	$\frac{1-j}{2}$
TwinT	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	2	2	2	10	1	$\frac{1-j}{2}$	$\frac{1-j}{2}$

In Tab. 3.1 special solutions are listed, which have been normalized to unity DC gain and to the same resonance frequency

$$f_0 = \frac{1}{2\pi R_i C}. \quad (3.4.8)$$

The component values in Tab. 3.1 are given as multiples of unit capacitor C and input resistor R_i . These solutions are optimized for good matching and low number of components. Their names are derived from the structure of the feedback network. For example, RCXX means that R , C and two cross-coupled RC structures are connected in parallel. For comparison, the component values of the standard differential Twin-T resonator depicted in Fig. 3.4b with identical transfer function (3.4.4) have been included.

With unity DC gain, all variants have the same level of thermal noise close to DC, because at DC only the gain-defining resistors R_i and R_0 contribute thermal noise. Other resistors start to contribute as f_Z is approached. In general, it is therefore beneficial for the noise level to have a high f_Z .

The RCXX configuration has the same zero as the differential Twin-T resonator, but requires only half the total capacitance C_Σ at the same impedance level. In general, cross-coupled resonators can be implemented with less total capacitance than Twin-T based resonators, because at high frequency

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

when the filter response is dominated by the impedance of the capacitors, C_1 in Fig. 3.4a is more effective than in Fig. 3.4b. This considerably reduces the chip size for low bandwidth modulators.

Since the resonator frequency response converges against the response of an integrator at high frequency, slew rate and GBW requirements for the opamp are similar to those of an integrator. Similar to the standard first order integrator, finite GBW much higher than the resonance frequency results in an additional pole at approximately the GBW frequency [55].

RCXX, CXX, CYY, Chh and RCX configurations are less sensitive to coupling between opamp input and output by parasitic capacitance than the Twin-T resonator, because the parasite is in parallel to C_1 , which can be chosen much larger or adjusted to account for the parasite.

In contrast to the Twin-T resonator, CYY, RCX and RYY configurations allow to place RC-calibration passgates for either all capacitors or all resistors at the virtual ground, which is beneficial for their linearity.

In Fig. 3.5 a Monte Carlo simulation of the resonator frequency response with 1000 runs and component mismatch with 1% standard deviation is shown. The intrinsic zero at f_z of both the Twin-T and the cross-coupled resonators has been canceled in the feed-in path with a technique that will be discussed in Section 3.5 in order to have identical nominal transfer functions according to (3.2.4).

The variants Chh and Rhh have been omitted for better visibility, because these are only mirrored versions of variants CYY and RYY that share the same sensitivity to component mismatch. For all single-opamp resonators the frequency spread of the resonant peaks is smaller than for the classic Tow-Thomas resonator. Accordingly, also the worst case gain at the nominal resonance frequency $f_0 = 10$ MHz is higher than for the Tow-Thomas resonator. Hence, single-opamp resonators appear to be more robust to component mismatch than the Tow-Thomas resonator.

In Fig. 3.6 the input referred noise is shown. It has been simulated with the same setup as for the Monte Carlo simulation. The opamp has been noiseless in this simulation setup and the feed-in resistor R_i has been identical for all resonators in order to obtain the same noise level close to DC.

In comparison to the Tow-Thomas resonator the noise increases stronger for lower frequency f_z of the intrinsic zero and for a lower input impedance of the feedback network $|Z_{f0,2}|$ at the virtual ground of the opamp. Those variants of the cross-coupled and the Twin-T resonators that have the same f_z

3.4. Cross-Coupled Single-Opamp Resonator

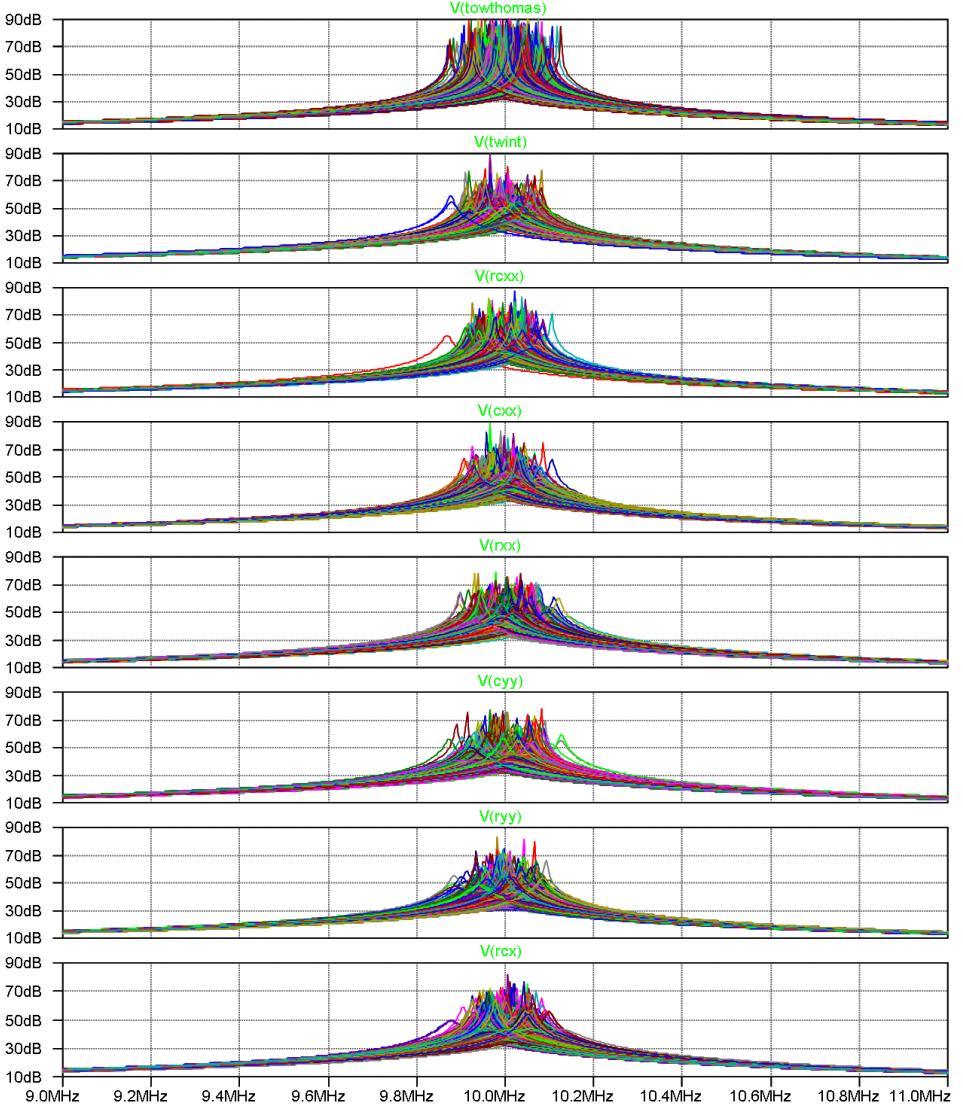


Figure 3.5.: Monte Carlo simulation of the resonator frequency response with 1000 runs and component mismatch with 1 % relative standard deviation.

and $|Z_{f_0,2}|$ also show an identical noise increase of approximately 3 dB versus the Tow-Thomas resonator at twice the resonance frequency $f_0 = 10$ MHz.

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

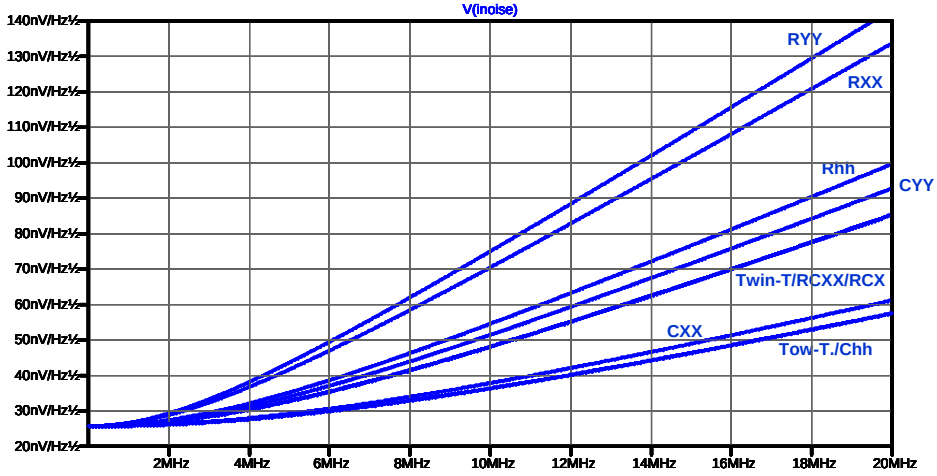


Figure 3.6.: Input referred noise voltage of resonator with ideal opamp.

The noise performance of the CXX variant is close to the Tow-Thomas resonator and the noise performance of the Chh variant is exactly the same as for the Tow-Thomas resonator.

In Fig. 3.7 the input referred noise is shown under the influence of an equivalent input referred opamp noise voltage that equals the thermal noise voltage of the two feed-in resistors R_i . In this scenario, the noise gain due to $|Z_{f0,2}|$ has a significant impact. Still the CXX and the Chh variants perform best, but in general all single-opamp resonators require a lower noise opamp than the Tow-Thomas resonator in order to avoid a degradation of the noise performance.

3.4. Cross-Coupled Single-Opamp Resonator

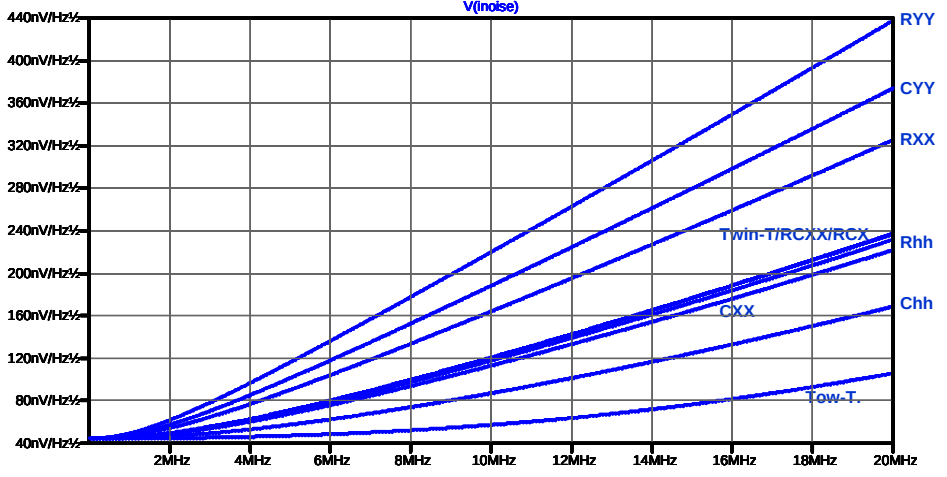


Figure 3.7.: Input referred noise voltage of resonator with real opamp.

Combining a resonator according to (3.4.4) with either a passive first order low- or high-pass both with a time constant

$$R_{BP}C_{BP} = R_{LP}C_{LP} = \frac{1}{2\pi f_Z} \quad (3.4.9)$$

yields the same types of transfer functions (3.2.3) (3.2.4) as for the Tow-Thomas resonator;

$$\begin{aligned} H_{BP,a}(s) &= \frac{Y(s)}{X_{BP}(s)} = \frac{R_0}{R_{BP}} \frac{s R_{BP} C_{BP}}{s^2 / (2\pi f_0)^2 + 1} \\ H_{BP,b}(s) &= \frac{Y_{BP}(s)}{X(s)} = \frac{R_0}{R_i} \frac{s R_{BP} C_{BP}}{s^2 / (2\pi f_0)^2 + 1} \\ H_{LP,a}(s) &= \frac{Y(s)}{X_{LP}(s)} = \frac{R_0}{R_{LP}} \frac{1}{s^2 / (2\pi f_0)^2 + 1} \\ H_{LP,b}(s) &= \frac{Y_{LP}(s)}{X(s)} = \frac{R_0}{R_i} \frac{1}{s^2 / (2\pi f_0)^2 + 1} \end{aligned} \quad (3.4.10)$$

A low- and a high-pass RC-filter can be added as feed-in paths at the virtual ground of the resonator (Fig. 3.8a) in order to have the two inputs that are

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

required for the feedback compensation of the modulator. In this scenario the disadvantage is that there are no silent virtual ground nodes to inject currents from the feedback DACs, which is detrimental for their linearity.

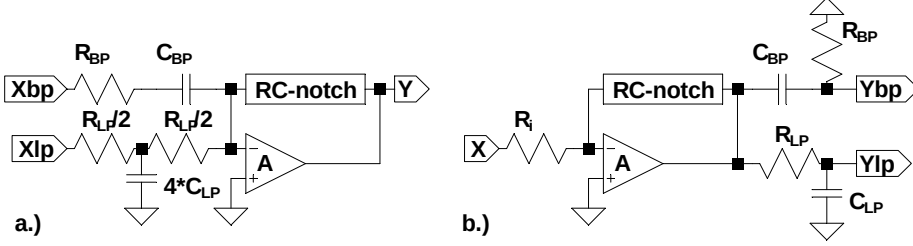


Figure 3.8.: Low- and high-pass, a.) at the input, b.) at the output of the resonator.

Similarly, if both a low- and a high-pass RC-filter is added at the output (Fig. 3.8b), the Tow-Thomas resonator can be directly replaced in feed-forward compensated loop filters. The disadvantage in this case is that an active summation stage for the feed-forward coefficients is required to suppress any interaction of the resulting high impedance resonator outputs. This increases both the power- and area-consumption and may lead to additional GBW-induced ELD due to the summation opamp.

To avoid these disadvantages, the resonator network can be extended by additional components in order to obtain a second order numerator polynomial (3.1.1) that allows direct filter synthesis by cascading biquad resonator stages according to (3.1.2).

3.5 Second Order Numerator Using Capacitive Feed-in

The components R_x , C_x , C_f in Fig. 3.9 allow to obtain an arbitrary second order numerator polynomial in its transfer function, while the input signal is still injected at the virtual ground for lower power consumption due to reduced loading of the preceding stage and less thermal noise than in case of the modified Twin-T resonator (Fig. 3.3).

The basic principle behind the modification of the transfer function with the feed-in paths R_x , C_x and C_f is analogous to the single-opamp PID-con-

3.5. Second Order Numerator Using Capacitive Feed-in

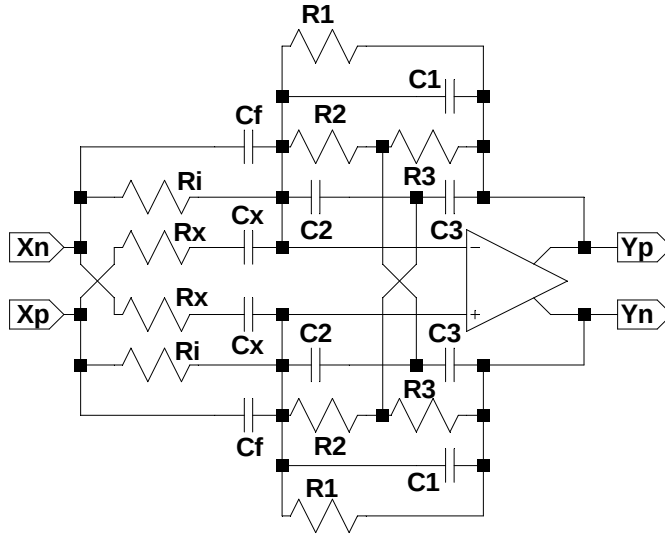


Figure 3.9.: Generic cross-coupled resonator with second order numerator polynomial.

troller illustrated in Fig. 3.10, where the transfer function of an integrator with zero resistor R is modified by different RC feed-in paths.

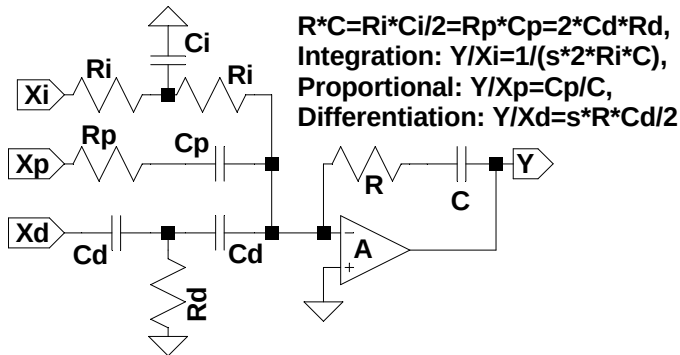


Figure 3.10.: Modifying transfer functions that contain a real zero by RC feed-in paths for single-opamp PID-control.

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

In a differential implementation, the T-networks in Fig. 3.10 can be replaced by a cross-coupled RC feed-in plus a direct capacitive feed-in or a direct resistive feed-in to arrive at the feed-in network of Fig. 3.9.

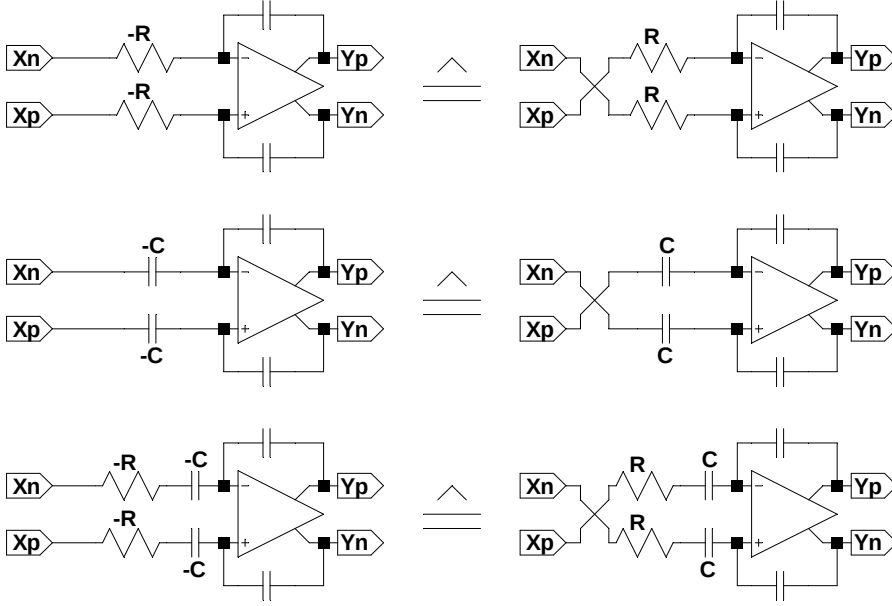


Figure 3.11.: Interpretation of negative component values in the feed-in paths of integrators and resonators.

Please note that in Fig. 3.9 it may be necessary to choose R_x and C_x or R_f and C_f negative. According to Fig. 3.11 in the circuit this means that these components must be connected to the opposite filter input terminal.

If the condition

$$R_x C_x = \frac{1}{2\pi f_Z} \quad (3.5.1)$$

is fulfilled, the zero in (3.4.4) is eliminated and any desired set of coefficients for the second order numerator polynomial can be chosen with

$$H(s) = H_X(s) \frac{s^2 R_i C_f R_x C_x + s [R_i (C_f - C_x) + R_x C_x] + 1}{s R_x C_x + 1}. \quad (3.5.2)$$

Choosing $R_i = \infty$ and $C_f = 0$ allows to use this technique also to replace the resonators in band-pass $\Sigma\Delta$ converters [70] with the transfer function

$$H(s) = \frac{-sR_0C_x}{s^2/(2\pi f_0)^2 + 1}. \quad (3.5.3)$$

Regarding chip size, it is interesting to note that the higher the ratio f_Z/f_0 of the intrinsic zero of the resonator, the smaller the capacitor C_x will become.

In the noise simulations shown in Fig. 3.6 and Fig. 3.7, the R_x feed-in path has been used to eliminate the intrinsic zero of the single-opamp resonators in order to have the same low-pass transfer function (3.2.4) as for the Tow-Thomas resonator. For loop filters of $\Sigma\Delta$ -modulators zeros in the numerator are required anyway. Hence, it is sufficient to modify the existing zeros instead of eliminating them.

For this reason, the value of R_x is usually always larger than R_i and therefore, the noise degradation due to the additional noise of R_x is bound by 3 dB and the additional load of the preceding stage due to the R_x, C_x feed-in path is smaller than the load due to the R_i feed-in path. On the other hand, this also means that the noise performance of the CXX and Chh resonator variant may become even better than the noise performance of the standard Tow-Thomas resonator in applications within $\Sigma\Delta$ -modulators, because the noise contribution of R_x will typically become smaller than shown in Fig. 3.6 and Fig. 3.7.

However, with rising frequency the degradation due to the noise gain of the opamp can become higher than 3 dB due to the additional C_f feed-in path. At the same time, the preceding stage is capacitively loaded by C_f , which increases the power consumption of the driving stage.

3.6 Second Order Numerator Using Bypass

The noise gain and the capacitive load of the previous method of obtaining a second order numerator can be mitigated for reduced power dissipation by a bypass path via resistors R_s and R_p .

3. RC-Resonators in Continuous-Time- $\Sigma\Delta$ -ADCs

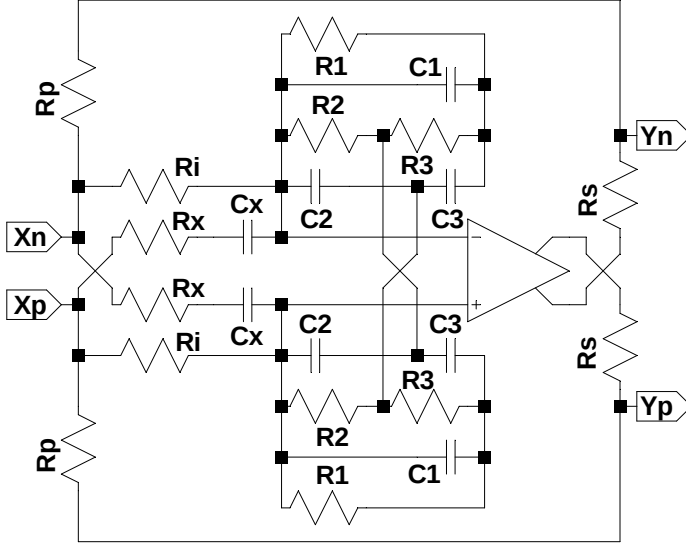


Figure 3.12.: Generic cross-coupled resonator with second order numerator polynomial using a bypass path.

Using (3.5.2) with $C_f = 0$ in the transfer function

$$H_p(s) = \frac{R_s + R_p H(s)}{R_s + R_p} \quad (3.6.1)$$

results in

$$H_p(s) = \frac{1 + \gamma}{1 + R_p/R_s} \frac{\frac{s^2}{(2\pi f_0)^2(1+\gamma)} + \frac{s(1-R_i/R_x)}{2\pi f_Z(1+1/\gamma)} + 1}{s^2/(2\pi f_0)^2 + 1} \quad (3.6.2)$$

with $\gamma = \frac{R_p R_0}{R_i R_s}$.

The purely resistive output impedance that is defined by the equivalent resistance of the parallel connection of R_s and R_p can be scaled to represent the input resistor at the virtual ground of a subsequent stage. In this way coupling between resonator input and output via R_p is avoided.

Moreover, the output impedance can be split in parallel networks and each network can be scaled such, that their output impedances represent R_i , R_p and R_x of a subsequent resonator.

3.6. Second Order Numerator Using Bypass

In contrast to the modified Twin-T resonators in Fig. 3.3, the numerator polynomial is defined here without modifying the notch network, which results in better component matching due to the possibility to implement one of the optimal solutions from Tab. 3.1.

4 Resonant Low Power Single-Opamp Integrators

The improved second and third order integrators that are discussed in this chapter are based on the cross-coupled single-opamp resonator. These integrators overcome all the drawbacks of the single-opamp resonators that were discussed in Chapter 3. For the third order Integrator, an additional pole at the origin of the s -plane is available, which makes this structure attractive for the first stage of the loop filter, where large in-band gain is needed to suppress noise and distortion originating from subsequent stages. Modulators with orders larger than three can be implemented by cascading these second and third order single-opamp integrators.

4.1 Resonant Single-Opamp Loop Filter

The second order integrator in Fig. 4.1 consists of a feed-in, a notch and a first order low-pass network, while the third order integrator in Fig. 4.2 consists of a feed-in, a notch and a first order high-pass network. The notch network defines a pair of conjugate imaginary poles and thereby the resonance frequency f_0 . The low- and high-pass networks define two zeros and in case of the high-pass an additional pole at the origin of the s -plane.

4. Resonant Low Power Single-Opamp Integrators

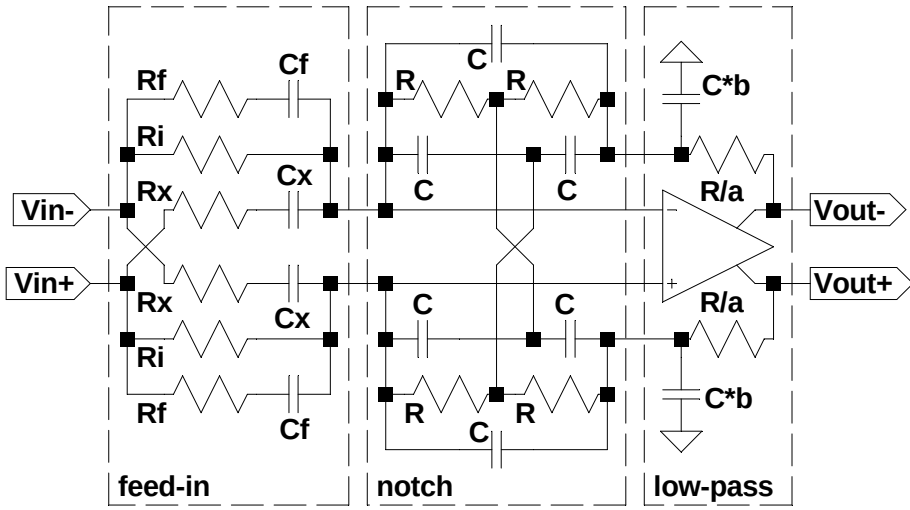


Figure 4.1.: Resonant second order single-opamp integrator.

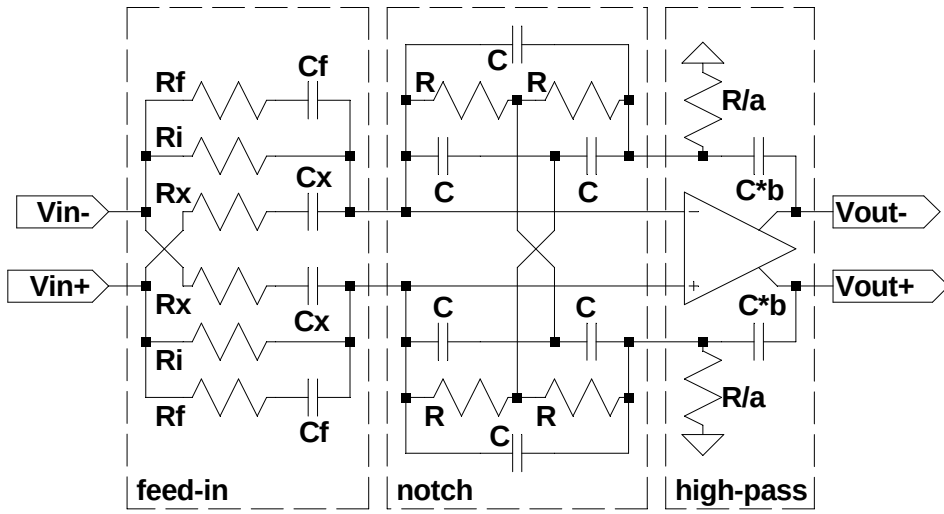


Figure 4.2.: Resonant third order single-opamp integrator.

4.2 Differential Mode

Using only the R_i feed-in path ($R_x = R_f = \infty$) in Fig. 4.1 or Fig. 4.2, the analytic expression for the resonant differential transfer function becomes

$$L_{diff}(s) = -H_0(s) \frac{R_0}{R_i} \frac{\left(\frac{s}{2\pi f_x} + 1\right) \left(\frac{s}{2\pi f_f} + 1\right)}{\frac{s^2}{(2\pi f_0)^2} + 1} \quad (4.2.1)$$

with the parameters

$$\begin{aligned} f_z &= \frac{1}{2\pi RC}, & f_0 &= \frac{f_z}{\sqrt{3}}, & R_0 &= \left(2 + \frac{1}{a}\right) R, \\ f_x &= \frac{1}{2\pi R_x C_x} = \frac{4 + a + b - \sqrt{13 + 2a + 6b + (a - b)^2}}{3 + 2b} f_z, & (4.2.2) \\ f_f &= \frac{1}{2\pi R_f C_f} = \frac{4 + a + b + \sqrt{13 + 2a + 6b + (a - b)^2}}{3 + 2b} f_z \end{aligned}$$

where $H_0(s)$ is either unity in case of the second order modulator (Fig. 4.1) or

$$H_0(s) = \frac{2\pi a}{sb} f_z \quad (4.2.3)$$

in case of the third order modulator (Fig. 4.2).

Both zeros in (4.2.1) are real, because the expressions under the square roots in (4.2.2) are always positive. The zero at f_x converges from lower frequency against f_z for large values of ratio a and small values of ratio b (Fig. 4.3). The zero at f_f converges from higher frequency against f_z for small values of a and large values of b (Fig. 4.4).

For a third order low-pass modulator, the optimum frequency of the resonance f_0 is $\sqrt{3/5}$ times the bandwidth of interest [10, pp. 107–111]. Referring to Tab. 3.1, the maximum frequency f_z that can be obtained for the zero at f_x is therefore limited to only $\sqrt{9/5} \approx 1.34$ times the bandwidth of interest. For a reasonable third order noise shaping, the frequencies of both zeros must be well above the bandwidth of interest.

The zero at f_f , which is always located above f_z , can be adjusted accordingly using the parameters a and b . However, the zero at f_x must be shifted to the desired frequency using the high-pass feed-in path R_x, C_x .

4. Resonant Low Power Single-Opamp Integrators

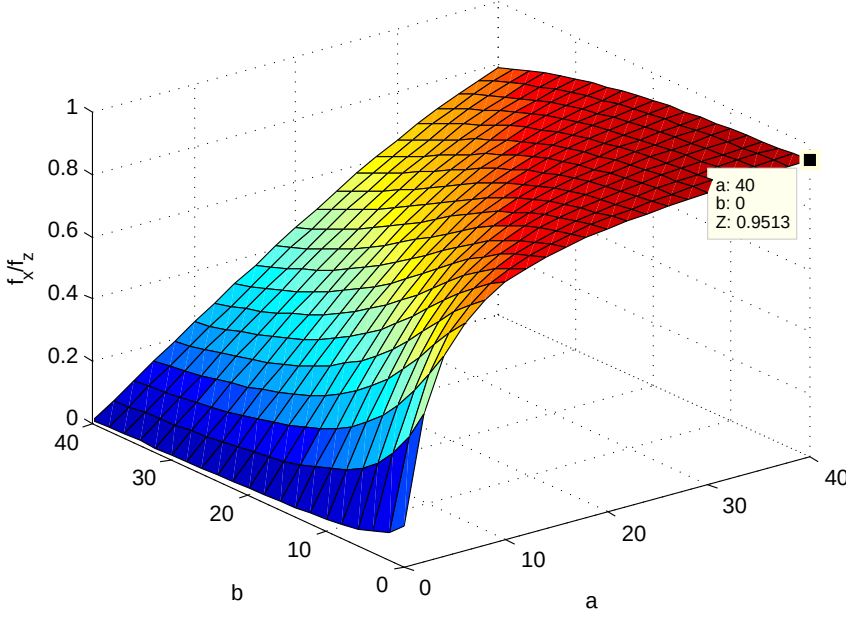


Figure 4.3.: Relative frequency f_x/f_z versus parameters a, b .

The original zero at f_x is canceled, if the $R_x C_x$ time constant matches $1/(2\pi f_x)$ and a new zero at f_x^* is defined by

$$f_x^* = \frac{f_x}{1 - \frac{R_i}{R_x}}. \quad (4.2.4)$$

The two real zeros f_x^* and f_f can now be placed arbitrarily above f_z .

For a more aggressive noise shaping, it is necessary to have the design freedom to place conjugate complex zeros as well. This can be achieved using the additional R_f, C_f high-pass feed-in path in Fig. 4.2. If its time constant $R_f C_f$ matches $1/(2\pi f_f)$, the differential transfer function L_{diff} becomes

$$L_{diff}(s) = -H_0(s)R_0 \frac{s^2 \frac{\frac{1}{R_i} - \frac{1}{R_x} + \frac{1}{R_f}}{(2\pi)^2 f_f f_x} + s \left(\frac{\frac{1}{R_i} - \frac{1}{R_x}}{2\pi f_x} + \frac{\frac{1}{R_i} + \frac{1}{R_f}}{2\pi f_f} \right) + \frac{1}{R_i}}{\frac{s^2}{(2\pi f_0)^2} + 1}. \quad (4.2.5)$$

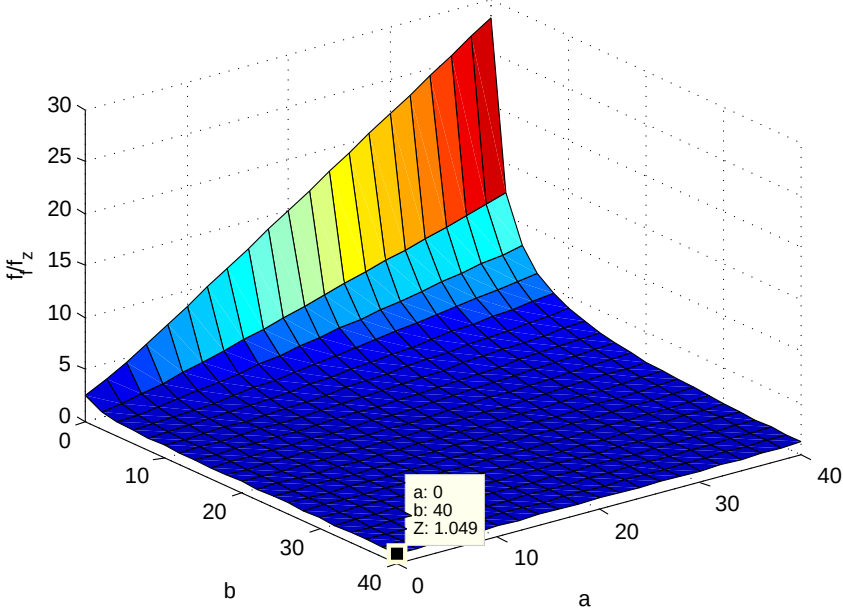


Figure 4.4.: Relative frequency f_f/f_z versus parameters a, b .

All numerator coefficients can now be adjusted arbitrarily via the resistors in the feed-in network. This not only allows to implement a more aggressive noise shaping with high frequency noise peaking but enables also to implement a filter with two feed-in networks (Fig. 4.5a) to define two transfer functions with different numerator polynomials. Thus, NTF and STF can be designed independently using this two-input-single-output filter.

The minus signs in the numerator of (4.2.5) represent the cross-coupling of the R_x, C_x feed-in path. For further design freedom, the feed-in networks can be modified to define either signs in front of all resistor terms in (4.2.5) by using cross- or direct-coupling in the corresponding feed-in path. Moreover, a single-input feed-in network can be moved alternatively to the input of a subsequent integrator or summation stage in order to have a virtual ground available that can be used to inject currents via a current-mode DAC.

4. Resonant Low Power Single-Opamp Integrators

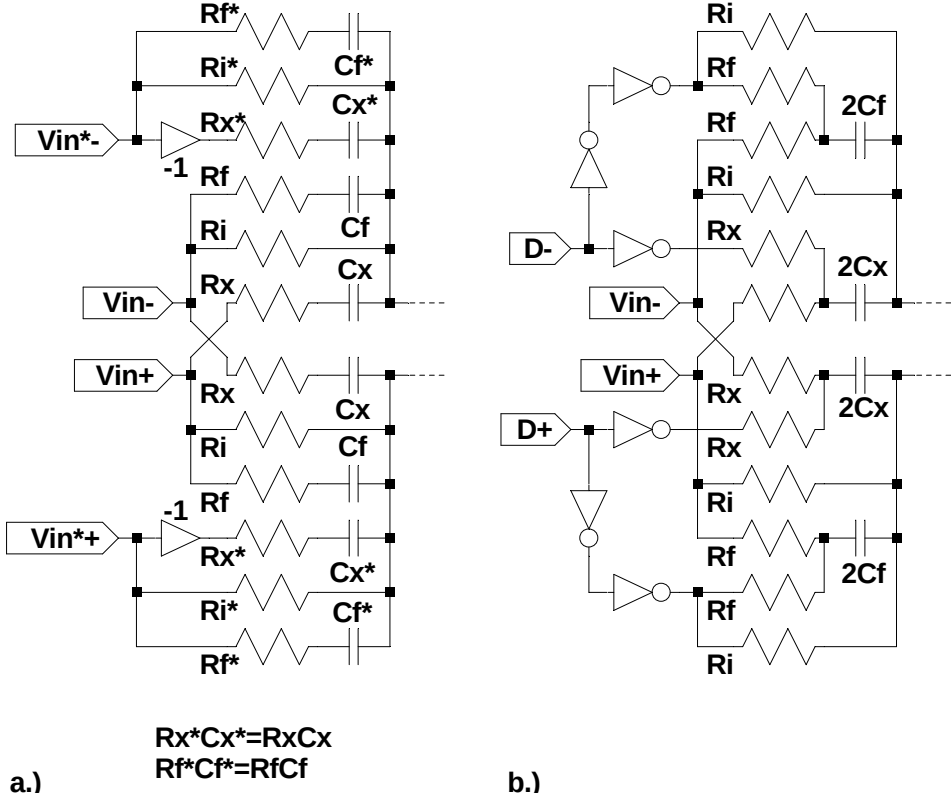


Figure 4.5.: a.) Separate feed-in networks, b.) mostly-digital feed-in network implementation of testchip 2.

The expression for the peak gain (3.4.7) remains valid for this improved integrator with

$$Z_{f0,2} = R \frac{1 - j\sqrt{3}}{2}, \quad (4.2.6)$$

and with

$$Z_{f0,3} = R \left(\frac{1 - j\sqrt{3}}{2 + b + jb/\sqrt{3}} + \frac{1}{a} \right) \quad (4.2.7)$$

in case of the second order integrator and with

$$Z_{f_0,3} = R \left(\frac{1 - j\sqrt{3}}{2 + a - ja\sqrt{3}} - \frac{j\sqrt{3}}{b} \right) \quad (4.2.8)$$

in case of the third order integrator respectively. Obviously, parameters a and b have an impact on the peak gain of the integrator at the resonance frequency via the voltage divider at the output of the opamp. Hence, the required output impedance of the opamp has to be taken also into account when optimizing a and b .

Large values of parameter a and small values of b result in a small integrator time constant in (4.2.3), while at the same time the gain factor R_0/R_i in (4.2.2) decreases asymptotically towards a lower bound. In total, large values of a and small values of b translate into high integrator gain.

For a given transfer function, a high integrator gain requires also a high impedance level of the feed-in network, which results in a high input-referred thermal noise of the integrator. On the other hand, the high-pass-shaped thermal noise introduced by R_x can be minimized by choosing large values of a and small values of b to obtain $f_x \approx f_z$.

These partially conflicting dependencies mandate optimizing a and b for low thermal noise under consideration of aspects like chip size, load for the opamp or component matching.

The cross-coupled notch filter in Fig. 4.2 can be implemented in different ways. This allows to further reduce the noise contribution of R_x to some extent by choosing a notch filter configuration with a high ratio f_z/f_0 .

For the mostly-digital testchip that will be discussed in Chapter 8, the CXX notch configuration has been selected because it has the highest f_z/f_0 ratio of all configurations listed in Tab. 3.1. The CXX configuration also has good matching properties, because all component values are identical. Furthermore, it allows implementing the integrator with the smallest total capacitance for high area-efficiency. Equations (4.2.1), (4.2.4) and (4.2.5) are valid for all notch configurations, whereas the parameters (4.2.2), (4.2.6), (4.2.7) and (4.2.8) are specific to the CXX notch configuration. General expressions for these parameters are given in Appendix A.3.

4.3 Common Mode

The analytic common mode transfer function (Appendix A.4) contains one additional pole and one additional zero that cancel for $f_x = f_z$. Close to this condition, the transfer function converges against

$$L_{cm}(s) = -H_0(s)R_0 \frac{s^2 \frac{\frac{1}{R_i} - \frac{1}{R_x} + \frac{1}{R_f}}{(2\pi)^2 f_f f_x} + s \left(\frac{\frac{1}{R_i} - \frac{1}{R_x}}{2\pi f_x} + \frac{\frac{1}{R_i} + \frac{1}{R_f}}{2\pi f_f} \right) + \frac{1}{R_i}}{\frac{s^2}{(2\pi f_0)^2} + s \left(\frac{1}{2\pi f_z} + \frac{f_z}{2\pi f_0^2} \right) + 1}. \quad (4.3.1)$$

In contrast to (4.2.5), (4.3.1) is non-resonant due to the non-zero second

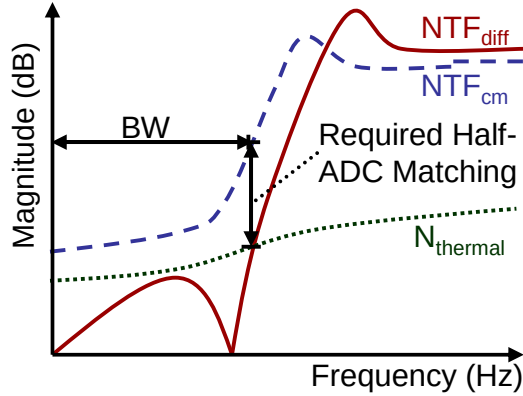


Figure 4.6.: Differential and common mode NTFs.

order term in the denominator polynomial. This term results in non-optimal distribution of the common mode quantization noise in the band of interest and in lower frequency NTF poles (Fig. 4.6).

Cross-coupling in the feed-in network does not change the sign of the feed-in current in common mode. Therefore, the minus signs in (4.3.1) become plus signs unless an inverting gain-stage instead of cross-coupling (Fig. 4.5a) is used to realize the same numerator in (4.2.5) and (4.3.1) for the quantized

feedback signal¹. In Fig. 4.5b the corresponding scheme is depicted that has been implemented in the mostly-digital testchip that will be discussed in Chapter 8. The inversion of the quantized feedback signal is done here in the digital domain by CMOS inverters to save power.

4.4 Implementation Example

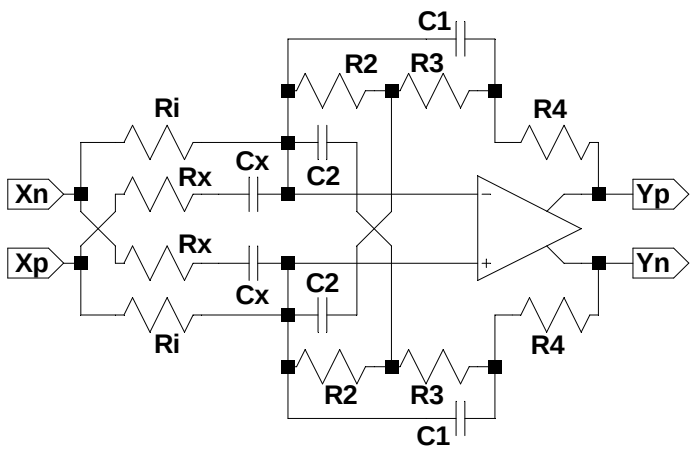


Figure 4.7.: Cross-coupled CYY resonator with second order numerator polynomial.

Table 4.1.: CYY Resonator Example

R_2	R_3	R_4	R_i	R_x	C_1	C_2	C_x
$2.9k$	$2.9k$	$1.23k$	$2.79k$	$3.6k$	$2.44p$	$4.88p$	$2.44p$

¹ Denoted by starred terminal and component names.

4. Resonant Low Power Single-Opamp Integrators

Table 4.2.: Modified Twin-T Resonator Example

R_{in1}	R_{in2}	R_1	R_2	R_3	C_{in}	C_1	C_2	C_3
400	1k	1k	1k	222	1p	10p	10p	21p

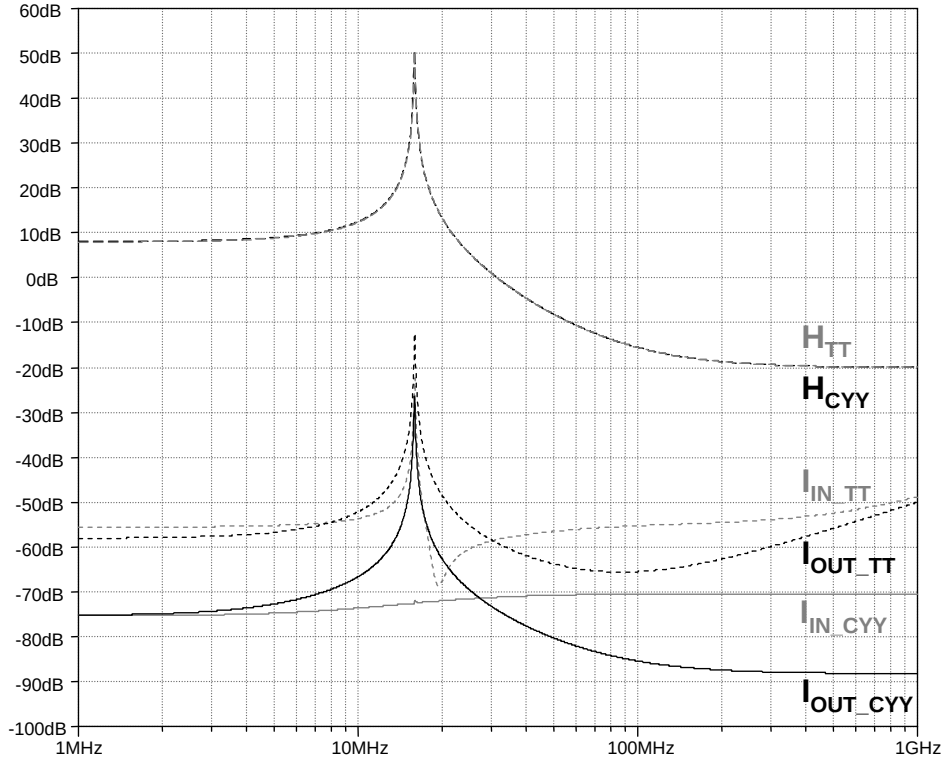


Figure 4.8.: CYY and modified Twin-T resonator frequency response and load currents of opamp and preceding stage in dBA for a 0 dBV input signal.

The component values of a cross-coupled resonator according to Fig. 4.7 and a modified Twin-T resonator according to Fig. 3.3(a) in a differential implementation are listed in Tab. 4.1 and Tab. 4.2, where each implementation is realizing a pair of conjugate imaginary poles at 16 MHz and two real zeros at 80 MHz (Fig. 4.8).

The impedance level has been chosen to obtain the same low frequency noise level². This results in much lower total capacitance and higher feed-in impedance level of the CYY resonator. Due to the higher feed-in impedance level and the resistive signal injection at the virtual ground, the current load for the previous stage is much smaller in case of the CYY resonator as can be seen when comparing I_{IN_TT} and I_{IN_CYY} in Fig. 4.8.

Also the output current of the opamp due to the feedback network itself is considerably smaller (I_{OUT_TT} versus I_{OUT_CYY} in Fig. 4.8).

Hence, in this example the power dissipation in the output stage of the opamp of the preceding stage as well as in the output stage of the resonator opamp could be reduced by substituting the modified Twin-T resonator with the CYY resonator. Moreover, also the total capacitance which dominates the chip area could be reduced significantly.

4.5 Integrator Swing Scaling for High-Order Modulators

Second and third order modulators can be implemented directly using the proposed single-opamp integrators. An advantage of such modulators is that saturation of internal loop filter nodes that might lead to instability cannot occur. The only node that can go into saturation is the output of the loop filter which is also the input of the quantizer (Fig. 2.2).

Both the loop filter opamp output stage and the quantizer have a limited voltage range, where the quantizer input voltage range must be smaller than the voltage range of the opamp output stage in order to avoid dead codes in the output of the quantizer.

Hence, as long as the quantizer is not overloaded, no saturation within the loop filter will occur. This is advantageous when compared to standard second and third order state space loop filters, where internal states of the loop filter can saturate. Saturation within the loop filter results in additional non-linearity that degrades the SQNR and may cause persistent oscillations which need to be detected and reset by extra circuitry.

² assuming a noiseless opamp

4. *Resonant Low Power Single-Opamp Integrators*

However, for higher order modulators that are implemented by cascading second and third order integrators according to (3.1.2), the internal loop filter nodes that connect the individual high order integrators can saturate. This has to be avoided by using a linear transformation of the loop filter that is also known as integrator swing scaling. The scaling process is analogous to the integrator swing scaling of standard state space loop filters.

The modulator ADC input signals have to be identified by time domain simulation that cause the largest voltage swings at the internal nodes of the loop filter with ideal non-saturating opamps. These worst case voltage swings then need to be scaled by modifying the impedance levels of the feed-in and/or the feedback networks of the individual high-order integrators such that no saturation occurs with real opamps and the overall transfer function of the loop filter remains unchanged.

5 Analysis of DAC Sensitivity to Extrinsic Noise

The feedback DAC is the most critical building block in a CT- $\Sigma\Delta$ -ADC for two reasons:

- It is connected in parallel to the input signal of the ADC. Any noise or distortion generated by the feedback DAC will appear as an additional undesired input signal. Consequently, the performance of the whole ADC is limited by the performance of this building block.
- The digital signal that feeds the DAC not only contains the desired ADC input signal but also strong high frequency quantization noise that can intermodulate or fold extrinsic noise such as sampling clock jitter or noise that is superimposed on the DAC reference into the band of interest.

For the design of high performance CT- $\Sigma\Delta$ -ADCs it is therefore of utmost importance to understand the impact of clock jitter and reference noise on the DAC noise floor¹.

Traditionally, the effect of clock jitter in CT- $\Sigma\Delta$ -ADCs has been studied by calculating charge errors generated by the feedback DAC in the time domain [72–75]. A Non-Return-to-Zero (NRZ)-DAC generates charge errors only when the digital data changes [53]. For example, in [11, pp. 94–99] this dependency on the input data is taken into account by an empirically found activity factor.

In contrast to this empirical approach the aim of this section is to identify the mechanism that maps sampling clock jitter and noise of the DAC

¹ The effect of DAC non-linearity will be covered in the next chapter.

5. Analysis of DAC Sensitivity to Extrinsic Noise

reference voltage or current onto the baseband noise floor for Return-to-Zero (RZ)- and NRZ-DACs by rigorous analysis in the time and frequency domain.

Some papers about jitter-induced noise use the Root Mean Square (RMS) phase jitter for their calculations and thereby implicitly assume white phase noise [76]. However, there is a significant dependence of the baseband noise on the spectral shape of the phase noise as will become apparent from the expressions derived in this chapter.

The derived time domain equations serve as a basis for a fast transient simulation model, while the derived frequency domain equations help to intuitively understand the requirements for the clock phase noise and the decoupling of the DAC reference voltage or current.

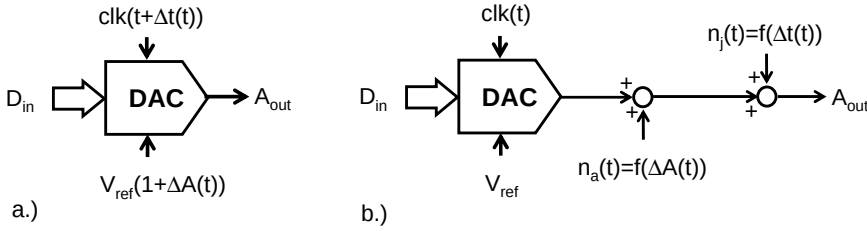


Figure 5.1.: a.) Real DAC with clock jitter and noisy reference signal, b.) equivalent model with additive noise sources.

The goal of the following derivation is to describe the in-band noise that is induced by clock jitter and noise of the DAC reference by equivalent additive noise sources (Fig. 5.1) at the output of the DAC.

5.1 Time Domain Synthesis

NRZ-DAC pulses modulated by both clock jitter $\Delta t(t)$ and reference noise $\Delta A(t)$ can be constructed by multiplication of the modulated square wave clock signals $c_j(t)$, $1 - c_j(t)$ and time interleaved version $y_{odd}(t)$, $y_{even}(t)$ of the non-modulated NRZ data signal $y_{ideal}(t)$ (Fig. 5.2).

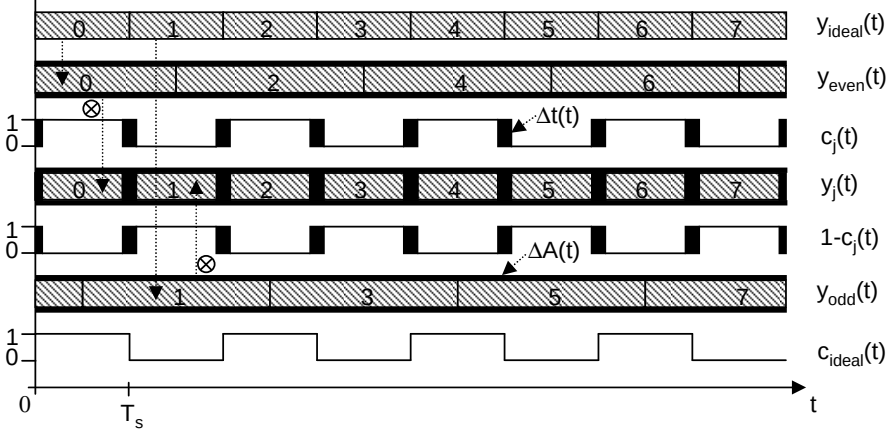


Figure 5.2.: Time domain synthesis of NRZ-DAC pulses.

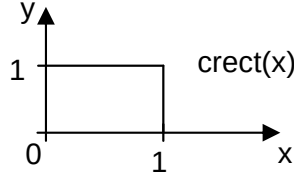


Figure 5.3.: Causal rectangular function.

With $crect(x)$ being the causal rectangular function (Fig. 5.3), $y[n]$ the data sequence and T_s the sampling period,

$$y_{ideal}(t) = \sum_{n=-\infty}^{\infty} y[n] \text{crect} \left(\frac{t}{T_s} - n \right) \quad (5.1.1)$$

can be split into the two interleaved data signals

$$y_{even}(t) = (1 + \Delta A(t)) \sum_{n=-\infty}^{\infty} y[2n] \text{crect} \left(\frac{t}{2T_s} - n \right) \quad (5.1.2)$$

and

$$y_{odd}(t) = (1 + \Delta A(t)) \sum_{n=-\infty}^{\infty} y[2n - 1] \text{crect} \left(\frac{t}{2T_s} - n + \frac{1}{2} \right). \quad (5.1.3)$$

5. Analysis of DAC Sensitivity to Extrinsic Noise

where $\Delta A(t)$ is the noise of the DAC reference. The DAC output signal then becomes

$$\begin{aligned} y_j(t) &= y_{\text{even}}(t)c_j(t) + y_{\text{odd}}(t)(1 - c_j(t)) \\ &= y_{\text{odd}}(t) + (y_{\text{even}}(t) - y_{\text{odd}}(t))c_j(t). \end{aligned} \quad (5.1.4)$$

From (5.1.4) it becomes apparent that an NRZ-DAC operates as a multiplicative mixer. DAC reference noise and phase noise sidebands of the clock fundamental tone and its harmonics are demodulated into the baseband by a filtered version of the data signal. The transfer function of the filter applied to the data signal depends on the pulse shape and will be analyzed in Section 5.3. As a prerequisite for this discussion the modulation of clock signals by phase noise is discussed in the next section.

5.2 Jitter-Modulated Clock Signals

A square wave clock signal² $c_j(t)$ with a period $2T_s$ that is modulated by a timing error of the clock edges $\Delta t(t)$ can be expressed as:

$$c_j(t) = c_{\text{ideal}}(t + \Delta t(t)) = \frac{1}{2} + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{\sin\left(\frac{\pi}{T_s}(2k-1)(t + \Delta t(t))\right)}{2k-1} \quad (5.2.1)$$

Applying the small angle approximation

$$\sin(\alpha + \beta) \approx \sin \alpha + \beta \cos \alpha \quad \text{for} \quad |\beta| \ll 1 \text{rad} \quad (5.2.2)$$

yields

$$\begin{aligned} c_j(t) &\approx c_{\text{ideal}}(t) + \frac{2\Delta t(t)}{T_s} \sum_{k=1}^{\infty} \cos\left(\frac{\pi}{T_s}(2k-1)t\right) = \\ &c_{\text{ideal}}(t) + \Delta t(t) \sum_{n=-\infty}^{\infty} (-1)^n \delta(t - nT_s) = \\ &c_{\text{ideal}}(t) + \sum_{n=-\infty}^{\infty} (-1)^n \Delta t[n] \delta(t - nT_s) \end{aligned} \quad (5.2.3)$$

² In order to simplify further derivations let $c_j(t)$ represent a clock signal with a clock rate of only half the sampling clock rate.

where the series

$$\Delta t[n] = \Delta t(nT_s) \quad (5.2.4)$$

that represents the sampled continuous timing error $\Delta t(t)$ of the fundamental sine wave in (5.2.1) is called the Time Interval Error (TIE) of the sampling clock [77].

The equivalence of cosine sum and Dirac sum in (5.2.3) can be shown by successive Fourier transform and inverse Fourier transform. It is worth to note that applying the small angle approximation to (5.2.1) is equivalent to reshaping the pulse width modulated error pulses to weighted Dirac pulses with equal area per pulse.

The number of relevant harmonics h of real world clock signals is limited due to finite edge steepness and the timing modulation due to jitter is usually very small compared to the clock period. Hence,

$$h \frac{\pi}{T_s} |\Delta(t)| \ll 1 \text{ rad} \quad (5.2.5)$$

holds true and the application of the small angle approximation is justified.

From (5.2.3) it is apparent that a jitter-modulated clock signal consists of the unmodulated clock signal and an additive component that is similar to a discrete-time signal. For this reason the additive spectral components due to jitter are periodic and non-decaying, while the unmodulated square-wave clock signal shows only odd order harmonics with a $1/f$ slope³.

5.3 Jitter-Induced Baseband Noise

With the help of (5.2.3), (5.1.4) can be expressed as the sum of an ideal NRZ-DAC output signal $y_{ideal}(t)$, an amplitude modulation noise signal $n_a(t)$ and a jitter-induced noise signal $n_j(t)$, i.e.

$$y_j(t) = y_{ideal}(t) + n_a(t) + n_j(t) \quad (5.3.1)$$

³ This is consistent with the observation that frequency division by a certain factor lowers the phase noise floor by the same factor [78, pp. 224–225].

5. Analysis of DAC Sensitivity to Extrinsic Noise

with

$$n_a(t) = \Delta A(t) y_{ideal}(t) \quad (5.3.2)$$

and

$$\begin{aligned} n_j(t) &= (y_{even}(t) - y_{odd}(t)) \Delta t(t) \sum_{n=-\infty}^{\infty} (-1)^n \delta(t - nT_s) = \\ &= (y_{even}(t) - y_{odd}(t)) \Delta t(t) \left(\sum_{n=-\infty}^{\infty} \delta(t - 2nT_s) - \sum_{n=-\infty}^{\infty} \delta(t - (2n-1)T_s) \right) \\ &= (1 + \Delta A(t)) \Delta t(t) \left(\sum_{n=-\infty}^{\infty} (y[2n] - y[2n-1]) \delta(t - 2nT_s) - \right. \\ &\quad \left. \sum_{n=-\infty}^{\infty} (y[2n-2] - y[2n-1]) \delta(t - (2n-1)T_s) \right) = \\ &= (1 + \Delta A(t)) \Delta t(t) \sum_{n=-\infty}^{\infty} (y[n] - y[n-1]) \delta(t - nT_s). \end{aligned} \quad (5.3.3)$$

Usually both $\Delta t(t)$ and $\Delta A(t)$ are small with respect to the NRZ pulse width and height, respectively. Therefore, the product $\Delta t(t)\Delta A(t)$ in (5.3.3) can be neglected:

$$\begin{aligned} n_j(t) &\approx \Delta t(t) \sum_{n=-\infty}^{\infty} (y[n] - y[n-1]) \delta(t - nT_s) = \\ &\sum_{n=-\infty}^{\infty} \Delta t[n] (y[n] - y[n-1]) \delta(t - nT_s) \end{aligned} \quad (5.3.4)$$

If one is interested in the low frequency components of $n_j(t)$ only, the droop caused by the *sinc* function can be neglected and the Dirac impulse can be replaced by the *crect*(x) function:

$$n_j(t) \approx \sum_{n=-\infty}^{\infty} \frac{\Delta t[n]}{T_s} (y[n] - y[n-1]) \text{crect}\left(\frac{t}{T_s} - n\right) \quad (5.3.5)$$

Note that the TIE $\Delta t(t)$ gets sampled by the Dirac impulses in (5.3.4).

TIE is the discrete-time domain representation of phase noise expressed in seconds or pico-seconds. Hence, $n_j(t)$ represents a discrete-time signal. This allows to simulate the effect of clock jitter in continuous-time $\Sigma\Delta$ -modulators with discrete-time models for increased simulation speed.

To perform such a simulation a random TIE sequence with the correct RMS jitter and the desired spectral shape of the phase noise needs to be generated.

The relation between phase noise and TIE is the following: From (5.2.1) the momentaneous excess phase of the fundamental tone of the clock signal $c_j(t)$ is

$$\phi'(t) = \pi \Delta t(t)/T_s. \quad (5.3.6)$$

The phase noise of a square wave clock signal is specified as a one-sided spectral power density function

$$S_{\phi'}(f)/2 = |\mathcal{F}\{\phi'(t)\}|^2/2 \quad (5.3.7)$$

of the excess phase of its fundamental tone. It is converted into logarithmic scale with the pseudo-unit dBc/Hz, which expresses that the spectral power density of phase noise is proportional to the power of the carrier.

Now, $c_j(t)$ is just a substitute signal that has been used to simplify the construction of the NRZ data signal. One can think of it as a clock that has been derived by a divide-by-2 frequency divider stage from the sampling clock. Usually one is interested in the phase noise of the sampling clock and therefore, at twice the frequency the excess phase doubles [78, pp. 224–225] with

$$\phi(t) = 2\pi \Delta t(t)/T_s \quad (5.3.8)$$

or in the discrete-time domain:

$$\phi[n] = 2\pi \Delta t[n]/T_s. \quad (5.3.9)$$

The one-sided phase noise becomes in units of dBc/Hz

$$\mathcal{L}(f) = 10 \log_{10} \left(\frac{1}{2} S_{\phi}(f) \right) = 10 \log_{10} \left(\frac{1}{2} |\mathcal{F}\{\phi(t)\}|^2 \right). \quad (5.3.10)$$

A jitter-modulated clock signal consists of the unmodulated clock signal and an additive component, which is according to (5.2.3) a periodic repetition

5. Analysis of DAC Sensitivity to Extrinsic Noise

of the phase modulation sidebands around the fundamental tone. Due to this periodicity, the phase noise $\phi(t)$ of a square wave clock signal needs to be measured only at a distance of $0 < \Delta f < \frac{1}{2T_s}$ around the fundamental tone, because any higher frequency component is already contained in this range due to aliasing.

This also means, one needs to integrate only up to $\Delta f = \frac{1}{2T_s}$ in order to calculate the RMS of the TIE $\Delta t(t)$ (also called RMS phase jitter) from the measured phase noise of the sampling clock:

$$\sigma_j = \frac{T_s}{2\pi} \sqrt{2 \int_0^{\frac{1}{2T_s}} S_\phi(f) df} \quad (5.3.11)$$

5.4 Digital Suppression of Jitter-Induced Baseband Noise

Subtracting the discrete-time series

$$n_j[n] = \Delta t[n] (y[n] - y[n-1]) \quad (5.4.1)$$

from the digital output data series $y[n]$ of a CT- $\Sigma\Delta$ -ADC allows to suppress jitter-induced noise via digital post processing when the sampled TIEs $\Delta t[n]$ are known. This is possible, because the differentiation in (5.4.1) filters out most of the spectral portion where $y[n]$ differs from the ideal data series that would be obtained without sampling clock jitter. However, in practical systems there is little benefit of this concept, because measuring the TIE sequence is usually too expensive.

Using a similar approach to suppress phase noise using an out of band helper signal from a high quality oscillator has been demonstrated in [79]. And in [80] another similar method of suppressing phase noise has been proposed. However, these methods represent a compromise that is effective for close-in phase noise skirts only.

5.5 Multi-Rate Application to Arbitrary Return to Zero DACs

Any RZ-DAC with a sampling period T_p , a pulse width T_w and a delay T_d that all are integer multiples of T_s can be modeled by an NRZ-DAC that operates

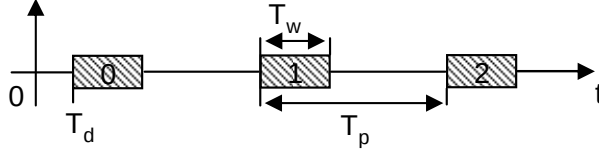


Figure 5.4.: Arbitrary RZ DAC signals.

with a sampling period T_s (Fig. 5.4). This allows to extend the previous considerations to arbitrary RZ-DACs using the multi-rate equation

$$y[n] = \frac{T_p}{T_w} \sum_{k=-\infty}^{\infty} y_{RZ}[k] \delta \left(n - \frac{kT_s + T_d}{T_p} \right) * \sum_{k=0}^{T_w/T_p - 1} \delta(n - k) \quad (5.5.1)$$

to generate a NRZ data series $y[n]$ at a sample rate T_s from an RZ data series at a sample rate T_p by upsampling, where $*$ denotes the convolution operator.

The first Nyquist zone after the upsampling now contains multiple replica images of the first Nyquist zone before upsampling at a level that is higher by a factor T_p/T_w in order to maintain a constant pulse area such that the same low frequency DAC output level as for a NRZ-DAC is obtained.

5.6 Spectral Interpretation

The expression (5.3.2) can be interpreted as multiplicative mixing of the reference noise $\Delta A(t)$ and the data signal $y_{ideal}(t)$ in the continuous-time domain while (5.3.4) can be interpreted as multiplicative mixing in the discrete-time domain of the TIE $\Delta t[n]$ and the high-pass shaped data signal $y[n] - y[n-1]$.

Applying the Fourier transformation, the spectra of $n_a(t)$ and $n_j(t)$ become

$$N_a(f) = \mathcal{F}\{\Delta A(t)\} * \left(\frac{\sin(\pi f T_s)}{\pi f} z^{-0.5} Y(z) \right) \Big|_{z=e^{j2\pi f T_s}} = \mathcal{F}\{\Delta A(t)\} * \left(\frac{1}{j2\pi f} (1 - z^{-1}) Y(z) \right) \Big|_{z=e^{j2\pi f T_s}} \quad (5.6.1)$$

5. Analysis of DAC Sensitivity to Extrinsic Noise

and

$$N_j(f) = \frac{1}{2} \mathcal{F}_d \{ \phi[n] \} * ((1 - z^{-1})Y(z)) \Big|_{z=e^{j2\pi f T_s}} = \frac{1}{2} \mathcal{F} \{ \phi(t) \} * ((1 - z^{-1})Y(z)) \Big|_{z=e^{j2\pi f T_s}} \quad (5.6.2)$$

where $\mathcal{F}$ denotes the continuous and $\mathcal{F}_d$ the discrete-time Fourier transform and

$$z = e^{j2\pi f T_s} \quad (5.6.3)$$

is evaluated on the unit circle in the z -plane.

A remarkable similarity becomes apparent, when comparing (5.6.1) and (5.6.2): In both folding mechanisms, the data signal is filtered by a $1 - z^{-1}$ first order Finite Impulse Response (FIR) high-pass before it folds with noise. This filtering is intrinsic to NRZ-DACs. However, there are also two fundamental differences between both folding mechanisms: There is an additional first order continuous-time integration of the data signal before it folds with reference noise and the reference noise has a continuous spectrum while the phase noise of a square wave clock has a periodic spectrum due to its discrete-time nature.

In Fig. 5.5a the folding of the spectrum of $\Delta A(t)$ with the *sinc*-filtered data signal $Y(z)$ is depicted. Low frequency noise components of $\Delta A(t)$ translate into noise skirts around any discrete in-band desired signal. Higher frequency interfering spurs in $\Delta A(t)$ that are located at frequencies where the quantization noise is high, may fold down significant quantization noise into the band of interest.

It is therefore necessary to provide a sufficiently low frequency decoupled DAC reference and to avoid coupling of interfering signals at those critical frequencies into this reference. This is true not only for frequencies within the first Nyquist zone of $Y(z)$, but also to a lesser extent for higher frequencies that are suppressed by $1/f$ thanks to the *sinc*-function.

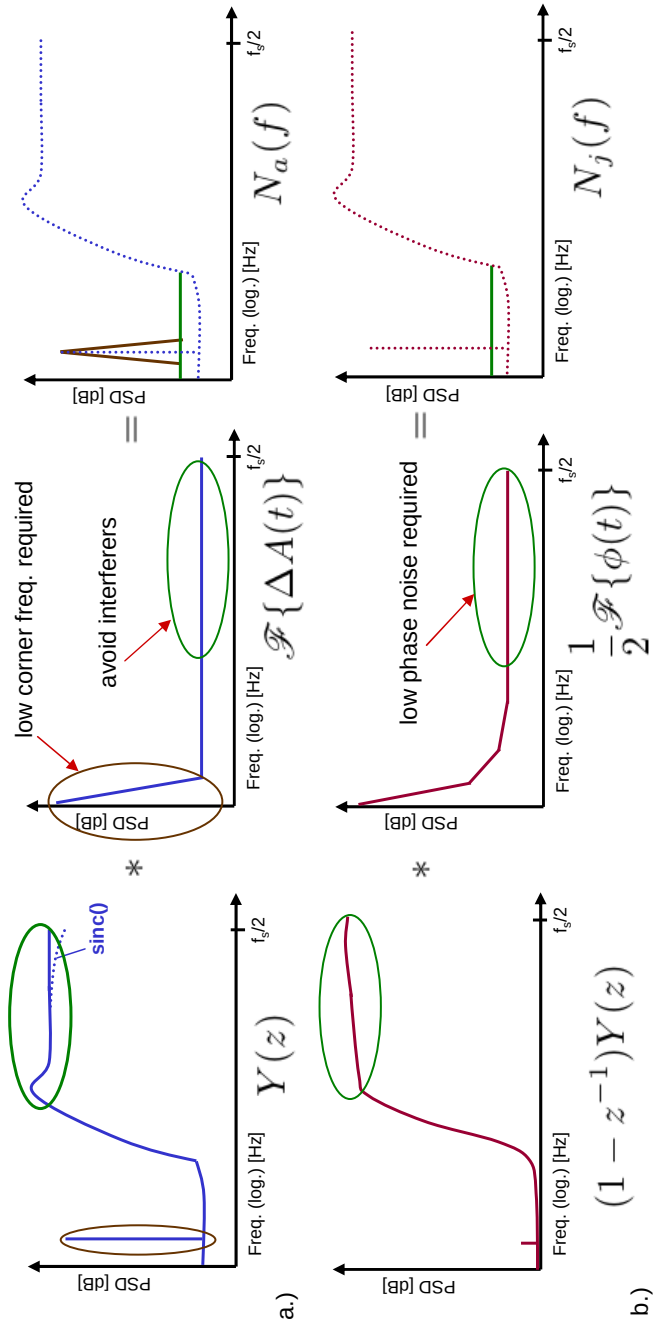


Figure 5.5.: a.) DAC with noisy reference signal, b.) DAC with jitter.

5. Analysis of DAC Sensitivity to Extrinsic Noise

For low-pass NRZ-DACs, the *sinc*-function provides zeros at higher frequency images of the desired in-band signals such that noise folding due to strong desired signals is suppressed. However, for RZ-DACs according to (5.5.1) the *sinc*-function has zeros at a larger frequency distance $1/T_w$ than the periodicity $1/T_p$ of the spectrum of the data signal and the level of the spectrum is higher by a factor of T_p/T_w , i.e. there are strong spectral components between two zeros of the *sinc*-function due to images of the quantization noise and the desired signal.

In a spectral interpretation this means that the first spectra in Fig. 5.5a contains not only the first Nyquist zone of the data signal, but multiple replica images of the first Nyquist zone at a level that is higher than for a NRZ-DAC. These strong spectral components fold more high frequency noise from the RZ-DAC reference into the band of interest than in the NRZ-DAC case.

In Fig. 5.5b the folding of the phase noise spectrum $S_\phi(f)$ with the high-pass filtered data signal $Y(z)$ is depicted. Since both signals have discrete-time spectra according to (5.6.2), the folded spectrum is periodic as well and it is therefore sufficient to consider folding within the first Nyquist zone only.

The $1 - z^{-1}$ first order FIR high-pass filtering of the data signal upfront the folding ensures that all low frequency spectral components are suppressed. This property of NRZ-DACs is very useful, because it avoids folding of low frequency spectral components of the data signal with low frequency phase noise⁴ that typically strongly rises towards the carrier with powers of $1/f$ into low frequency in-band noise at the DAC output.

For a RZ-DAC, the $1 - z^{-1}$ high-pass filtering is less beneficial⁵ due to the implicit zero stuffing of the upsampling in (5.5.1). In a spectral interpretation this means that there are images of the low frequency data signal appearing in-between the zeros of the $1 - z^{-1}$ high-pass filtering.

Consequently, these unsuppressed images of the data signal can fold significant amounts of phase noise into the band of interest. This is the reason why low-pass CT- $\Sigma\Delta$ -ADCs with RZ-DACs suffer from a much stronger SNR degradation with strong test signals than ADCs with NRZ-DACs.

⁴ For phase noise the term frequency refers to the frequency distance from the carrier in this context.

⁵ assuming for the sake of simplicity that $T_w = T_s$

In [81] an SNR degradation of 14 dB has been reported due to this effect. This degradation can become troublesome in radio receivers where a weak signal needs to be processed in the presence of strong in-band neighbor channels.

The jitter-induced in-band noise floor that is observed for low amplitude test signals or idle input in CT- $\Sigma\Delta$ -ADCs is determined by the folding of the strong high frequency quantization noise and the phase noise at the same frequency (Fig. 5.5b).

For this reason LC-Phase Locked Loops (PLLs) are very well suited for providing the sampling clock of continuous-time ADCs, because the quantization noise starts to rise at frequencies that are typically much larger than the region outside the bandwidth of such a PLL, where the phase noise drops significantly due to the low noise LC filtering within the Voltage Controlled Oscillator (VCO). This is true for both low-pass and band-pass ADCs with NRZ-DACs, because the low-frequency portion of the quantization noise in band-pass ADCs is suppressed by the DC zero of the $1 - z^{-1}$ high-pass filtering.

The difference between NRZ- and RZ-DACs with respect to the noise floor that is obtained for idle input is that the charge errors due to timing jitter of the pulse edges are stronger for RZ-DACs, because according to (5.5.1) the height of the RZ-pulses is larger and the high-pass filtering is ineffective due to the implicit zero stuffing.

Hence, for the same STF and NTF, a lower phase noise is required for an CT- $\Sigma\Delta$ -ADC with an RZ-DAC. In a spectral interpretation this means that the first spectrum in Fig. 5.5b contains multiple images of the first Nyquist zone of the data signal and higher frequency images are less suppressed by the high-pass filtering than the first image. Together with the factor T_p/T_w in (5.5.1) this results in more phase noise being folded down into the band of interest.

6 Extrinsic-Noise-Tolerant DACs

The feedback DAC of a $\Sigma\Delta$ -ADC (Fig. 2.2) has to be very linear to avoid intermodulation of out-of-band spectral noise components into the band of interest.

Traditionally, the solution to this linearity problem has been to use inherently linear single-bit DACs. However, CT- $\Sigma\Delta$ -ADCs with single-bit DACs are very sensitive to sampling clock jitter. This became apparent in Chapter 5 where the mechanism that maps DAC timing jitter onto the ADC noise floor has been analyzed. In the next section several ways of mitigating jitter-induced noise are discussed.

An elegant way of reducing the jitter sensitivity of single-bit DACs that has been employed in [35, 82–84] is using mismatch insensitive single-bit FIR-DACs with a low-pass transfer function [85]. This concept will be discussed in Section 6.2.

In order to guarantee loop stability the low-pass transfer function needs to be compensated [86, 87] as will be discussed in Section 6.3.

In Sections 6.4 and 6.5 two compensated FIR-DAC concepts that have been verified in two testchips (Chapters 7 and 8) are proposed. One of these novel concepts integrates two FIR-DACs and a quantizer into a so called Infinite Impulse Response (IIR)-quantizer that reveals remarkable properties which even suggest its application beyond the field of $\Sigma\Delta$ -ADCs.

6.1 Mitigation of Jitter- and Reference-Induced Noise

According to (5.6.1) and (5.6.2), jitter- and DAC reference-induced noise can be mitigated by reducing the spectral content of the data spectrum $Y(z)$. In CT- $\Sigma\Delta$ -ADCs with NRZ-DACs, the low frequency spectral content that is already intrinsically suppressed by the $1 - z^{-1}$ high-pass filtering cannot be further reduced, because it contains also the signal of interest. In contrast

6. Extrinsic-Noise-Tolerant DACs

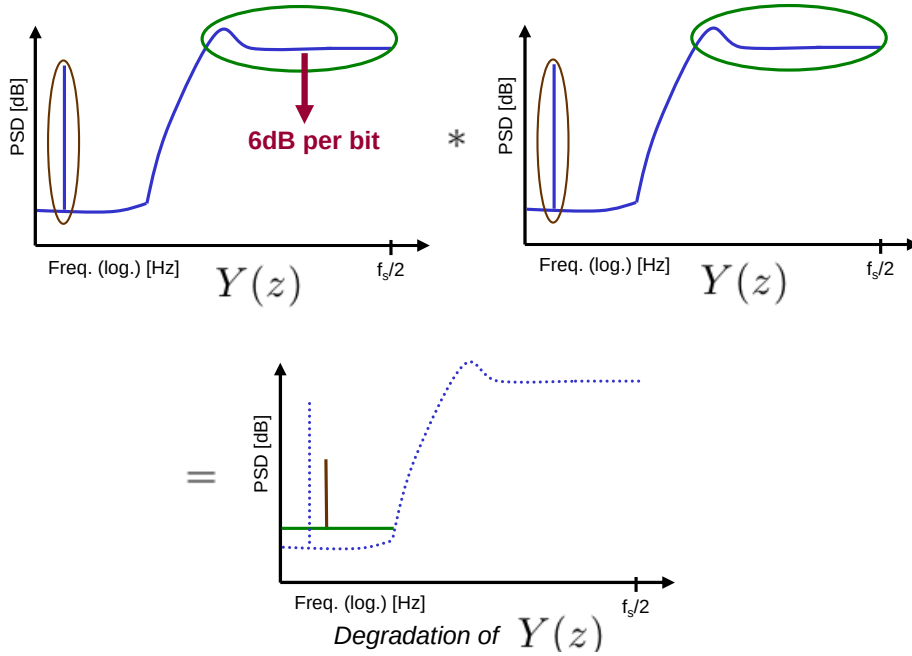


Figure 6.1.: Self-mixing of quantization noise and desired signal due to DAC non-linearity.

to that, the spectral content outside the band of interest can be reduced, because it contains only quantization noise.

One way of doing this is to define the NTF such that it exhibits a low frequency quantization noise peaking which makes the intrinsic high-pass filtering of the NRZ-DACs more effective in suppressing the quantization noise [81, 88]. However, the effectiveness of this approach is limited due to stability constraints for the $\Sigma\Delta$ -modulator loop.

Another way of reducing the high frequency spectral content of the data spectrum $Y(z)$ is to increase the number of quantization levels.

According to (2.3.1), with every additional bit of quantizer resolution, the quantization noise drops by 6 dB¹. However, only single-bit DACs are intrinsically linear, because any mismatch in its two DAC output levels translates into static offset, while the transfer characteristic becomes non-linear for mismatched output levels in multibit DACs. DAC non-linearity results not only in harmonics of the desired signal but also in intermodulation or self-mixing of the high frequency quantization noise into the band of interest (Fig. 6.1).

DAC self-mixing is a very problematic phenomenon in $\Sigma\Delta$ -ADCs, because due to the strong noise shaping only very little non-linearity can be tolerated. In fact, the linearity of the DAC must correspond to the resolution of the whole ADC after the downsampling. Therefore, in high performance multibit CT- $\Sigma\Delta$ -ADCs, excessive circuit area is consumed in order to achieve the required matching [39].

So called Dynamic Element Matching (DEM) by thermometric coding and scrambling of unit elements can be used to linearize the feedback DAC dynamically at the cost of additional noise. For high-performance high-bandwidth ADCs, the additional noise is often unacceptable even if it is high-pass shaped by Data Weighted Averaging (DWA) techniques that are also known as mismatch shaping [10, pp. 186–198].

Hence, in recent years most high performance CT- $\Sigma\Delta$ -ADCs have relied on DAC-linearization by trimming unit elements [41] or by measuring the DAC transfer characteristic and applying the reciprocal transfer characteristic to the bitstream by digital post-processing [61]. However, these calibration techniques are still expensive in terms of power consumption, chip area and production test effort. Moreover, it may require periodic recalibration due to aging effects and temperature or supply voltage variation, which is not possible in all applications².

Background calibration concepts have been proposed in [41, 60] to avoid interfering the DAC operation. However, it remains to be proven that these concepts are reliable in the field under changing operating conditions and

¹ Although often this reduction is partially offset by a more aggressive NTF.

² Analog AM/FM radio broadcast is an example, where interrupting the ADC operation for recalibration can be problematic, because it may result in audible disturbances of the audio signal.

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under the influence of strong and dynamic interfering signals considering the weak pseudo noise test signals that are employed for calibration and the high accuracy that is required.

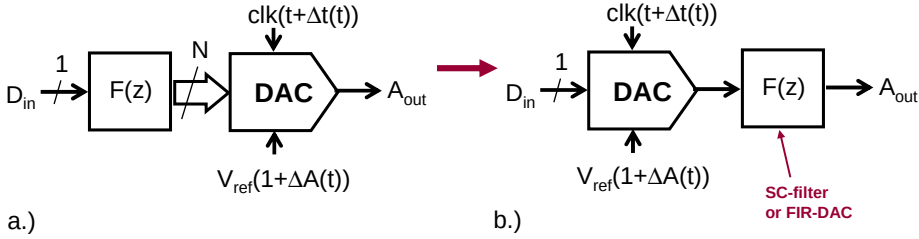


Figure 6.2.: a.) Discrete-time filtering in front of, b.) after or within the DAC.

Instead of increasing the quantizer resolution, the out-of-band quantization noise can also be suppressed by discrete-time low-pass filtering in front of the DAC (Fig. 6.2a). However, this approach is unfavorable, because it increases the number of bits that feed the DAC, which would still require a very linear DAC even though its linearity requirements are relaxed when compared to the multi-bit quantization approach, because self-mixing of the low-pass filtered residual quantization noise is less critical than self-mixing without any preceding filtering.

A better approach than placing the filter in front of the DAC is to place it subsequent to the DAC (Fig. 6.2b) as this allows to operate the DAC with one bit for inherent linearity.

The NRZ pulse shaping is done at the output of the filter if the filter operates in the discrete-time domain which can be achieved by a combination of Switched Capacitor (SC) DAC, SC filter and sample and hold stages to obtain the desired NRZ pulses. In this way very high robustness against jitter can be achieved according to the mechanisms discussed in Section 5.6. For this reason, many HiFi-audio- $\Sigma\Delta$ -DACs on the market use such a SC scheme.

Within a CT- $\Sigma\Delta$ -modulator loop an additional SC filter subsequent to the feedback DAC would increase the circuit complexity and the power consumption of the $\Sigma\Delta$ -modulator. Moreover, the SC filter transfer function would have to be compensated to obtain a stable $\Sigma\Delta$ -modulator loop.

In order to avoid these disadvantages, a simple discrete-time integrator can be selected for $F(z)$ and this filter can be merged into the first integrator of

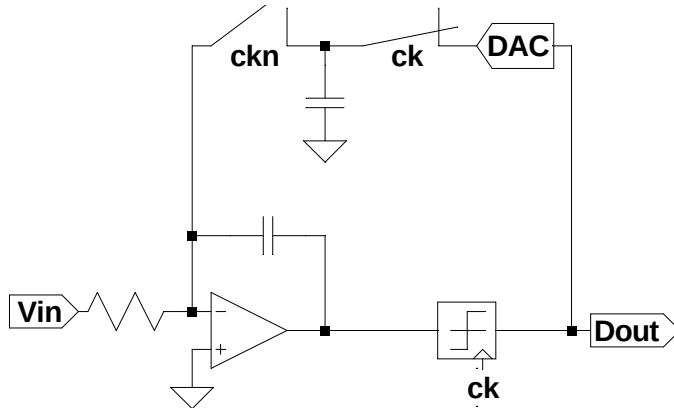


Figure 6.3.: Simplified principle of first order $\Sigma\Delta$ -modulator using a SC-DAC that is driven by non-overlapping clocks ck and ckn .

a standard state-variable loop filter (Fig. 6.3), since continuous and discrete-time integrators differ only in the feed-in network.

Assuming ideal switches and an ideal opamp, the charges of the SC-DAC are transferred via Dirac pulses and the integrator reshapes the Dirac pulses into rectangular NRZ pulses that represent the Discrete-Time (DT) integral of the bitstream. Hence, the jitter folding mechanisms (Fig. 5.5) apply to the signal output of the first integrator, which contains much less high frequency spectral content than the DAC output. Moreover, the undesired result of this folding appears now after the first integrator where it is subject to first-order noise shaping so that the impact of jitter is further reduced.

There is also a simple time domain interpretation of the effect of this so called SC feedback DAC: In contrast to NRZ charge pulses that are injected into the virtual ground of the integrator, the short SC-charge pulses are not bound by clock edges, because they are self-decaying. Hence, timing jitter does not result in charge errors of the injected charge pulses.

However, the drawback of the SC-DAC concept is that the opamp must have more bandwidth and a much higher slew-rate than in the NRZ-DAC case in order to complete the charge transfer from the SC-DAC to the integrator within half of the sampling period.

Due to the higher swing at the virtual ground, the non-ideal opamp needs to be more linear in order to avoid increased distortion of the continuous time input signal. This effect can be mitigated to some extent either by using

the so called Switched Capacitor Resistor (SCR)-DAC approach [89] although the same effect can be achieved reducing the width over length of the CMOS passgate switches to increase their on resistance, or by using a transistor-based self-decaying DAC [90].

Nevertheless, higher opamp bandwidth and linearity requirements translate into higher power consumption. Moreover, the SC-DAC concept is more susceptible to jitter due to finite opamp GBW [91] and to the reference noise folding mechanism discussed in Chapter 5.

In fact, it even increases the sensitivity to high frequency reference noise, because the reference noise is effectively sampled which means that the *sinc* filter term in (5.6.1) becomes unity³.

6.2 Finite-Impulse-Response-DAC

The so called FIR-DAC [82, 87, 92] is an elegant alternative for discrete-time filtering after or within the DAC that is more robust to reference noise and more power-efficient. In Fig. 6.4a a digital low-pass FIR-filter is placed in front of a DAC in order to suppress the high frequency quantization noise. This improves the robustness to jitter and reference noise, but the inherent linearity of the single-bit DAC is lost, because the FIR-filter increases the number of bits from one at its input to M at its output.

Both the ideal D/A conversion and the digital summation within the FIR-filter are linear operations that can be rearranged according to 6.4b in order to obtain a FIR-DAC. In this way, perfect linearity is maintained, because only inherently linear single-bit DACs are employed. Mismatch of the DAC elements in terms of conversion gain and offset only causes static offset and modifies the coefficients $b_0, \dots, b_n$ of the FIR-DAC, whereas mismatch of the DAC elements of thermometric encoded standard multi-bit DACs results in a non-linear transfer characteristic.

The main functional difference with respect to linearity between a FIR and a multi-bit DAC is that the individual DAC elements convert different ranges of the input signal. In the FIR case, each element converts the full-scale range

³ Assuming ideal opamps and switches, otherwise the reference noise is subject to first order low pass suppression due to settling time constants before it is sampled.

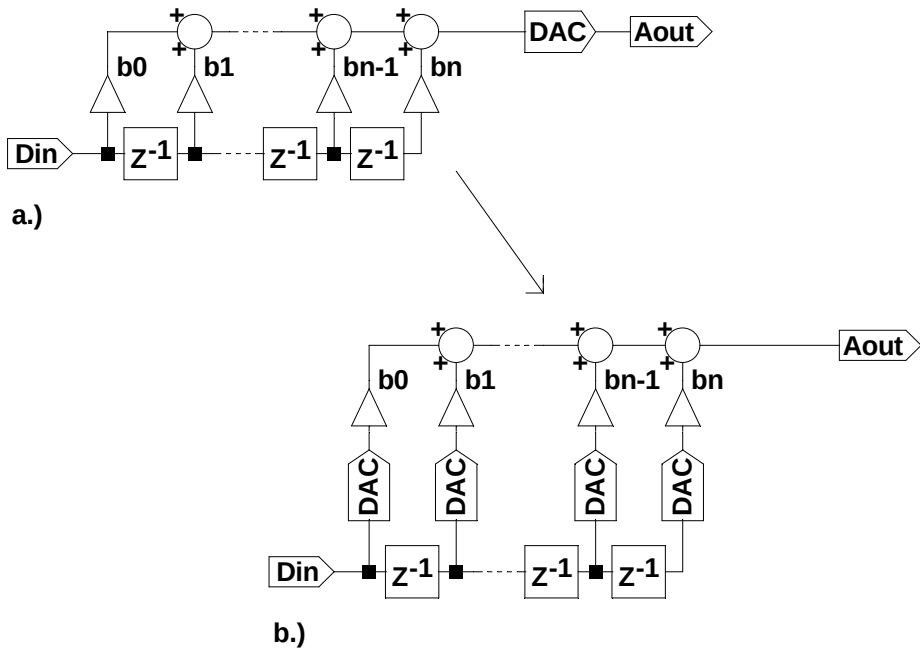


Figure 6.4.: a.) FIR-filter with subsequent DAC, b.) equivalent FIR-DAC.

and in the multi-bit case each element converts only a part of the full-scale range. Hence, any mismatch of the DAC elements in a FIR-DAC affects the entire input signal in the same linear way, whereas mismatch in the multi-bit DAC modifies the input signal depending on its momentaneous value, which causes distortion.

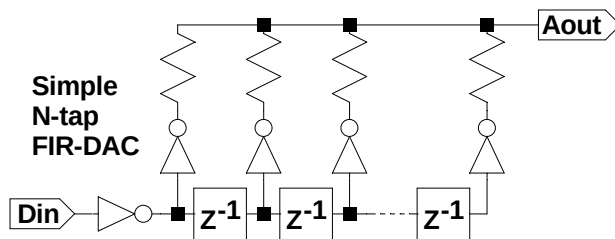


Figure 6.5.: Most simple FIR-DAC implementation.

6. Extrinsic-Noise-Tolerant DACs

FIR-DACs are often implemented with moving-average FIR-filter transfer functions with equal coefficients

$$b_0 = b_1 = \dots = b_n. \quad (6.2.1)$$

In this case all DACs have the same nominal conversion gain, they share the same reference voltage and they are clocked by the same sampling clock. Consequently, both the desired data pulses and the error pulses due to jitter and reference noise that all have implicitly equal height and width superimpose constructively or destructively at the summation stage, i.e. errors of delayed NRZ pulses with opposite sign cancel.

The more often the data changes, the more errors are eliminated. Hence, in $\Sigma\Delta$ -modulators the errors due to folding with out-of-band quantization noise are strongly reduced.

In Fig. 6.5 the most simple implementation of a FIR-DAC is shown. Its DAC elements each consist of an inverter and a resistor. The reference voltage V_{ref} is half the supply voltage of the inverters and the output voltage A_{out} has an offset equal to V_{ref} and an impedance that corresponds to the equivalent resistance of the parallel connection of all resistors.

6.3 FIR-DAC Compensation

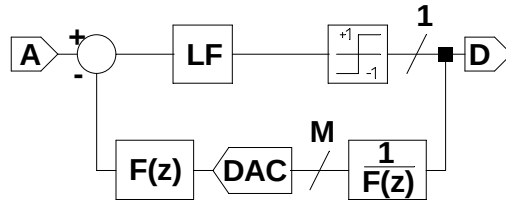


Figure 6.6.: Serial compensation of FIR-DAC transfer function.

For a stable $\Sigma\Delta$ -modulator, the FIR-DAC transfer function $F(z)$ in the feedback loop needs to be compensated. Compensating $F(z)$ serially by $1/F(z)$ (Fig. 6.6) is a nonviable solution, because the additional $1/F(z)$ IIR-filter increases the bus width and despite a single-bit quantizer, there is still an M-bit DAC required that is prone to non-linearity.

Moreover, the $1/F(z)$ IIR-filter strongly increases the spectral content of the out-of-band quantization noise. The same spectral content as at the output of the quantizer can be observed after the subsequent $F(z)$ filtering. Hence, in total there is no reduction of reference and jitter-induced noise and the result is the same as for a standard single-bit DAC.

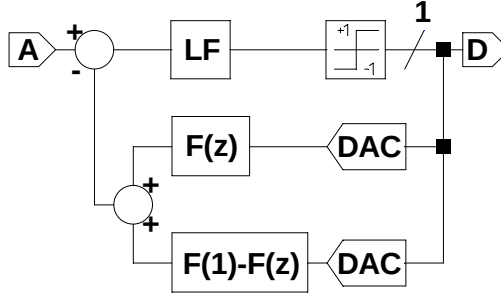


Figure 6.7.: Parallel compensation of FIR-DAC transfer function.

Compensating the FIR-DAC transfer function $F(z)$ by a parallel path in Fig. 6.7 allows to use only inherently linear single-bit DACs, because the $F(1) - F(z)$ filter in the compensation path can be implemented by a FIR-DAC as well.

The transfer function of the FIR-DAC in the $F(z)$ low-pass path is fully compensated by the $F(1) - F(z)$ high-pass path and the structure in total represents a standard NRZ-DAC. So far, there is no benefit of this structure with respect to reference noise and jitter robustness. In the next sections, modifications to the concepts of parallel compensation will be proposed that overcome this dilemma of FIR-DAC compensation.

6.4 Jitter-Noise-Reduction-DAC

FIR-DAC compensation can be done with the JNR-DAC scheme depicted in Fig. 6.8. A block level diagram of its implementation is depicted in Fig. 6.9, where the definition and summation of the FIR coefficients and the high-pass filtering is hidden within an analog CT Multiple Input Single Output (MISO) filter block. The JNR-DAC concept has been implemented in both testchips that will be discussed in Chapters 7 and 8 [69, 93].

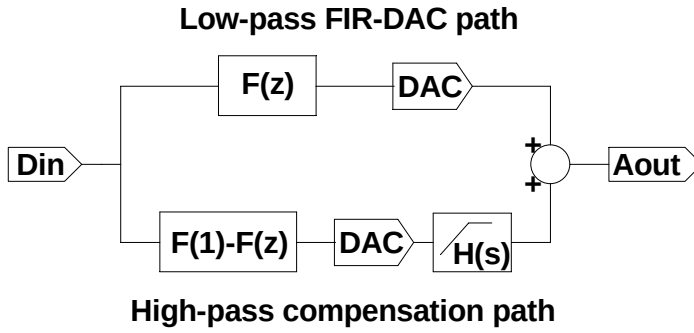


Figure 6.8.: Concept of Jitter Noise Reduction (JNR)-DAC.

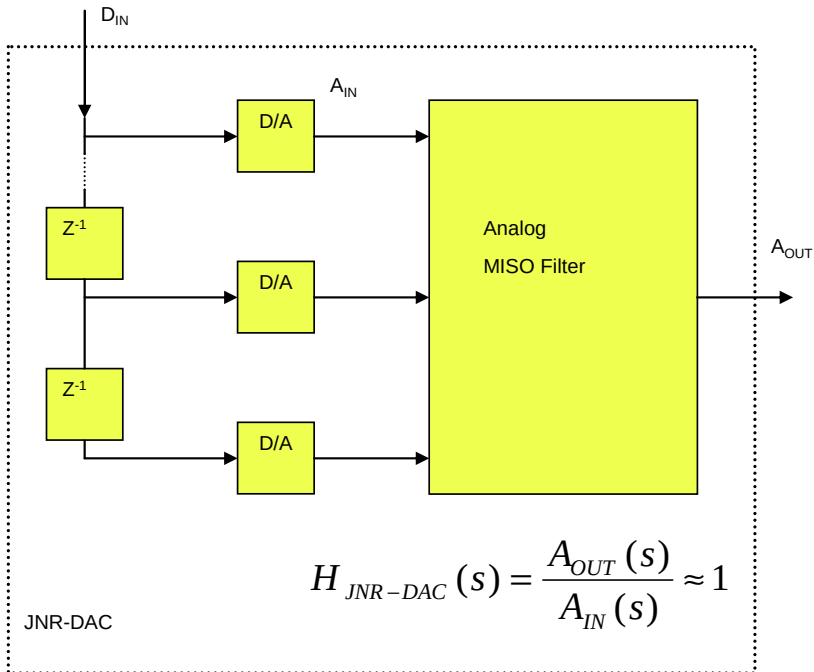


Figure 6.9.: Implementation of JNR-DAC.

For $H(s) = 1$, the transfer function of the FIR-DAC in the low-pass path is fully compensated by the high-pass path and the structure in Fig. 6.8 rep-

represents a standard NRZ-DAC without any reduction of jitter- and reference-induced noise at its output. Most of this output noise must be contributed by the high-pass path $F(1) - F(z)$ because the low-pass path $F(z)$ suppresses jitter- and reference-induced noise significantly according to the discussions in Chapter 5. It can be suppressed also in the high-pass path with an additional analog high-pass filter $H(s)$. Choosing a lower corner frequency for $H(s)$ than for $F(1) - F(z)$ ensures that the total transfer function of the JNR-DAC is almost the same as for a standard NRZ-DAC. The FIR-DAC transfer function $F(z)$ may also incorporate a delay for reduced effect of quantizer-metastability [53].

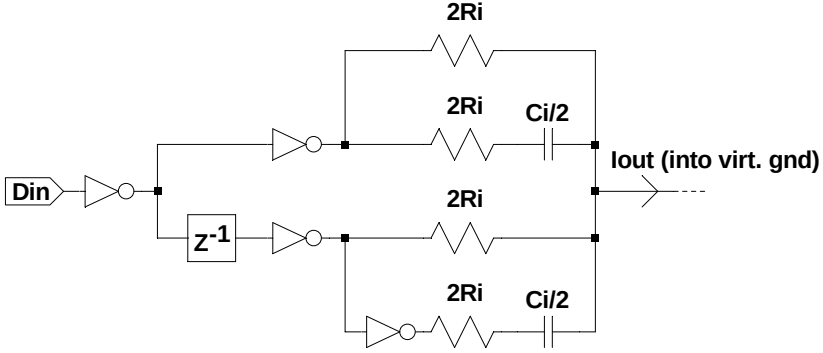


Figure 6.10.: Minimalistic JNR-DAC implementation.

Fig. 6.10 depicts the most simple implementation of a JNR-DAC. Its low-pass FIR-DAC transfer function is

$$F(z) = (1 + z^{-1})/(2R_i) \quad (6.4.1)$$

and its high-pass transfer function is

$$F(z) = (1 - z^{-1})/(2R_i) \quad (6.4.2)$$

accordingly. The FIR coefficients are defined by the impedance of two resistors and two first-order RC-high-pass feed-in paths that inject currents into a common node. The virtual ground node of an integrator or an amplifier can be used as a common node in order to decouple the individual branch currents. The corner frequency f_c of the RC-high-pass filter becomes

$$f_c = 1/(2\pi R_i C_i). \quad (6.4.3)$$

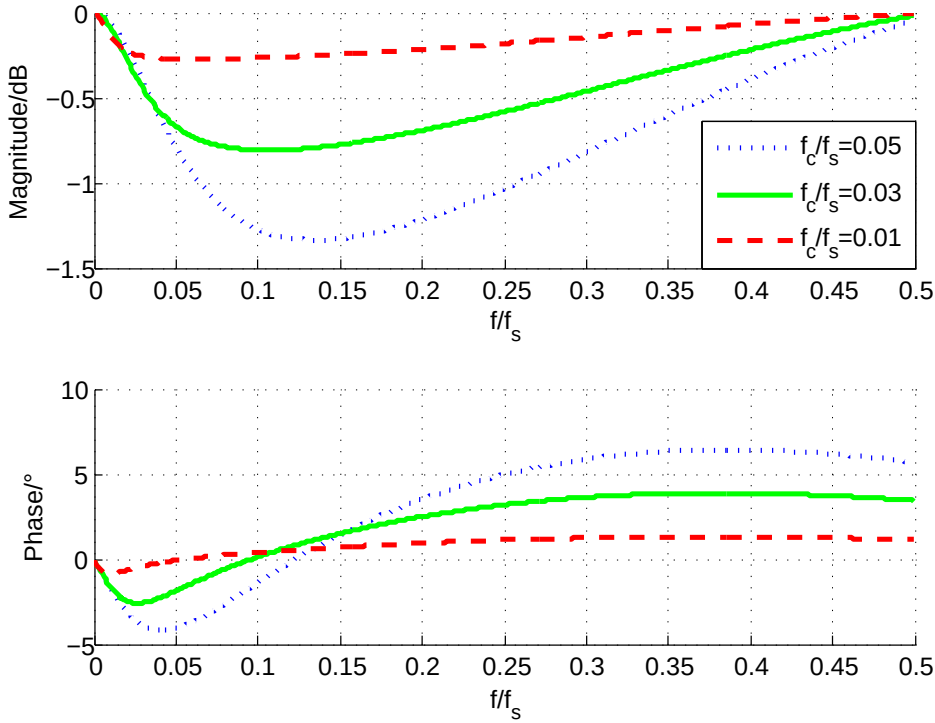


Figure 6.11.: Transfer function of minimalistic JNR-DAC for different corner frequencies f_c of continuous-time high-pass filter.

Fig. 6.11 depicts the transfer function of this minimalistic JNR-DAC for different corner frequencies f_c . These transfer functions do not incorporate the *sinc* function due to the NRZ pulse shaping.

Hence, the ideal transfer function to compare those plots with is unity. Fig. 6.12 shows the maximum deviation from the ideal transfer function of the JNR-DAC versus the corner frequency f_c of the continuous-time high-pass filter.

Fig. 6.13 shows the noise floor of a CT- $\Sigma\Delta$ -ADC for audio applications using a standard NRZ feedback DAC versus a 7-tap JNR feedback DAC with $f_c = f_s/100$. These harmonic balance noise simulation results illustrate the effect of the JNR-DAC in the presence of jitter- and reference-induced noise.

The JNR-DAC is useful mainly for $\Sigma\Delta$ -ADCs with high OSR because for a high suppression of the jitter-induced noise, $F(z)$ must have a low corner fre-

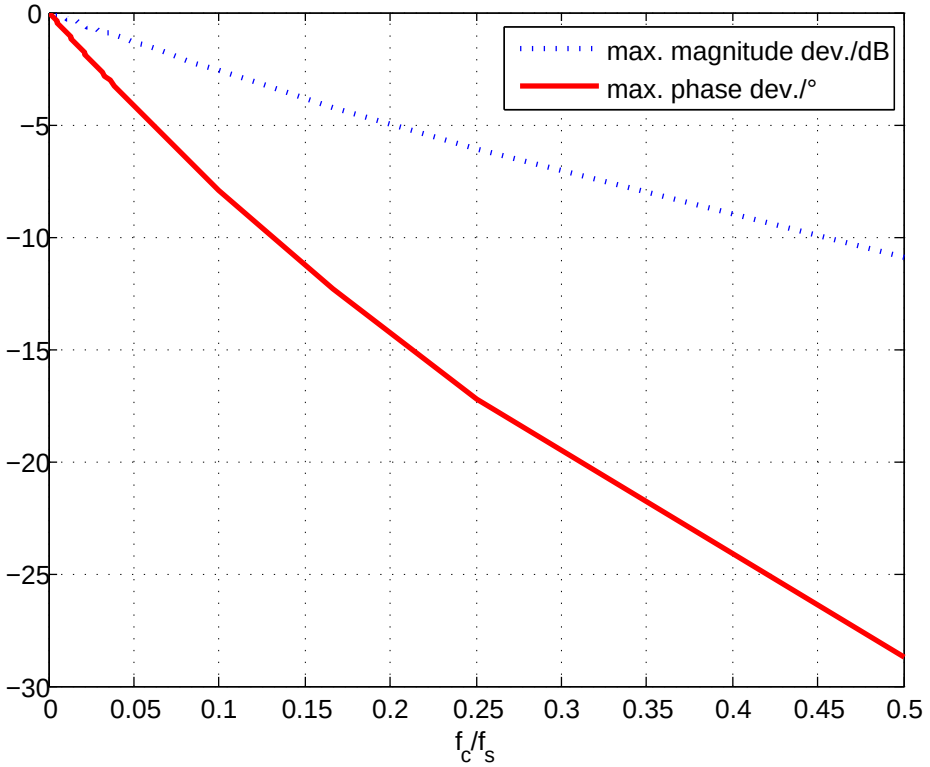


Figure 6.12.: Maximum deviation from ideal transfer function of minimalistic JNR-DAC versus corner frequency f_c of high-pass filter.

quency which in turn requires $H(s)$ to have an even lower corner frequency. Finally, the bandwidth of interest of the ADC must be considerably smaller than that corner frequency for a high attenuation of $H(s)$.

A further drawback is that the same level of high-frequency quantization noise must be processed in the loop filter as for a standard single-bit NRZ-DAC. In [83], a similar concept has been proposed, where most of the high-frequency quantization noise has been processed in a path parallel to the first integrators of the loop filter.

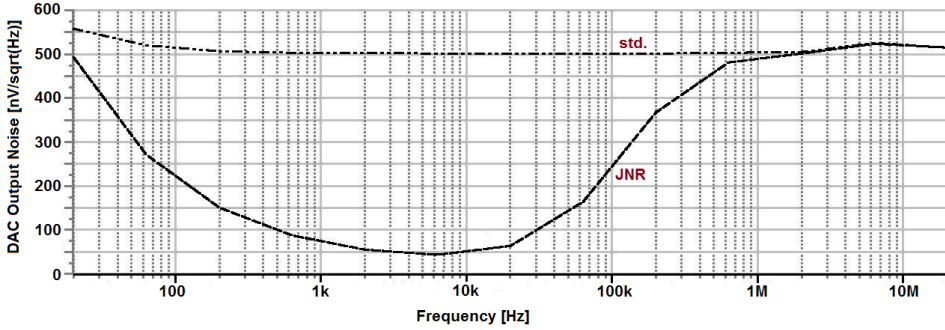


Figure 6.13.: Jitter- and reference-induced output noise of standard NRZ-DAC and JNR-DAC.

However, the same limitation to high OSR applies and this approach demands extra power consumption and circuit area for the parallel path as well as sufficient matching of the main and the parallel path. A novel alternative that works well also with a lower OSR will be discussed in the next section.

6.5 Infinite-Impulse-Response-Quantizer

In previous designs [83, 94], the compensation of the FIR-DAC has been done partly in the continuous-time domain within the loop filter. The drawback of such a compensation is that the loop filter still has to process the strong high frequency single-bit quantization noise. A solution has been proposed in [95], where the loop filter opamps were unburdened from the high frequency quantization noise by a loop around a current-DAC-C integrator and the quantizer.

In [93], passive discrete-time FIR compensation by a local loop around the quantizer has been proposed by the author instead. In this regard the proposed concept is similar to the noise-coupled $\Sigma\Delta$ -modulator [96]. However, in contrast to the noise coupled $\Sigma\Delta$ -modulator it does not require power hungry SC circuitry.

It improves suppression of jitter-induced noise in the FIR-DAC while maintaining a low power consumption. In this way, the loop filter has to process only the slow low-pass FIR-filtered feedback signal, while the high-frequency quantization noise is fed back passively to the quantizer input.

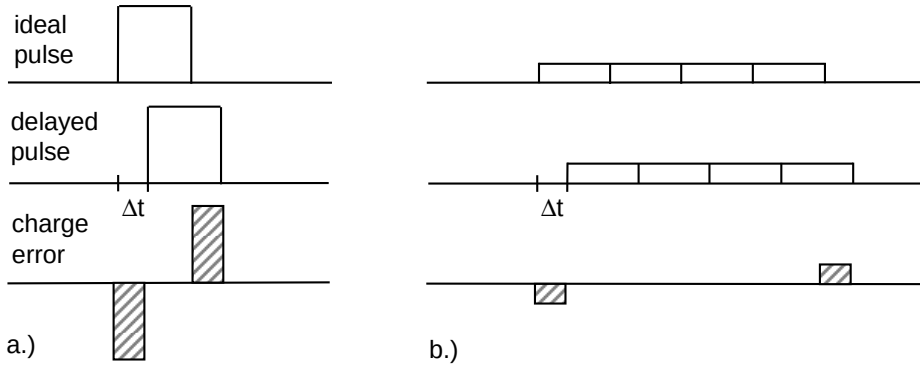


Figure 6.14.: a.) Impulse responses and delay-induced charge-errors of a.) std. NRZ-DAC and b.) moving-average FIR-DAC with equal DC conversion gain $F(1)$.

Significant ELD can be tolerated in the slow loop. This can be understood best in the time domain: ELD results in error pulses at the beginning and at the end of the DAC impulse response; these charge errors decrease with increasing length of the FIR-DAC impulse response (Fig. 6.14).

Consequently, moderate ELD caused by finite opamp-GBW and moderate deliberately introduced delay to mitigate quantizer metastability [53, 97] have no significant impact on the stability of the modulator. In general, the more high frequency quantization noise is suppressed in the slow loop, the more ELD can be tolerated.

6.6 Single-Bit-Modulator Interpretation

An intuitive design method for the coefficients of DAC 2 in Fig. 6.15 can be found by interpreting the compensation loop together with DAC 1 as a direct-form-2 IIR-filter with an embedded quantizer.

6. Extrinsic-Noise-Tolerant DACs

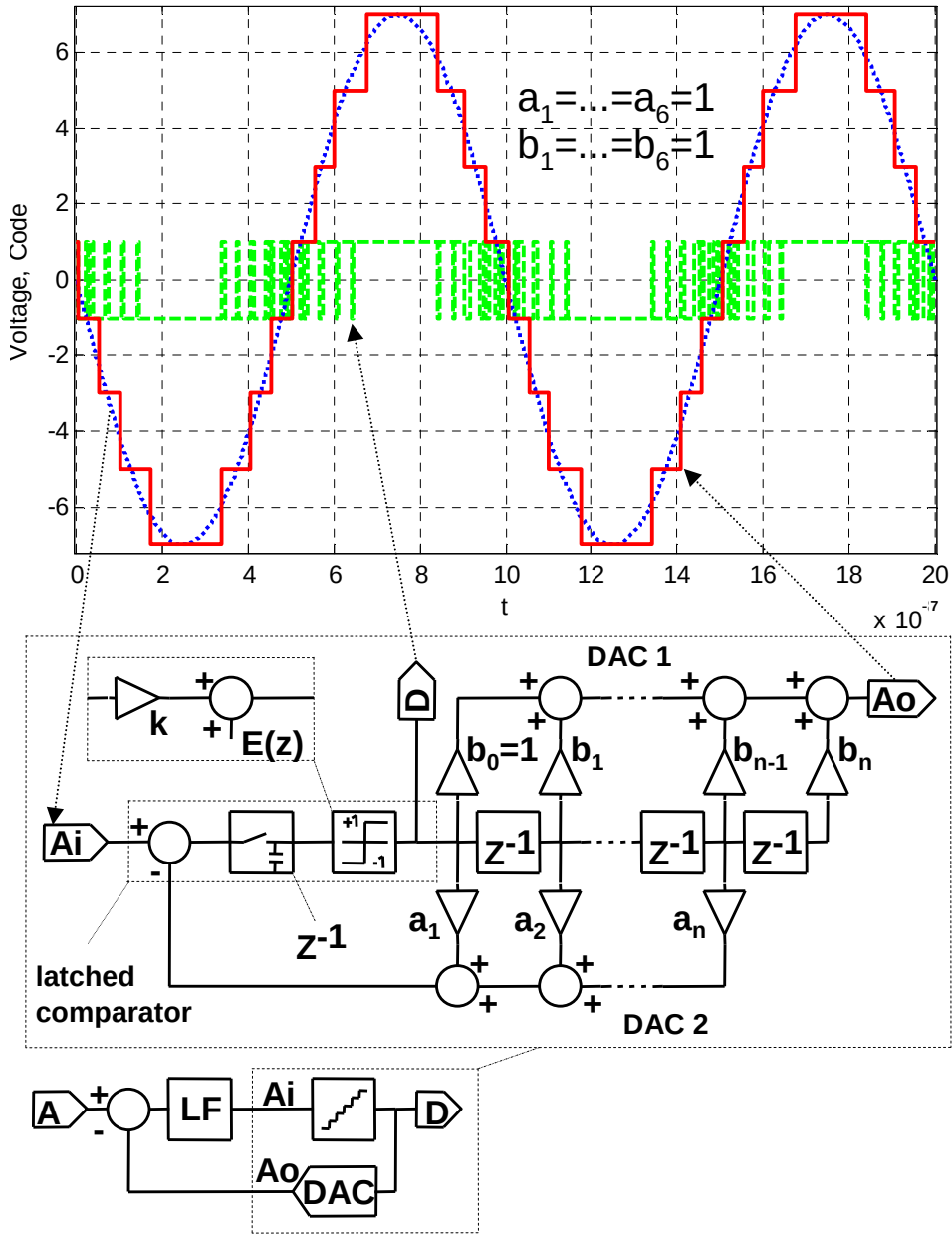


Figure 6.15.: Block diagram of the IIR-quantizer with waveforms.

The small-signal transfer function of this filter becomes

$$\frac{A_o(z)}{A_i(z)} = \frac{1 + b_1 z^{-1} + \dots + b_n z^{-n}}{1/k + a_1 z^{-1} + \dots + a_n z^{-n}} \quad (6.6.1)$$

where the coefficients $b_0, \dots, b_n$ represent the taps of FIR-DAC 1, while $a_1, \dots, a_n$ represent those of FIR-DAC 2. The transfer function of this IIR-quantizer becomes equal to the linearized quantizer gain k under the conditions $a_1 = b_1/k, \dots, a_n = b_n/k$.

Thus, the coefficients of DAC 2 can be defined to fully compensate the FIR transfer function of DAC 1, if the exact value of the quantizer gain k is known a priori. The loop filter of the $\Sigma\Delta$ -ADC can then be designed with the same transfer function as for a standard single-bit prototype modulator.

However, for a single-bit quantizer k depends on signal statistics. In the standard single-bit modulator, the loop filter gain can be scaled arbitrarily, because the non-linear feedback loop will adjust the linearized quantizer gain k such that the small-signal open loop transfer function remains constant for a given ADC input signal level. However, with an IIR-quantizer, there is only one optimum loop filter gain scaling factor, because k is already defined implicitly by the coefficients of DAC 2.

Therefore, designing a $\Sigma\Delta$ -modulator with an IIR-quantizer is similar to designing a multi-bit modulator, where the linearized quantizer gain k is also defined a priori by the LSB-step-size of the flash quantizer. Without a negative impact on the achievable system performance, it is save to first assume an arbitrary value of k (e.g. $k = 1$) to define the coefficients of DAC 2 and then to find the optimum value of the loop filter gain scaling factor for the chosen value of k .

6.7 Multi-Bit-Modulator Interpretation

The IIR-filter interpretation yields another remarkable property of this structure: For unity coefficients $b_0, \dots, b_n$, the proposed IIR-quantizer in Fig. 6.15 monotonously tracks signals similar to a quantizer with $n + 2$ levels. In other words, a moving-average FIR-filter with length $n + 1$ is the optimum decoder for a bitstream encoder that consists of a Δ -modulator based on a moving-average FIR-loop-filter with length n .

The quantization noise of the Δ -modulator is concentrated exactly at the notches of the decoding FIR-filter (Fig. 6.16). This minimizes the residual

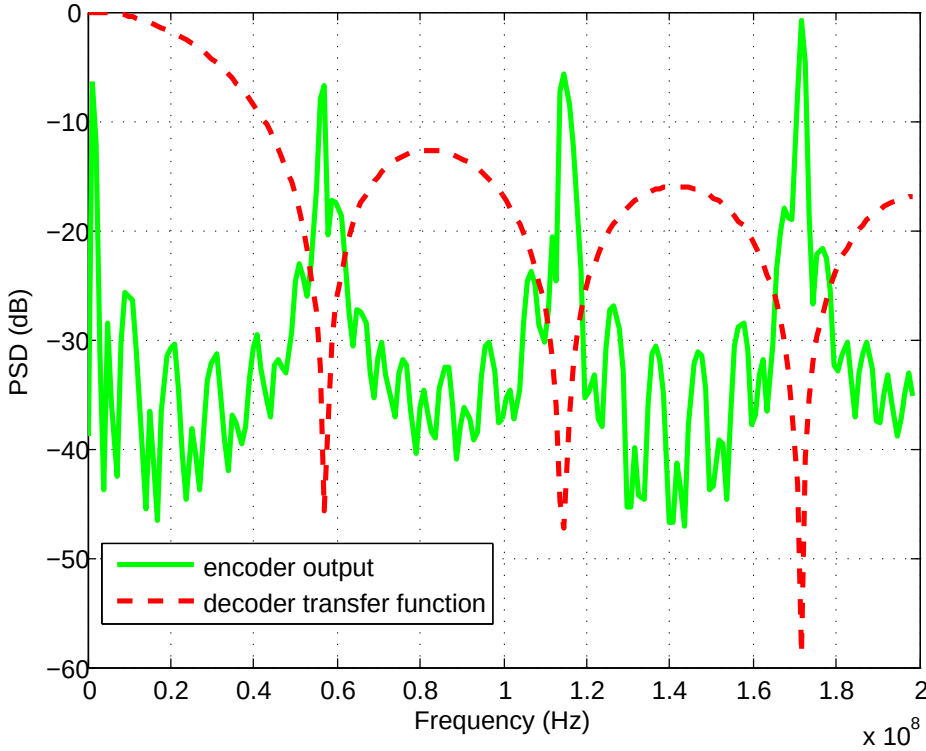


Figure 6.16.: PSD of IIR-quantizer bitstream output and transfer function of moving-average FIR-DAC decoder.

quantization noise at the output of the decoder. In previous CT- $\Sigma\Delta$ -ADCs that incorporated FIR-DACs, there has been no such matching of the shape of the quantization noise and the FIR-DAC transfer function. For this reason, CT- $\Sigma\Delta$ -ADCs implemented with an IIR-quantizer can achieve better clock-jitter immunity and lower loop filter linearity requirements than previous solutions.

However, in contrast to a flash quantizer, this IIR-quantizer is subject to slew-rate limitation, because its output code can change only by ± 2 per clock cycle. Therefore, the IIR-quantizer can be regarded as an efficient and highly linear implementation of a tracking ADC.

In [98–101] it has been already shown that tracking-ADCs are well suited for replacing a flash-quantizer within a multi-bit- $\Sigma\Delta$ -ADC, because the out-of-band quantization noise is usually much smaller than the maximum in-band signal at the input of the quantizer. The IIR-quantizer allows to do this in a more elegant way, because it does not need any DAC linearization due to the inherent linearity of its FIR-DACs.

In fact, using internal oversampling in the IIR-quantizer to avoid slew-rate distortion enables full substitution of a $n + 2$ -level flash quantizer and thermometric DAC with the same level of performance and clock jitter sensitivity, but with perfect quantizer and DAC linearity and smaller circuit complexity. The quantization noise introduced by a $n + 2$ -level IIR-quantizer with internal oversampling is even lower than the quantization noise of a $n + 2$ -level flash quantizer due to the higher timing resolution.

In addition and unlike the solution presented in [102], the anti-aliasing is improved due to the higher sampling frequency. Greatly relaxed matching requirements with this concept translate into significantly smaller circuits without the need for calibration.

Starting with a standard $n + 2$ -level flash-quantizer-based prototype design, a modulator with an IIR-quantizer can be derived by replacing the quantizer and simulating it with successively decreasing internal OSR until the same peak SNR is obtained as in the prototype. Strong out-of-band interferers may require to increase the internal OSR again due to the inherent slew-rate limitation of the IIR-quantizer.

The IIR-quantizer concept also works with multi-bit-quantization within the embedded Δ -modulator. However, only single-bit FIR-DACs are inherently linear.

6.8 Non-Moving-Average FIR-DAC Coefficients

For $a_1 = b_1/k, \dots, a_n = b_n/k$, the internal STF and NTF of the Δ -modulator within the IIR-quantizer becomes

$$\frac{D(z)}{A_i(z)} = \frac{kD(z)}{E(z)} = \frac{k}{1 + b_1z^{-1} + \dots + b_nz^{-n}}. \quad (6.8.1)$$

This high-pass transfer function can be compensated in the digital domain by a reciprocal FIR-filter. However, mismatch of the analog FIR coefficients

6. Extrinsic-Noise-Tolerant DACs

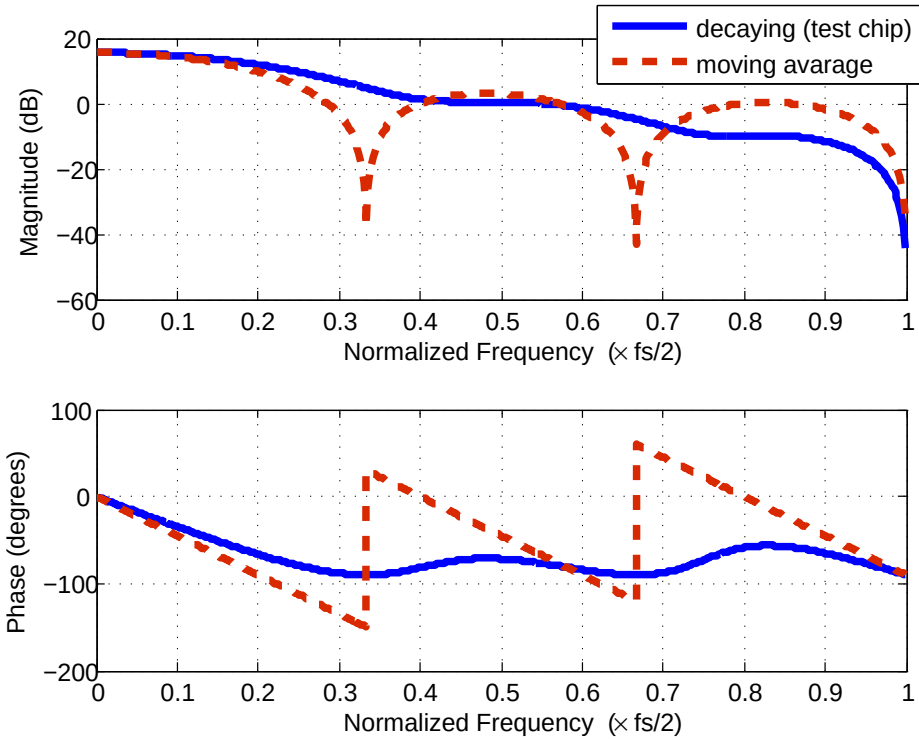


Figure 6.17.: Transfer functions of decaying and moving average FIR-DACs.

within the IIR-quantizer and variations of the linearized quantizer gain k lead to imperfect compensation. This and the slew-rate limitation of the IIR-quantizer can be problematic if strong out-of-band interferers are present; especially if they are located at the notch frequencies of the decoding FIR-filter.

The IIR-quantizer can be implemented with non-moving-average FIR-DAC coefficients as well. Good results have been obtained with decaying impulse responses with different roll-offs. Empirically, it has been found that for any type of FIR-filter, the coefficients should satisfy $b_0 = 1$ and $b_1 + \dots + b_n = n$ to obtain minimum quantization noise power. The transfer function of DAC 1 in the mostly-digital testchip 2 that will be discussed in Chapter 8 is

$$\frac{A_o(z)}{D(z)} = 1 + \frac{5z^{-1} + 4z^{-2} + 3z^{-3} + 2z^{-4} + z^{-5}}{3}. \quad (6.8.2)$$

6.8. Non-Moving-Average FIR-DAC Coefficients

This filter significantly suppresses high frequency quantization noise for high immunity against clock jitter and low loop filter linearity requirements (Fig. 6.17). Also a better robustness to out-of-band interferers is obtained, because it has only one notch at $f_s/2$ and it yields a higher slew-rate than a moving-average transfer function of the same order.

7 Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

CT- $\Sigma\Delta$ -ADCs with medium to low OSRs are designed with NTFs containing conjugate complex zeros to extend the usable bandwidth. Traditionally, these zeros are implemented with a resonance generated by feedback around two integrators.

In Chapter 3 a differential single-opamp resonator with cross-coupled feedback has been presented that allows to reduce the number of opamps in the loop filter. This solution is more compact, more power-efficient, more robust and more linear than previous single-opamp resonators [68].

In Chapter 6 an NRZ-DAC that reduces jitter-induced noise has been discussed. This concept allows to improve the clock jitter robustness of single-bit modulators without having to employ large and complex multi-bit quantization or self-decaying pulse shaping that would increase the loop filter power dissipation.

In this chapter, a ninth-order CT- $\Sigma\Delta$ -ADC in 350 nm CMOS is presented that has been implemented as a first mostly-analog testchip to prove these concepts. Thanks to the novel concepts and a novel compact low power gain stage for the feed-forward compensation network, this jitter-robust modulator could be implemented with only five instead of ten opamps in the conventional feed-forward state variable loop filter topology [69].

7.1 Concept of Testchip

$\Sigma\Delta$ -ADCs and DACs are well suited for digital control loops with high requirements to the control accuracy due to their high resolution. Latency within a control loop is critical for loop stability. The latency within the control loop illustrated in Fig. 7.1 is caused not only by the computation in the

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

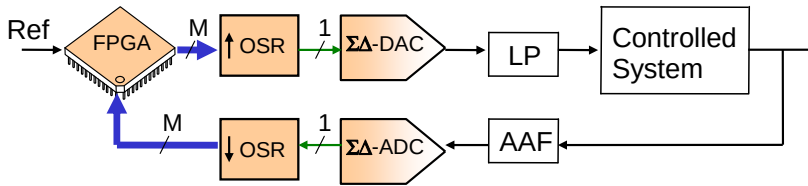


Figure 7.1.: Digital control loop.

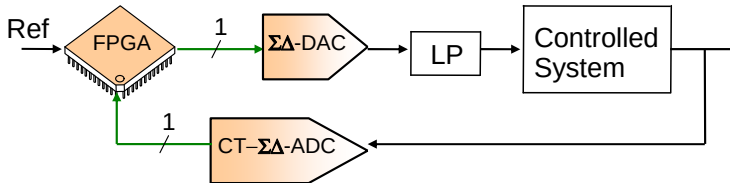


Figure 7.2.: Digital control loop operating with oversampled data.

DSP but also by the decimation, the interpolation, the reconstruction filter and the anti-alias filter stages. Some of these contributions can be eliminated if the controller operates directly with the oversampled data (Fig. 7.2).

As a further benefit, the inherent anti-alias filtering of a CT- $\Sigma\Delta$ -ADC allows to omit a separate anti-alias filter for reduced system complexity.

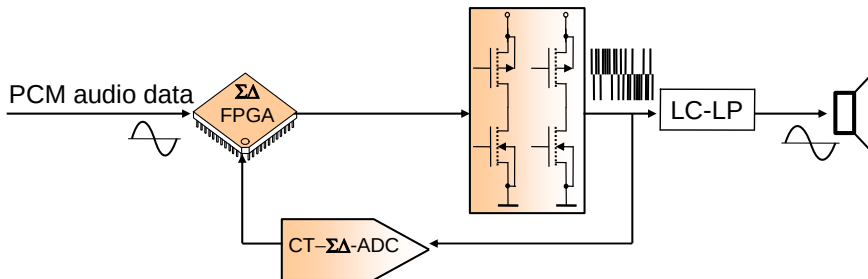


Figure 7.3.: Feedback linearized Class-D amplifier.

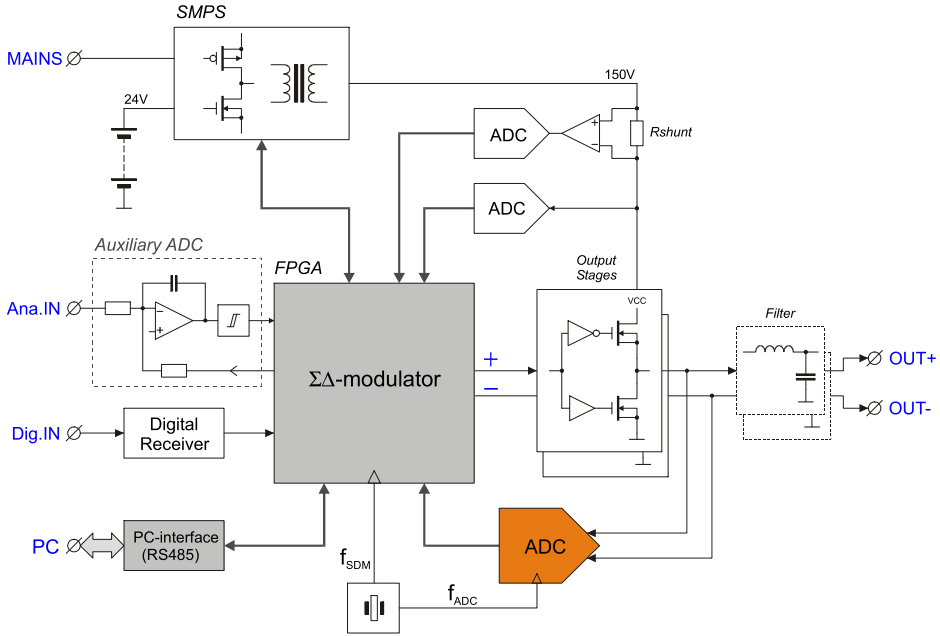


Figure 7.4.: Linearized $\Sigma\Delta$ modulated Class-D amplifier [103].

An example of such a loop is a digital $\Sigma\Delta$ modulated Class-D power amplifier with feedback linearized power stage (Fig. 7.3) [104, 105]. A block diagram of the complete system is shown in Fig. 7.4.

There are no suitable high-resolution CT- $\Sigma\Delta$ -ADCs on the market that provide low-latency access to the undecimated bitstream. Hence, such an ADC testchip has been designed for a feedback linearized Class-D power amplifier project at the circuit design laboratory of the University of Applied Sciences Munich [103, 106].

With later volume production in mind, the ADC has been implemented with the smallest possible chip area in a low cost 350 nm CMOS process. Single-bit converters can be implemented more compact than multi-bit converters, because they are much more robust to component mismatch. Also the circuit complexity reduces significantly which results in a mostly-analog chip with only a small number of digital gates and simple interfaces. Therefore, a single-bit converter has been implemented for this project.

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

CT- $\Sigma\Delta$ -ADCs and in particular those with single-bit quantization are very sensitive to clock jitter. Thus, several methods to reduce the influence of jitter have been implemented. One of them is the modulator design with low OBG denoted by the parameter H_∞ which is also a design parameter in Schreier's $\Sigma\Delta$ toolbox [27].

7.2 Loop Filter

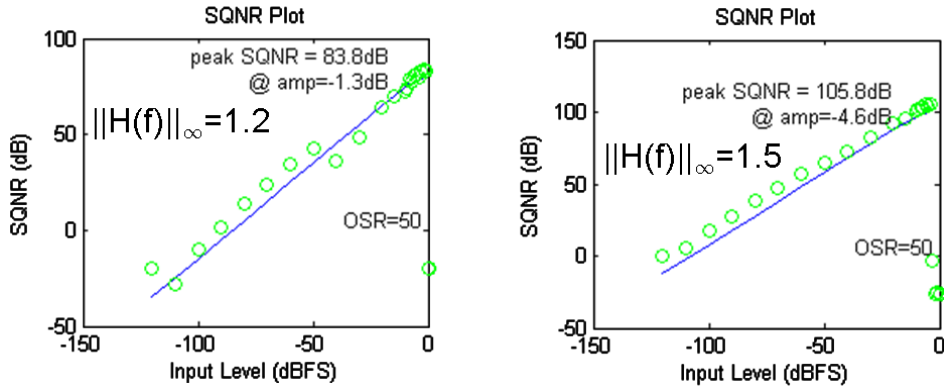


Figure 7.5.: Peak SQNR of a fifth order single-bit modulator for different values of the design parameter $H_\infty = \|H(f)\|_\infty$.

Reducing H_∞ yields a higher MSA. For example, the converter in Fig. 7.5 with $H_\infty = 1.2$ can tolerate an input level that is higher by 3.3 dB than the same converter with $H_\infty = 1.5$.

For a given target SNRp of the signal chain that contains the ADC, a higher maximum input level at the ADC allows to place a gain stage in front of it. In this way, a higher absolute level of the thermal and jitter-induced noise floor can be tolerated at the ADC. The downside of this approach is that the in-band quantization noise also rises sharply with reduced OBG as can be seen from the Peak Signal to Quantization Noise Ratio (SQNRp) values in Fig. 7.5. Hence, the order of the noise shaping has to be increased in order to avoid that the quantization noise is becoming the dominant contributor to the overall noise floor of the ADC.

In the standard state variable loop filter topology increasing the order of the noise shaping requires additional opamps, which degrades the power-

efficiency and increases the chip size. Although, considering the target application, a higher robustness to jitter clearly has been a more important design goal than a higher power-efficiency of the ADC, measures have been implemented to compensate the negative impact of the low OBG on the power-efficiency and chip size.

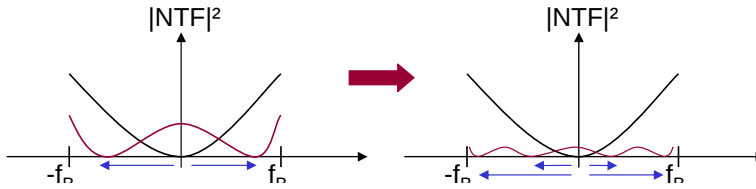


Figure 7.6.: Increasing the number of NTF zeros for SQNR optimization.

One can reduce the in-band quantization noise by optimizing the zeros of the noise transfer function. The number of available zeros for this optimization is limited by the order of the modulator. For example, in a fifth order modulator only one zero at the origin and two complex conjugate pairs of zeros are available. Thus, one research aim of this mostly-analog testchip has been to increase the number of complex conjugate pairs of zeros, without increasing the number of opamps (Fig. 7.6). This ultimately increases also the order of the loop filter.

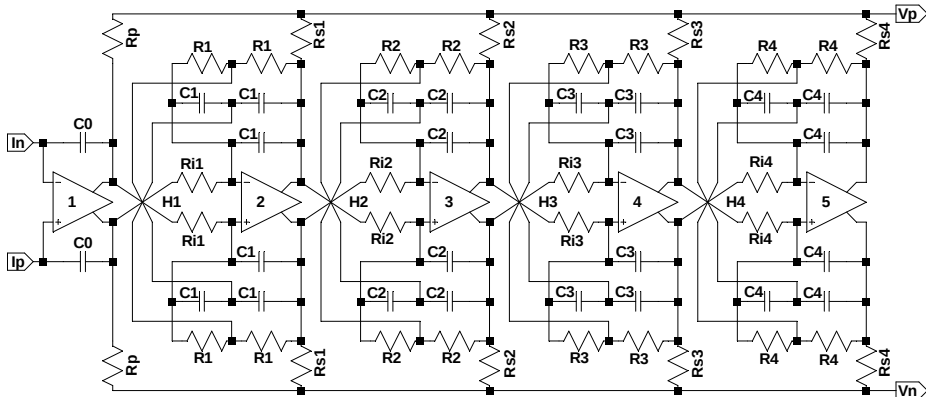


Figure 7.7.: Ninth-order loop filter configuration.

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

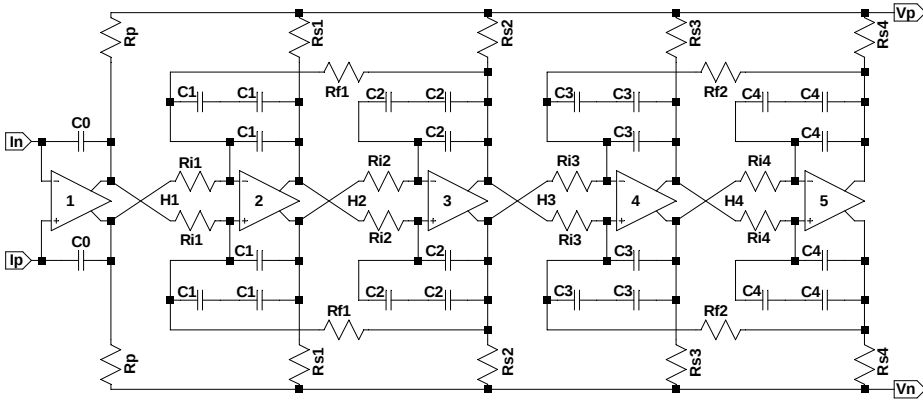


Figure 7.8.: Fifth-order loop filter configuration.

To put it another way, lowering H_∞ requires to increase the order of the NTF to maintain low in-band quantization noise. The desired SQNR_p of 100 dB at an OSR of 55 and $H_\infty = 1.2$ requires a ninth-order NTF.

The corresponding ninth-order loop filter has been implemented using one standard integrator and a subsequent cascade of four cross-coupled resonators (Fig. 7.7) in order to obtain one pole at the origin of the s -plane and four pairs of conjugate imaginary poles. Placing a standard integrator at the input of the loop filter has the advantage of low offset contribution of subsequent stages and low in-band thermal noise due to the strong low frequency gain of the integrator.

The numerator polynomial of the loop filter V/I^1 transfer function $Z_{LF}(s)$ has been defined by the bypass method presented in 3.6. However, for reduced number of components, this method has been extended to obtain an eighth order numerator polynomial by bypassing a chain of the four resonators $H_{1...4}(s)$:

¹ Transfer function is normalized to the impedance of the feed-in network.

$$Z_{LF}(s) = \frac{V(s)}{I(s)} = \frac{AR_{||}}{sC_0} \left(\frac{1}{R_p} + \frac{H_1(s)}{R_{s1}} + \frac{H_1(s)H_2(s)}{R_{s2}} + \frac{H_1(s)H_2(s)H_3(s)}{R_{s3}} + \frac{H_1(s)H_2(s)H_3(s)H_4(s)}{R_{s4}} \right) \quad (7.2.1)$$

where

$$R_{||} = \left(\frac{1}{R_p} + \frac{1}{R_{s1}} + \frac{1}{R_{s2}} + \frac{1}{R_{s3}} + \frac{1}{R_{s4}} \right)^{-1} \quad (7.2.2)$$

is the equivalent resistance of the parallel connection of resistors R_p and $R_{s1...4}$.

The high frequency intrinsic zero at f_Z of the CXX solution from Tab. 3.1 has allowed to find a suitable $Z_{LF}(s)$ without modifying the numerator polynomial in the individual transfer functions (3.5.2) of the resonators $H_{1...4}(s)$ by choosing $C_x = C_f = 0$.

This design method can be understood also in another way: Increasing the number of NTF zeros can be achieved if the individual integrators of a standard feed-forward compensated fifth order state variable loop filter are replaced by the cross-coupled resonators as shown in Fig. 7.7.

Since the frequencies f_z of the zeros of the resonator are close to its resonance frequencies f_0 , above their resonance frequencies the transfer functions of the resonators are converging against the transfer function of a standard first order integrator (Fig. 7.9).

Significantly above the highest resonance frequency f_0 , the order of the noise shaping of such a modified loop filter becomes equal to the order of the noise shaping of an ordinary loop filter. This raises the question to what extent this modification has an influence on the stability of the modulator.

As long as the transit frequency f_T of the loop gain of the modulator in Fig. 7.10 is far away from the highest resonant frequency f_0 , the effect on the stability is negligible. In a single-bit modulator the linearized gain of the quantizer k depends on signal statistics. With increasing input amplitude k is reduced and consequently f_T moves to lower frequencies. The modulator becomes unstable if f_T reaches the point of 180 degree phase lag f_{180} (Fig. 2.5).

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

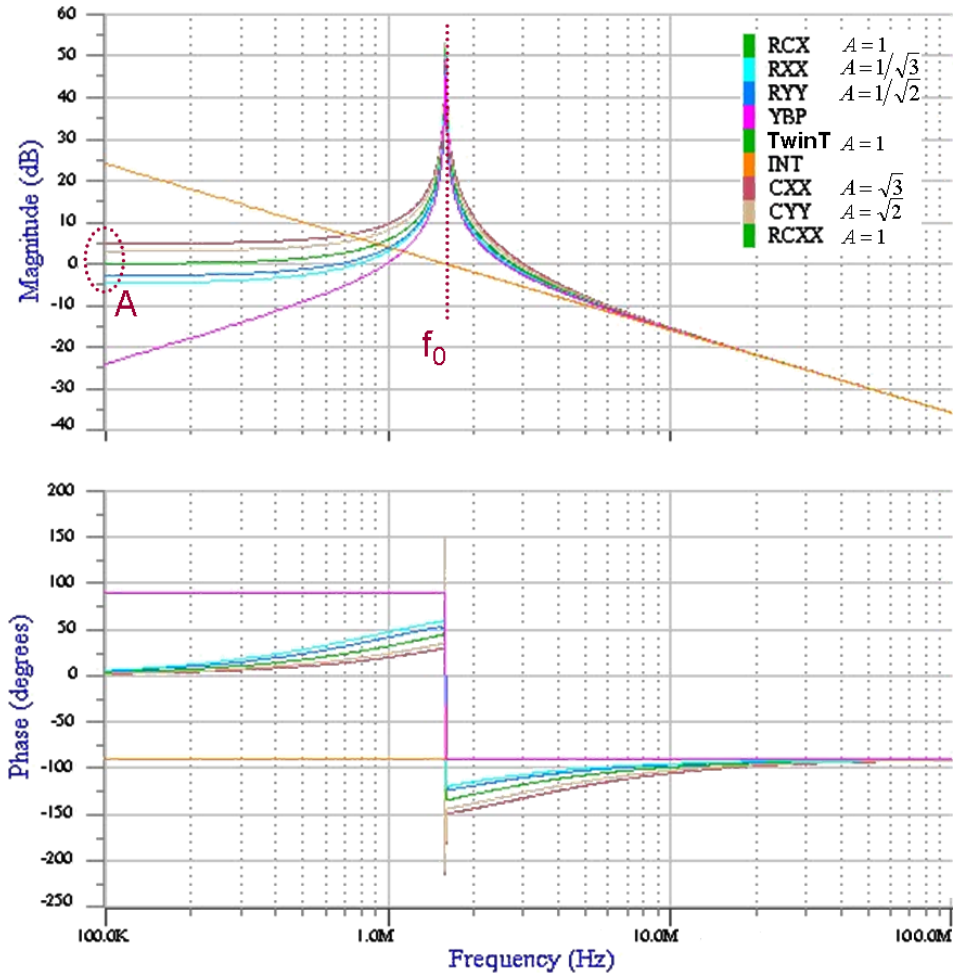


Figure 7.9.: Resonator transfer functions that are approximating an integrator transfer function for $f \gg f_0$.

Therefore, this point can serve as a lower bound for f_T . Additional resonators have no effect on the stability of the modulator as long as they resonate at a frequency sufficiently below f_{180} .

Due to the relatively high target OSR this condition is fulfilled with the implemented modulator and it is possible to substitute integrators with resonators with no further adjustment in the compensation network. Although

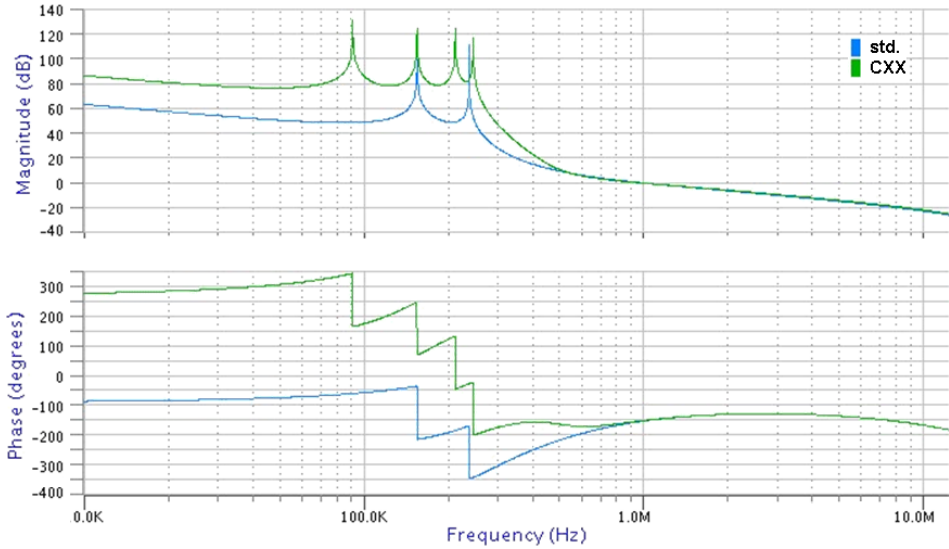


Figure 7.10.: Bode-plot of loop filter transfer function.

this procedure has been found to yield good results, it has to be stressed that stability can only be verified with extensive transient simulations of the non-linear modulator loop.

The starting point for the loop filter design has been a standard feed-forward compensated fifth-order loop filter with optimized zeros and $H_\infty = 1.2$ shown in Fig. 7.8. The local feedback around the integrators has been removed and the integrators 2 to 5 have been replaced by cross-coupled resonators. For the resonator, the CXX solution has been selected for the following reasons:

- It has the **highest pass-band gain** A in Fig. 7.9, which translates into the highest suppression of in-band quantization noise.
- It has a **small thermal noise** according to Fig. 3.6.

Each integrator time constant τ has been weighted by the scaling factor $f_z/f_0 = \sqrt{3}$ shown in Tab. 3.1 for the CXX structure, so that the high-frequency behavior of the individual integrators remains unchanged with $\tau = R_i C \sqrt{3}$. Then, the resistances in the feedback of the resonators and

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

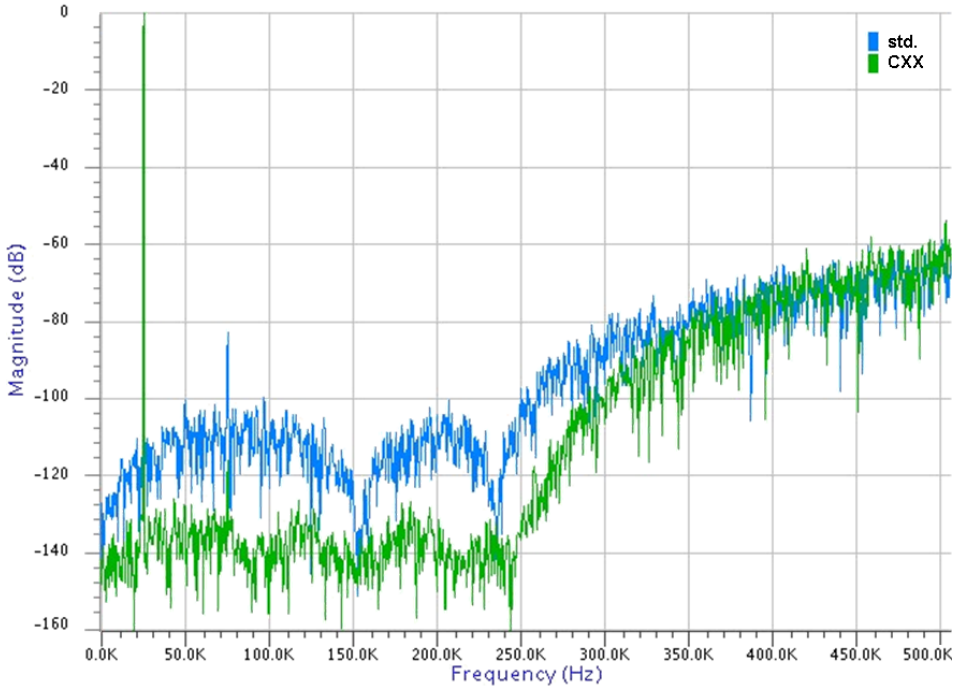


Figure 7.11.: Spectrum of simulated bitstream.

thereby the individual resonance frequencies f_0 have been optimized by AC simulation for the largest possible pass-band gain. An improvement of approximately 30 dB could be achieved (Fig. 7.11²).

Transient simulation have shown that the MSA degradation due to this modification is negligible. Thus, the scaling of the integrators and the compensation network did not need to be modified.

For comparison purposes and to demonstrate the improvement over a standard loop filter, switches have been added that allow to reconfigure the resonators such that they behave like standard integrators by disconnecting the

² The original target bandwidth has been 250 kHz which later has been reduced to 200 kHz, because the target sampling frequency has been reduced as well.

resistors from the feedback network of the CXX structure. In this way a standard fifth order loop filter transfer function is obtained. At the same time these switches connect a resistive local feedback path around integrators 2/3 and 4/5 according to Fig. 7.8 in order to optimize the NTF zeros also in the fifth order configuration.

These zeros are optimized to maintain the same in-band quantization noise floor as for the CXX configuration but within a smaller bandwidth. It would not have been reasonable to implement the fifth order transfer function of Fig. 7.10 and Fig. 7.11, because it would have resulted in in-band quantization noise that is approximately 30 dB higher than the thermal noise of the loop filter.

The opamps of the resonators are standard two stage miller compensated designs and the opamp of the first standard integrator stage is a two stage design using gain boosting in the first stage. A detailed discussion of the opamps can be found in the design report of the mostly-analog testchip [103].

Binary encoded passgate switches have been added at all the capacitors in the loop filter in order to allow the calibration of the process dependent RC product.

7.3 Quantizer

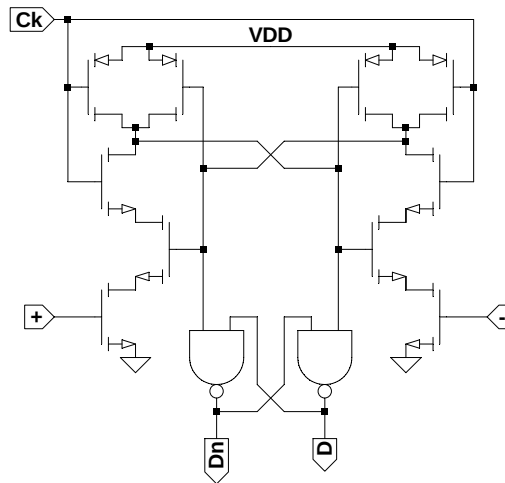


Figure 7.12.: Dynamic latched comparator.

The single-bit quantizer is a standard latched comparator (Fig. 7.12), also known as sense amplifier flip-flop [107]. It operates fully dynamic, i.e. there is no static power consumption.

Quantizer metastability usually requires to add a delay between the sampling instant and the rising edge of the DAC pulse [53]. This delay could be easily obtained by inhibiting the DAC pulse during the high phase of the sampling clock. However, the resulting RZ pulse would be more sensitive to clock jitter than an NRZ pulse according to the discussion in Section 5.6.

Using a delayed NRZ pulse would require a method of ELD compensation to obtain a stable loop. However, simulations have shown that the effect of quantizer metastability can be mitigated by the following two measures to such an extent that no delay is necessary: A gain stage in front of the quantizer to reduce the probability of metastability and a FIR-DAC that is less sensitive to metastability, because all taps except the first one are delayed anyway.

7.4 Feed-Forward Summation Gain Stage

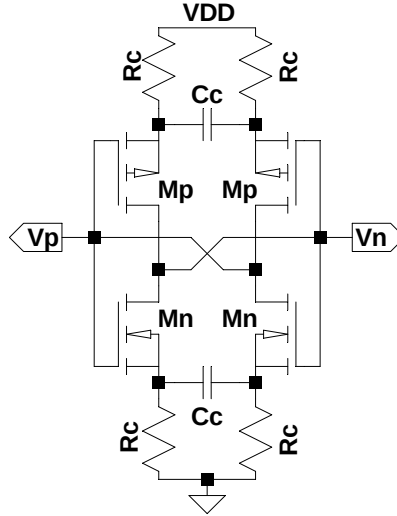


Figure 7.13.: Feed-forward gain stage based on negative impedance.

In order to avoid a dedicated summation opamp with gain for the adder network R_p , $R_{s1...4}$, low power amplification with gain A of the signal at the quantizer input is obtained by adding in parallel a negative impedance (Fig. 7.13) with an absolute resistance that is slightly larger than the output resistance of the adder network (7.2.2). This yields a gain factor A under the condition

$$R_c + 1/g_m = \frac{2AR_{||}}{A - 1} \quad (7.4.1)$$

where g_m is the transconductance of the transistors M_p and M_n . In this way the signal at the input of the quantizer is amplified and the probability of quantizer metastability is reduced. Since the negative resistance is dominated by R_c and no precise gain factor A is needed, no measures have been implemented to precisely define g_m .

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

The quantizer represents a capacitive load for the output of the loop filter. To reduce the impact of the resulting pole, the compensation capacitors C_c have been added in Fig. 7.13, such that the impedance of this stage corresponds mostly to the parallel connection of a negative resistor and a negative capacitor. This active summation stage allows to compensate both the resistive output impedance of the filter and the capacitive input impedance of the quantizer for enhanced gain and increased corner frequency of the extra pole.

With these measures, the ADC could be implemented with only five instead of ten opamps that would be required in case of a conventional ninth-order active RC loop filter with feed-forward compensation and summation opamp. Compared to the conventional topology, the estimated reduction of the total power consumption is 30 % and the estimated reduction of the loop filter area is 40 %.

7.5 Feedback DAC

Table 7.1.: JNR-DAC Modes

Mode	LP-FIR coeff.	HP-FIR coeff.
1	+1 + 1 + 1 + 1	+3 - 1 - 1 - 1
2	+2 + 0 + 1 + 1	+1 + 1 - 1 - 1
3	+2 + 1 + 0 + 1	+2 - 1 + 0 - 1
4	+3 + 0 + 0 + 1	+0 + 1 + 0 - 1
5	+1 + 2 + 1 + 0	+3 - 2 - 1 + 0
6	+3 + 0 + 1 + 0	+1 + 0 - 1 + 0
7	+2 + 2 + 0 + 0	+2 - 2 + 0 + 0
8	+4 + 0 + 0 + 0	+0 + 0 + 0 + 0
9	+0 + 1 + 2 + 1	+4 - 1 - 2 - 1

For further improved robustness to clock jitter the JNR-DAC concept that has been discussed in Section 6.8 has been implemented with a four tap FIR-filter and a first order analog high-pass with a corner frequency $f_c = 500$ kHz.

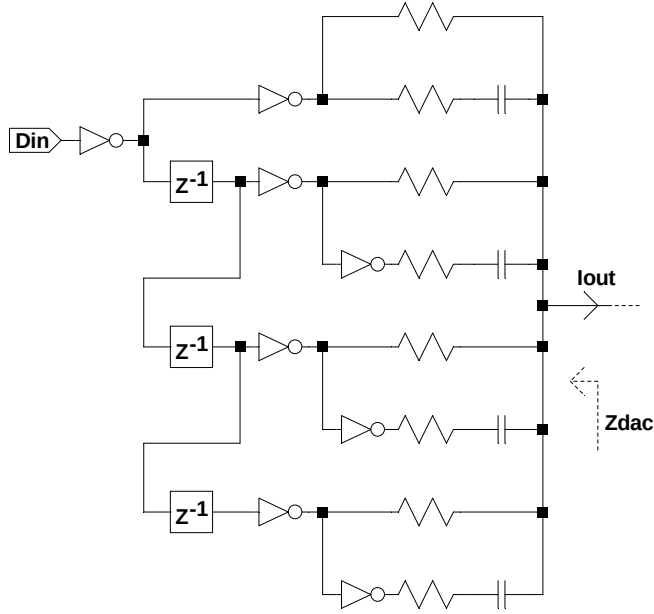


Figure 7.14.: Single-ended illustration of the JNR-DAC implementation.

Targeting low thermal noise and high linearity, the FIR coefficients have been implemented with differential resistor-inverter-taps (Fig. 7.14). Since the reference voltage V_{ref} is half the supply voltage for all resistor-inverter tap, these taps have been connected to a separate supply voltage domain in order to minimize cross-coupling that could impact the modulator performance according to the reference-induced noise folding mechanism discussed in Chapter 5.

Passgate switches have been added to allow the selection of different configurations for the FIR-coefficients. The low-pass FIR-DAC frequency response of the various modes are depicted in Fig. 7.15 and the corresponding coefficients are listed in Tab. 7.1, where the numbers correspond to weighting factors for the admittance of the R taps in the low-pass FIR-DAC and the RC series connection taps in the high-pass FIR-DAC.

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

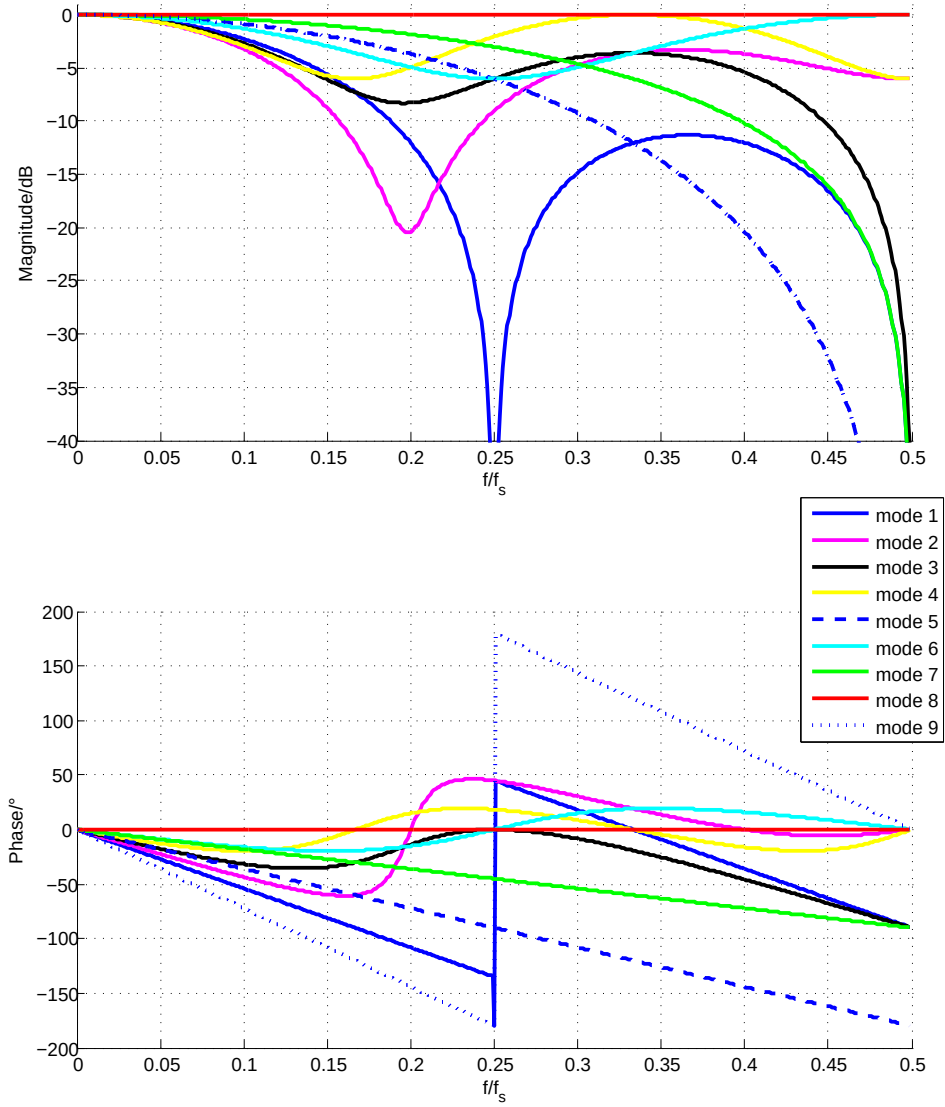


Figure 7.15.: Low-pass frequency responses of the various programmable JNR-DAC operating modes.

In mode 1 the low-pass FIR-DAC operates as a four tap moving-average filter which should result in good suppression of the out-of-band quantiza-

tion noise. Modes 2 – 4 and 6 select various filters which suppress different portions of the spectrum.

Mode 5 corresponds to the convolution of the impulse responses of two successive two-tap moving-average filters, i.e. it represents the series connection of two such filter stages. Mode 7 selects a single two-tap moving-average filter and in mode 8 the JNR-DAC is disabled and operates like a standard NRZ-DAC.

Mode 9 is a special mode to suppress pulse distortion due to quantizer metastability. This is achieved by shifting the low-pass impulse response of mode 5 by one clock period, such that the magnitude frequency response remains unchanged and only the phase response changes linearly.

The ELD that is caused by the required causality of the low-pass FIR impulse response is inherently compensated in every mode via the high-pass FIR-filter path.

7.6 Passive Pre-Filter

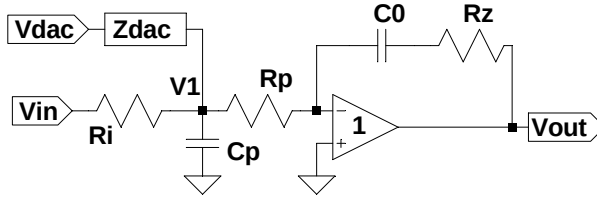


Figure 7.16.: Passive pre-filtering at first loop filter integrator.

In order to reduce the high frequency currents that the first opamp needs to drive into its feedback network, a first-order passive pole has been implemented by the capacitor C_p that is compensated by the zeroing resistor R_z in Fig. 7.16 [108, 109]. This reduces the load that the opamp has to drive at high frequency and allows to compensate the opamp for stability at closed loop gain $1 + R_z/R_p$ instead of unity which yields larger bandwidth.

Both effects translate into higher open loop gain at high frequencies and thus, less swing at the virtual ground node for improved linearity which reduces quantization noise folding.

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

The corner frequency of this pole and its compensation zero becomes

$$f_z = \frac{1}{2\pi R_z C_0} = \frac{R_p R_i + Z_{dac} R_i + Z_{dac} R_p}{2\pi Z_{dac} R_p R_i C_p} \quad (7.6.1)$$

where the impedance seen into the JNR-DAC Z_{dac} is assumed to be mostly resistive close to the corner frequency. This assumption is justified if the corner frequency of this pole is well above the corner frequency f_c of the high-pass filter within the JNR-DAC, i.e. $f_z \gg f_c$.

This condition is fulfilled with $f_z = 5$ MHz and $f_c = 500$ kHz. Above f_z the impedance between the virtual ground node and ground drops significantly which results in increasing noise gain of the opamp. This is another reason why f_z should be placed well above the bandwidth of the modulator.

For low frequencies the node V1 becomes a virtual ground itself due to the high open loop gain of the modulator. For higher frequencies, when the loop gain drops, the swing at V1 starts to increase until the pole at f_z becomes effective and thereby counteracts the increase.

Swing at node V1 may result in distortion of the feedback DAC. Hence, also the swing at node V1 has to be observed when defining R_p and C_p . For this reason $R_p = R_i/10$ has been chosen.

The additional resistance R_p modifies the time constant of the first integrator. This has to be compensated by adjusting the capacitor C_0 .

7.7 Implementation

A RC-oscillator for RC-calibration, a Serial Peripheral Interface (SPI)-Bus-Interface, a crystal oscillator circuit, a Low Voltage Differential Signaling (LVDS) interface, an input buffer with programmable gain, a bandgap and Design for Testability (DfT) circuits that allow to access internal nodes and inject test signals for bench evaluation complement the design.

The top schematic of the mostly-analog testchip is shown in Fig. 7.17 and the top layout is shown in Fig. 7.18. The chip has been implemented using Mentor Graphics IC station and it has been manufactured by X-Fab in a 1P3M 350 nm CMOS process [110].

The die micrograph of the testchip is shown in Fig. 7.19.

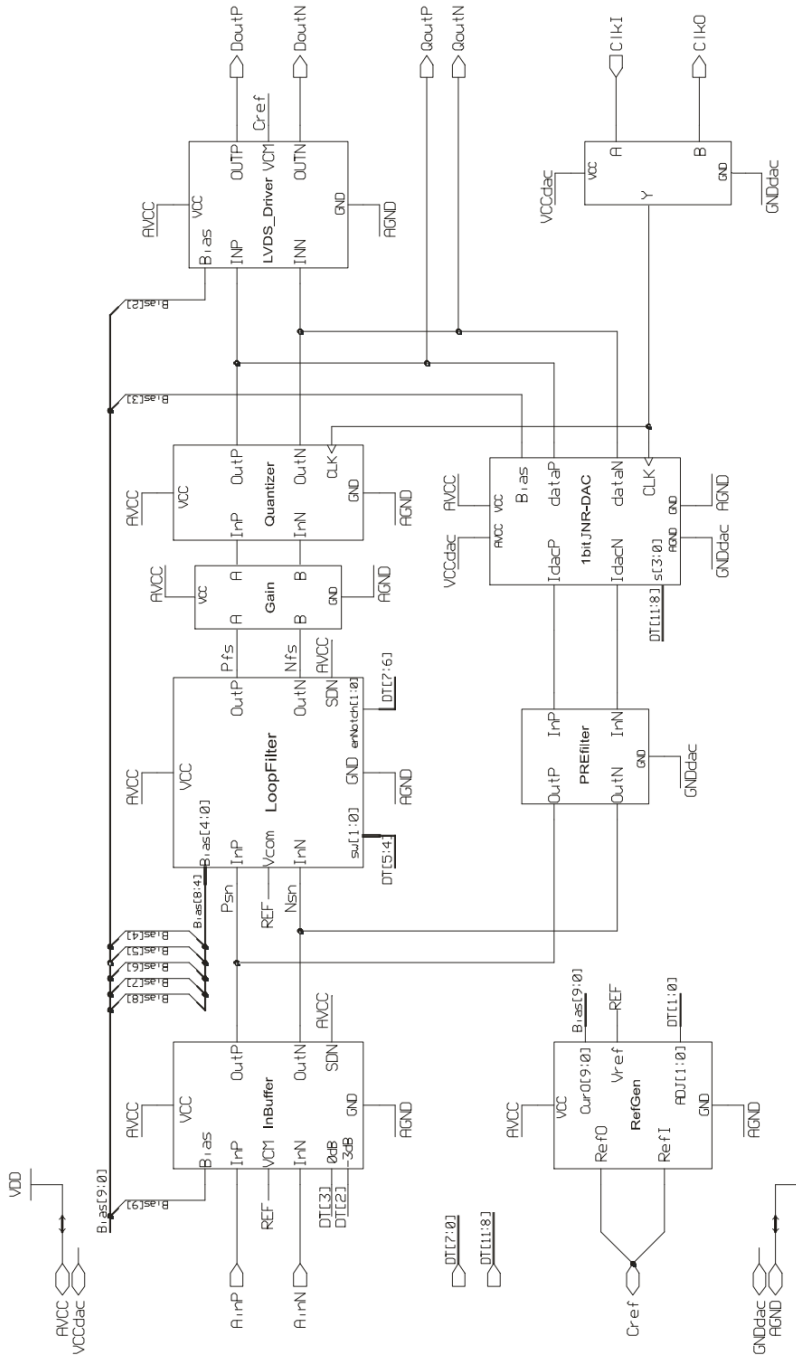


Figure 7.17.: Top schematic of mostly-analog testchip 1.

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

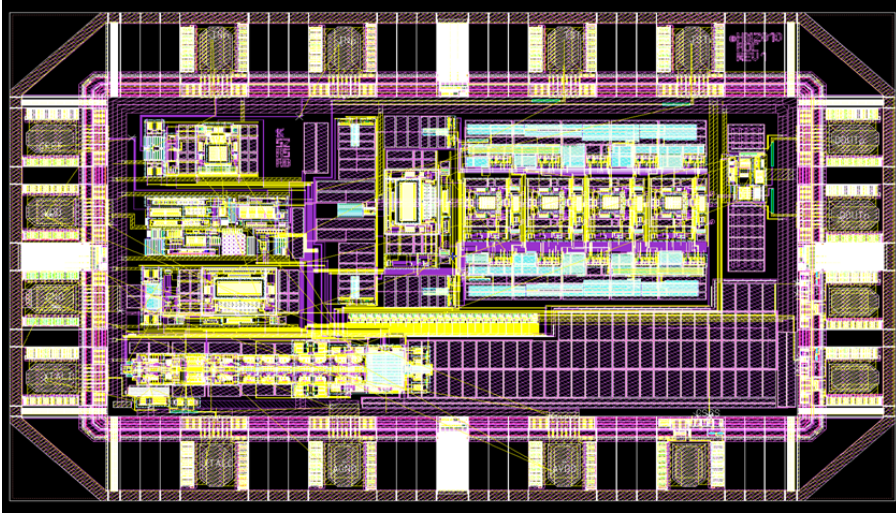


Figure 7.18.: Top layout of mostly-analog testchip 1.

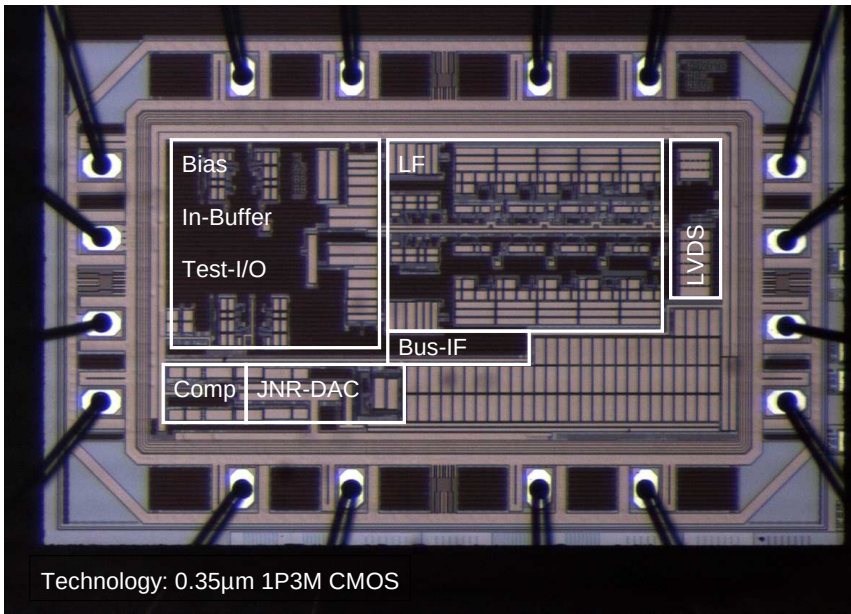


Figure 7.19.: Testchip 1: A ninth-order single-bit CT- $\Sigma\Delta$ -ADC.

7.8 Testbench

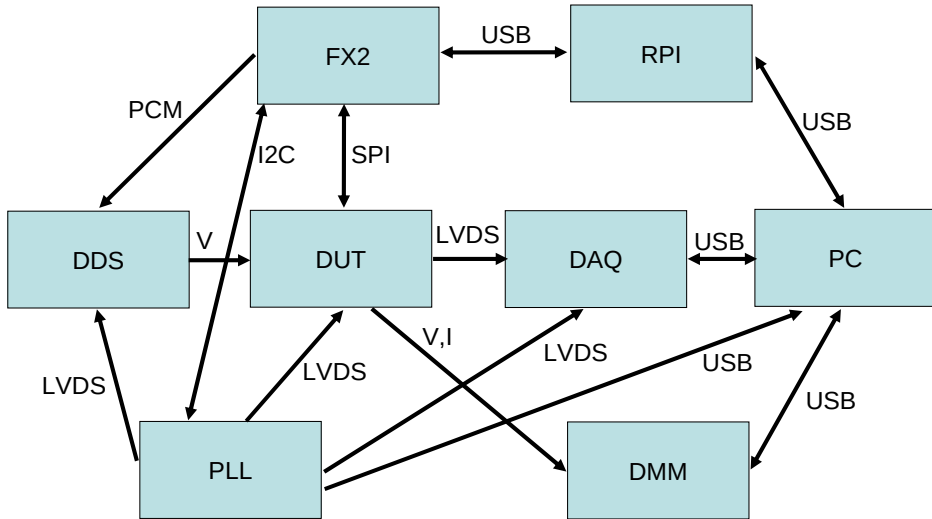


Figure 7.20.: Block diagram of measurement setup.

For the evaluation of data converter testchips, a comprehensive test environment has been developed (Fig. 7.20). It consists of a Direct Digital Synthesis (DDS) based stimuli generator that can provide single- and multi-tone test signals, a Device Under Test (DUT) board, a Field Programmable Gate Array (FPGA)-based Universal Serial Bus (USB) multi-channel data acquisition system and a PLL that provides synchronous low jitter LVDS, Emitter Coupled Logic (ECL) and CMOS clocks to the DDS system, the DUT and the Data Acquisition (DAQ) system for true coherent sampling (Fig. 7.21).

The DDS system consist of a 16-Bit laser-trimmed LTC1668 50 MHz differential RF-DAC that is fed by a Raspberry Pi single-board ARM-computer via a Cypress FX2-based USB interface. The Raspberry Pi runs a stripped down version of the Raspbian Linux distribution that has been tweaked to achieve realtime stimuli data generation at the full speed USB 2.0 data rate of 480 Mbit/s. Linux software for data generation, USB stream transfers and the firmware for the i8051 Micro Controller (μ C) core of the Cypress FX2 have been developed based on the fx2pipe open source project [111].

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

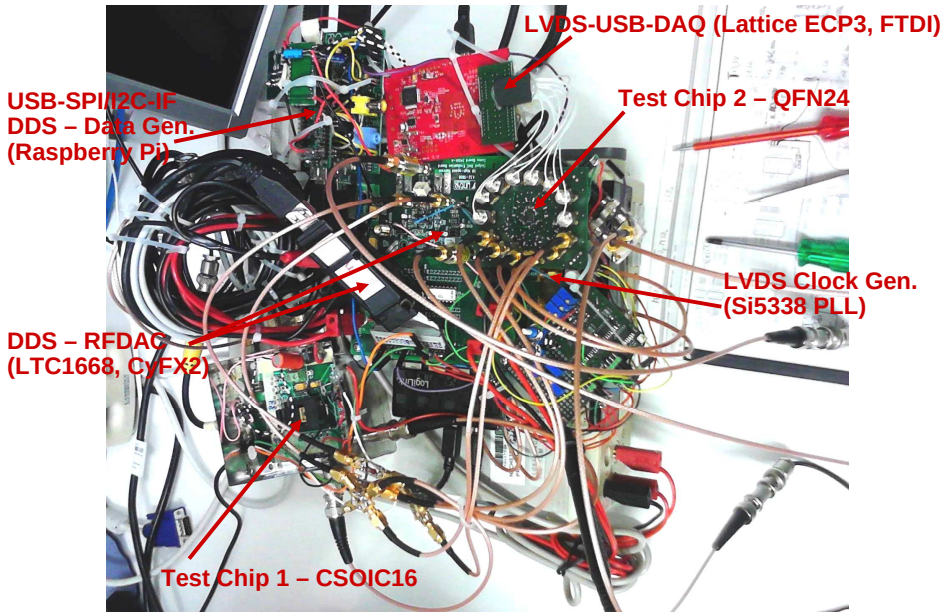


Figure 7.21.: Measurement setup.

The DUT board is designed specifically for the testchip. Inter-Integrated Circuit (I²C) or SPI buses are controlled from a bus master software that runs on the Cypress FX2. This μ C software in turn is controlled from the raspberry Pi data generation software.

The DAQ system is based on the TSW1405EVM board of Texas Instruments [112]. This board consists of a Lattice ECP3 FPGA and a full speed FTDI USB 2.0 interface. The Hardware Description Language (HDL) interface source code provided by Lattice [113] has been adapted for up to 16 arbitrary synchronous LVDS data links from DUT boards. Each data link may deliver data at a rate of up to 1 Gbit/s.

The FPGA is able to capture 65536 samples from all 16 data links concurrently in realtime until the data is transferred to a Personal Computer (PC) via USB 2.0. A command-line PC capture software has been developed with Microsoft Visual C using Dynamic Linked Librarys (DLLs) for USB communication provided by Texas instruments [114].

The PLL is based on the Si5338 evaluation board. It provides four low jitter outputs with independent fractional division ratios from a common VCO.

The maximum output frequency is 710 MHz. The RMS phase jitter is 0.7 ps typically. The Si5338 is controlled via I²C from the Raspberry Pi or alternatively via USB directly from the PC.

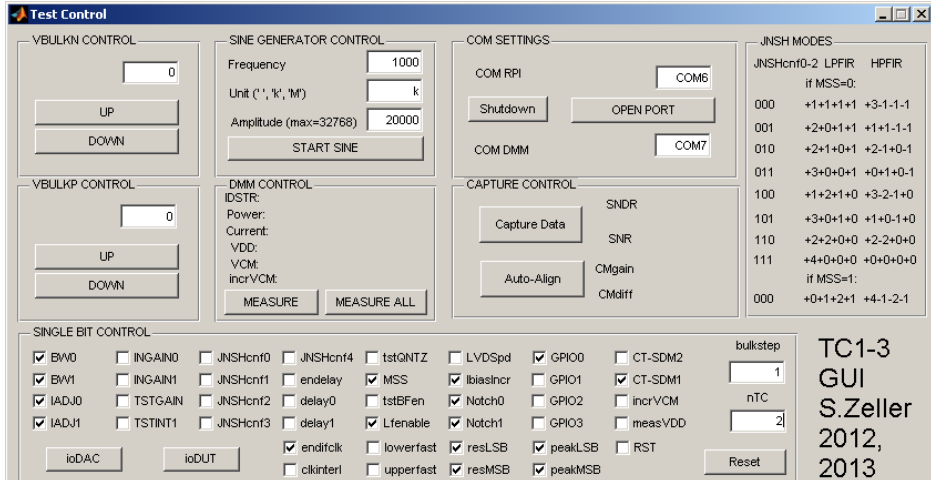


Figure 7.22.: Graphical User Interface (GUI) that controls the measurement setup.

The Raspberry Pi is controlled via its serial console and an USB to serial bridge from the PC. Also a Digital Multimeter (DMM) is connected via an USB to serial bridge to the PC. On the PC a MatLab script controls the software on the Raspberry Pi, the command-line DAQ software and the DMM. This script also provides a GUI (Fig. 7.22) for the various testchip control registers and the DDS/DAQ/DMM systems. It is able to perform fully automated measurements such as SNR/SNDR level sweeps.

7.9 Measurement Results

Measurement results for the CXX configuration are listed in Tab. 7.2 and a SNR/SNDR level sweep within 200 kHz bandwidth is shown in Fig. 7.23.

The measured spectrum at the output of the modulator is depicted in Fig. 7.24 and Fig. 7.25 for both the standard fifth-order and the ninth-order CXX loop filter configurations. These spectra show that the usable bandwidth can be doubled with negligible extra power consumption using CXX resonators instead of integrators.

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

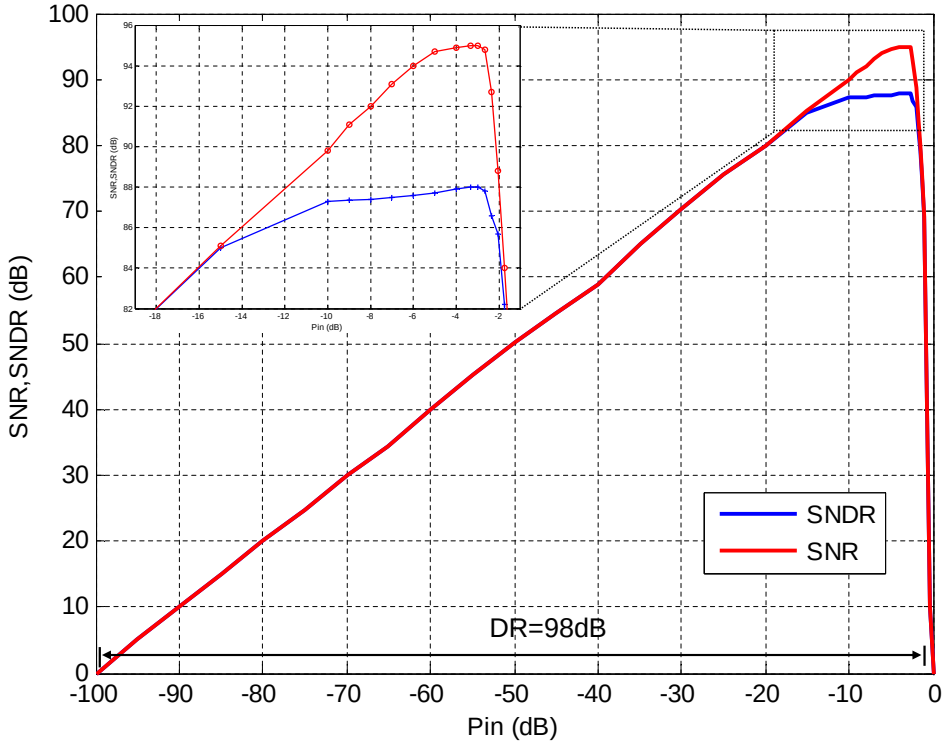


Figure 7.23.: Differential bitstream SNR/SNDR (Bandwidth (BW)=200 kHz, ninth order loop filter configuration) sweep for a 50 kHz test signal.

The dominant noise source of this ADC is the flicker and thermal noise of the first loop filter opamp. This opamp has a high power dissipation due to the low noise level required for a DR of 98 dB within 200 kHz bandwidth and due to the high slew rate required to process the strong single-bit quantized current pulses at high linearity. As a result the achieved FoM is worse than that of more broadband designs. However, a more fair comparison using FoM_2 shows that this ADC yields state of the art power-efficiency[115].

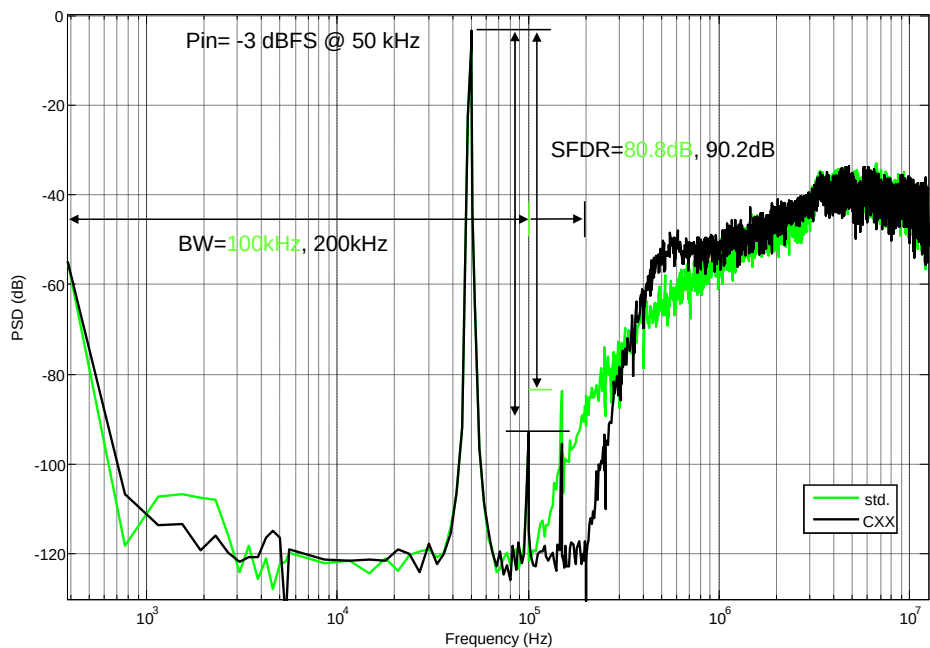


Figure 7.24.: Measured spectrum of the bitstream output.

Table 7.2.: Measured Chip Performance

V_{DD}	3.3 V	Core Area	0.9 mm ²
DR	98 dB	Total P_{diss}	17.4 mW
SNDR _p	88.1 dB	LF P_{diss}	13.8 mW
SNR _p	95.1 dB	SFDR	90.2 dB
MSA	-2 dBFS	Bandwidth	200 kHz
FoM	1.7 pJ/conv.-step	f_s	22 MHz
FoM ₂	158.7 dB	Technology	350 nm

7. Testchip 1: A Mostly-Analog Continuous-Time $\Sigma\Delta$ -ADC

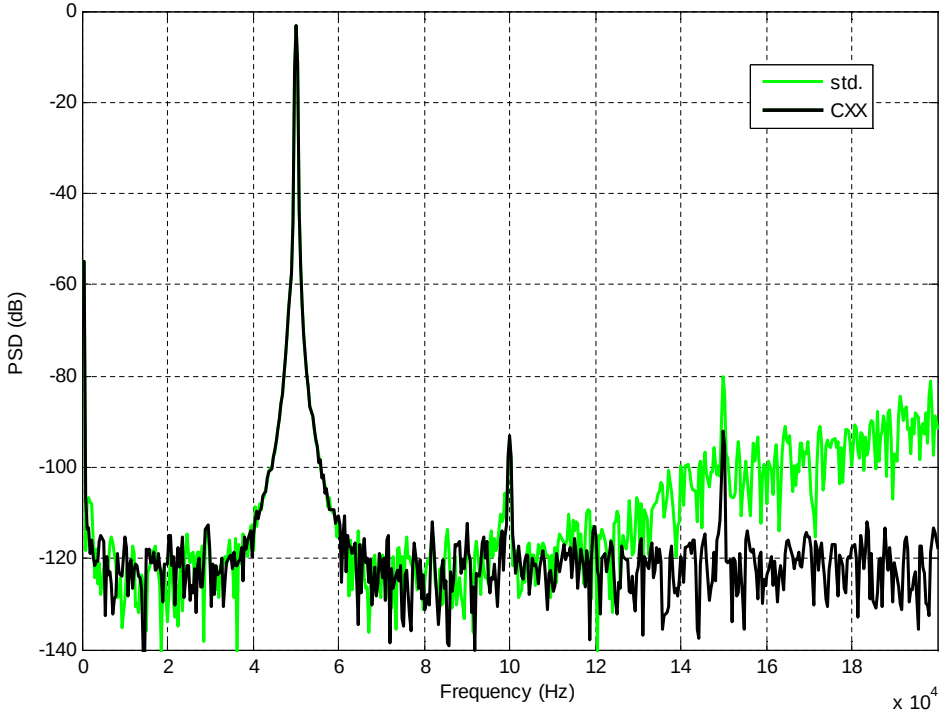


Figure 7.25.: Measured bitstream spectrum within the band of interest.

The various JNR-DAC modes have been evaluated with a sampling clock provided by the internal Crystal (XTAL) oscillator and with an external sampling clock. The external clock has a higher phase noise than the internal XTAL oscillator. The results are listed in Tab. 7.3. Mode 1 shows the best performance with both clocks. With the external clock it yields a 10 dB improvement over a standard NRZ-DAC (mode 8), but it is still 5 dB worse than the results for the XTAL. This means that jitter-induced noise is still dominating over thermal and quantization noise.

It also means that 10 dB is the maximum improvement that can be obtained for the characteristic phase noise spectrum of the external clock signal. A different phase noise spectrum might yield a higher improvement, but ultimately the simple first order high-pass within the JNR-DAC and its low corner frequency are the limiting factors. For more suppression of jitter-induced noise a higher order high-pass would be required.

Table 7.3.: JNR-DAC Measurements

Mode	XTAL SNR/SNDR	ext. clock SNR/SNDR
1	95/88 dB	90/86 dB
2	92/86 dB	85/83 dB
3	92/86 dB	84/83 dB
4	90/85 dB	84/83 dB
5	94/87 dB	89/86 dB
6	91/86 dB	84/82 dB
7	93/87 dB	87/85 dB
8	89/84 dB	80/78 dB
9	94/87 dB	89/86 dB

Also modes 5 and 9 yield a considerable improvement. Since both modes show the same results it can be concluded that the impact of quantizer metastability is negligible in this design.

The measurement results of the testchip prove that with the proposed measures full ninth-order noise shaping with four pairs of conjugate complex NTF zeros is possible in a power-efficient way with only five opamps.

8 Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

In this chapter design techniques for the realization of compact, low-power CT- $\Sigma\Delta$ -ADCs in ultra deep submicron CMOS are presented:

A resonant single-opamp third order integrator with loss compensation, an inverter-based opamp with digitally-assisted biasing and common mode control, a pseudo-differential modulator topology with quasi-1.5-bit quantization, a jitter-noise-reduction DAC with NRZ pulse shape, a mismatch-tolerant IIR-quantizer, linearized single-ended FIR-DACs with passive DT compensation and a rail-to-rail dynamic latched comparator.

A highly compact 41.4 fJ/conv.-step, 77 dB-SFDR, 1.1 V ADC has been implemented to prove these concepts [116]. The entire active analog circuitry in this minimalistic mostly digital third order modulator consists of only 10 CMOS inverters.

8.1 Concept of Testchip

In recent years, there has been a significant improvement in power- and even more in area-efficiency of CT- $\Sigma\Delta$ -ADCs. While in 2006 a state of the art design in the class of above 10 MHz bandwidth had a FoM of around 122 fJ/conv.-step at a chip size of 1.2 mm², recently published designs are now below 50 fJ/conv.-step and below 0.1 mm² [37, 61, 93].

In the past, CT- $\Sigma\Delta$ -modulators have relied on large and power hungry first order integrators and element-mismatch-sensitive multi-bit quantization to achieve state of the art figures-of-merit FoMs above 10 MHz bandwidth [39]. However, recent designs using higher order integrators [117], single-bit FIR-DACs at high sample rates [83, 94] and digitally-assisted DAC

8. Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

2006: 122fJ/conv.-step, 1.2mm² $\longrightarrow$ today: <50fJ/conv.-step, <0.1mm²

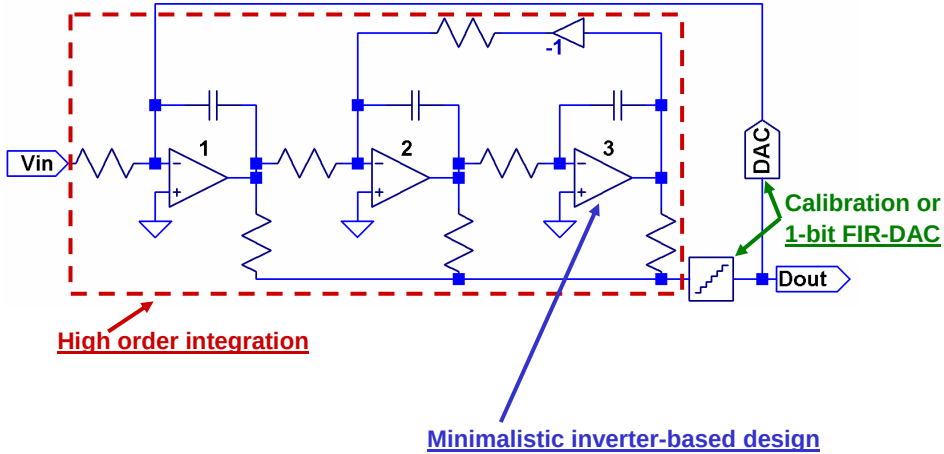


Figure 8.1.: Motivation for testchip 2.

correction [41, 61] have demonstrated improved FoMs with significantly less chip size. This work contributes techniques for further improvement:

Power and area reduction using a single-opamp third order integrator instead of a cascade of three integrators has been proposed in [117]. However, this non-resonant loop filter does not allow to optimize the noise transfer function NTF zeros for maximum SNR. In Section 8.2, an implementation of the novel *resonant single-opamp third order integrator* according to Chapter 4 will be presented that overcomes this limitation.

The power consumption of loop filter RC-integrators depends on the required opamp GBW that has been relaxed in recent publications by compensating finite-GBW-induced ELD [39, 41, 61] or by assisting the opamp with current mode DACs [83]. However, the tolerable loss that determines the required opamp DC-gain is also an important parameter for the integrator power consumption, because DC-gain trades with GBW for a given power dissipation.

This becomes apparent at low supply voltage, where cascading of stages is preferred over cascoding due to insufficient voltage headroom. In Section 8.3, a negative-resistor-based *integrator loss compensation technique* is proposed that supports low supply voltage and technology scaling by reducing the required DC-gain. It provides a way to better utilize the decreasing transistor intrinsic gain and the increasing transit frequency in modern technologies [18, pp. 3–18].

To put it another way, with integrator loss compensation, a desired loop gain can be obtained with a smaller number of gain stages in the opamp. One goal of this work is to enable the implementation of modulators with single-gain-stage opamps in order to avoid wasting power and bandwidth on local frequency compensation. A third order integrator based on a novel *single CMOS inverter-opamp* will be discussed in Section 8.4. The inverter bias is robust against PVT variations using *digitally-assisted control of bulk potentials*.

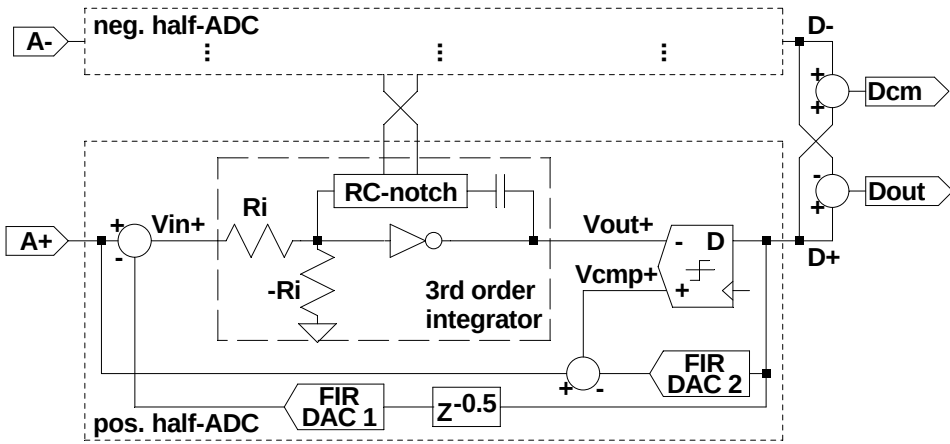


Figure 8.2.: Pseudo-differential ADC using two single-ended CT- $\Sigma\Delta$ modulators.

Traditionally, high-performance CT- $\Sigma\Delta$ -ADCs are implemented with fully-differential opamps. However, fully-differential inverter-based opamps require extra stages for common mode rejection and common mode output bias voltage definition [118–121].

8. Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

Instead, a novel *pseudo-differential modulator topology* is proposed in Section 8.5. It avoids extra inverter gain-stages by implicit common mode control using single-ended quantized feedback (Fig. 8.2). Two highly decorrelated quantizers yield linear *quasi-1.5-bit quantization* with high Common Mode Rejection Ratio (CMRR) by digital subtraction. A *linearization technique for single-ended, single-bit NRZ-DACs* avoids non-linearity caused by Intersymbol Interference (ISI) (Section 8.6).

According to Chapter 6 FIR-DACs suppress shaped quantization noise by a low-pass transfer function yielding high clock jitter tolerance and relaxed loop filter linearity requirements. Using a single-bit DAC per FIR tap guarantees inherent linearity. This enables the realization of more compact and power-efficient modulators than comparable multi-bit designs that require expensive DAC linearization. For loop stability, the FIR transfer function needs to be compensated by restoring the suppressed portion of the quantized signal. In recent designs, this has been done within the CT loop filter [83, 94]. In this testchip two alternative solutions are used:

In Section 6.4, a *jitter-noise-reduction JNR-DAC* has been presented that achieves suppression of clock jitter-induced noise while preserving a standard NRZ-DAC impulse response. No further compensation of the FIR transfer function is required.

In Section 6.5, an *IIR quantizer* has been proposed that achieves FIR-DAC compensation within the quantizer itself. This guarantees a stable modulator loop while only the slow FIR-filtered DAC output signal needs to be processed by the CT loop filter for reduced opamp speed requirements.

A FIR-DAC transfer function that inversely matches the quantization noise spectrum ensures optimum suppression of jitter-induced noise. The feedback of the fast quantizer signal components is realized with a passive DT loop directly around the quantizer. Subtraction is performed by a novel differential *rail-to-rail dynamic latched comparator* for minimized load at the loop filter output.

In Section 8.7 an *optimizer based design method* for third order modulators that incorporate IIR quantizers will be proposed and in Section 8.8 the IC implementation and the testbench is discussed.

Finally, in Section 8.9 measurement results of a highly-compact ultra-low-FoM CT- $\Sigma\Delta$ -ADC in 65 nm CMOS will be presented.

8.2 Resonant Single-Opamp Loop Filter

The loop filter of this testchip is based on the novel third order single-opamp integrator (Fig. 4.2) discussed in Chapter 4. It consists of a feed-in, a notch and a high-pass network. The notch network defines the denominator of the transfer function and thereby the resonance frequency. The high-pass network defines a basic second order numerator polynomial with real roots only. It can be modified to an arbitrary second order polynomial with complex roots by the feed-in network.

Separate feed-in networks (Fig. 4.5a) for the analog input signal and the digital feedback signal allow defining the STF independently of the NTF as discussed in Section 4.2. This possibility has not been exploited in this mostly-digital testchip, because the chosen wideband modulator topology [122] does not allow to have an STF other than unity.

In Fig. 4.5b the scheme is depicted that has been implemented in this testchip. The inversion is done here in the digital domain to save power.

The inverter-resistor DACs only illustrate the linearized single-ended FIR-DACs that will be discussed in Section 8.6. Merging the capacitors in both feed-in networks minimizes the voltage swing across them because the analog input signal V_{in} is canceled by the digital feedback signal D . This reduces distortion in the gm -stages of the integrator loss compensation technique that is discussed in the next section.

Modulators with orders larger than three can be implemented by cascading this third order integrator with the second order integrators proposed in [64, 68] as has been discussed in Chapter 4. Mismatch within the notch network degrades the quality factor of the resonance. The CXX notch configuration from Chapter 3 [68] has been selected in Fig. 4.2 for its low thermal noise, low circuit area and good matching properties due to identical component values.

In comparison to the standard state variable active-RC loop filter topologies, additional high-pass-shaped thermal noise is introduced by R_x and R_f . The corner frequency of their noise contribution can be increased by choosing small component ratio b and large a for a given transfer function.

On the other hand, reducing these ratios increases the impedance level of the feed-in network and consequently the thermal noise contribution of R_i . These conflicting dependencies mandate optimizing a and b for low in-band thermal noise under consideration of aspects like chip size, load for the

8. Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

opamp or component matching. Choosing e.g. $a = 3$ and $b = 1$ yields the analytic expression for the differential resonant third order transfer function

$$L_{diff}(s) = -\frac{5s^2 R^2 C^2 \left(\frac{1}{R_i} - \frac{1}{R_x} + \frac{1}{R_f} \right)}{3s^3 R^2 C^3 + sC} - \frac{sRC \left(\frac{16}{R_i} - \frac{8+\sqrt{29}}{R_x} + \frac{8-\sqrt{29}}{R_f} \right) + \frac{7}{R_i}}{3s^3 R^2 C^3 + sC} \quad (8.2.1)$$

with

$$C_x = \frac{8 + \sqrt{29}}{7R_x} RC, \quad C_f = \frac{8 - \sqrt{29}}{7R_f} RC. \quad (8.2.2)$$

The analytic common mode transfer function for an implementation based on a pseudo-differential opamp (Fig. 8.2) is a fourth order expression that has one additional pole and one additional zero. It can be approximated using the third order transfer function

$$L_{cm}(s) = -\frac{5s^2 R^2 C^2 \left(\frac{1}{R_i} + \frac{1}{R_x} + \frac{1}{R_f} \right)}{3s^3 R^2 C^3 + 4s^2 RC^2 + sC} - \frac{sRC \left(\frac{16}{R_i} + \frac{8+\sqrt{29}}{R_x} + \frac{8-\sqrt{29}}{R_f} \right) + \frac{7}{R_i}}{3s^3 R^2 C^3 + 4s^2 RC^2 + sC}. \quad (8.2.3)$$

The numerator polynomial in (8.2.3) becomes the same as in (8.2.1) if -1 gain stages are used instead of cross-coupling in the feed-in network (Fig. 4.2). The additional second order term in the denominator of (8.2.3) stems from the ineffectiveness of the cross-coupling within the notch network for common mode signals. It prevents the filter from resonating and weakens the achievable noise shaping in common mode (Fig. 4.6).

With this filter, a minimum opamp DC-gain of about 65 dB is required to meet the ADC performance target. That is clearly too much for an opamp implementation with a single near minimum feature size CMOS inverter stage. In the next sections techniques to relax the required opamp DC gain are proposed.

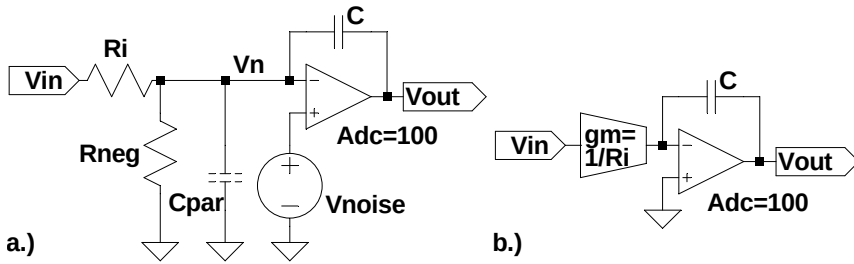


Figure 8.3.: a.) Integrator loss compensation technique, b.) gmC -opamp integrator.

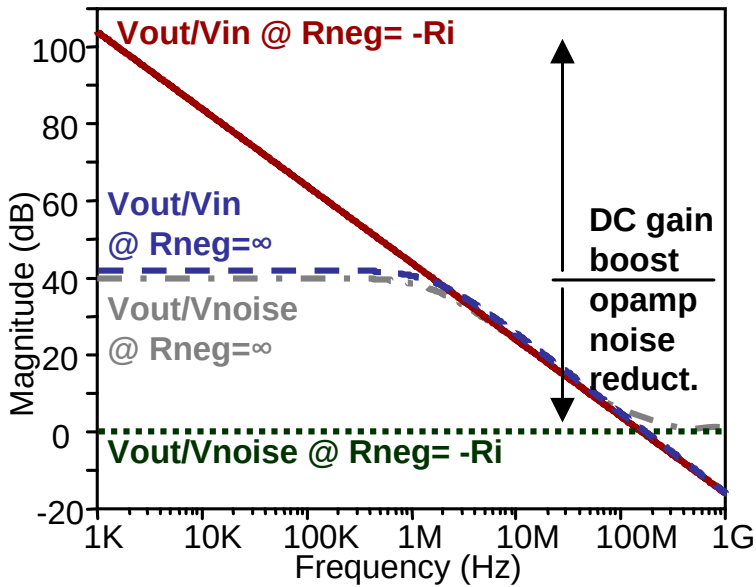


Figure 8.4.: DC gain improvement and noise reduction.

8.3 Integrator Loss Compensation

Finite DC gain of the opamp in Fig. 8.3a results in lossy integration, because low frequency swing of the virtual ground node voltage V_n degenerates the current through the feed-in resistor R_i .

8. Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

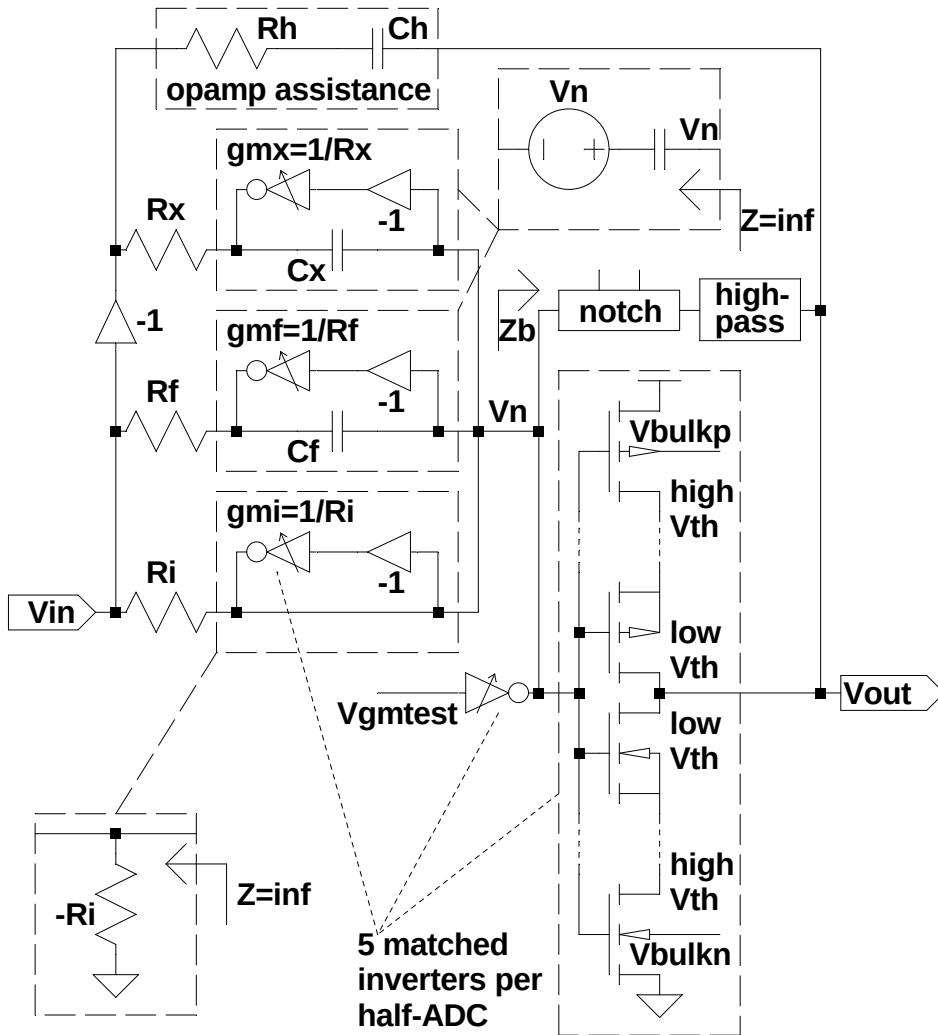


Figure 8.5.: Implemented third order integrator.

Using a high-output-resistance gm -stage instead of R_i (Fig. 8.3b) would avoid that loss at the cost of transconductor non-linearity. However, infinite output-resistance of the feed-in network can also be obtained by adding a negative resistor R_{neg} in Fig. 8.3a.

The resulting transfer function is

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{\left(1 + \frac{1+C_{par}/C}{A(s)}\right) sR_iC + \frac{1+R_i/R_{neg}}{A(s)}} \quad (8.3.1)$$

where $A(s)$ is the opamp voltage gain. With $R_{neg} = -R_i$ and the single-pole opamp model

$$A(s) = \frac{A_{dc}}{1 + s\frac{A_{dc}}{2\pi f_T}}. \quad (8.3.2)$$

ideal integration is restored (Fig. 8.4):

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{\left(1 + \frac{1+C_{par}/C}{A_{dc}} + s\frac{1+C_{par}/C}{2\pi f_T}\right) sR_iC} \quad (8.3.3)$$

Finite-GBW induces an extra pole at approximately the transit frequency f_T of the opamp. This pole can be compensated with a series resistor in the feedback [60].

From (8.3.1), the DC gain boost becomes

$$A_{boost} = \left| \frac{1}{1 + R_i/R_{neg}} \right|. \quad (8.3.4)$$

The achievable A_{boost} depends on resistor matching, where R_i includes the output resistance of the preceding stage or source. For example, a 20 dB gain boost requires a 10% matching.

High impedance at the virtual ground node also means low amplification of the input referred opamp noise V_{noise} (Fig. 8.4). With $R_{neg} = -R_i$, the equivalent integrator input noise power spectral density (PSD)

$$|V_{in,noise}(f)|^2 = \left(\frac{f^2}{f_n^2} + \left(1 + \frac{R_i}{R_{neg}}\right)^2 \right) |V_{noise}(f)|^2 \quad (8.3.5)$$

due to the opamp input noise PSD $|V_{noise}(f)|^2$ decreases below the corner frequency

$$f_n = \frac{1}{2\pi R_i (C + C_{par})}. \quad (8.3.6)$$

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Therefore, the thermal and even more the $1/f$ noise specification of the opamp can be greatly relaxed with this technique. On the other hand, the active stage that represents R_{neg} contributes noise as well. Beyond integrators, the concept of manipulating the noise gain by a negative resistor at the virtual ground can be useful also for general opamp circuits. If this stage shows a noise similar to R_i , then the contribution of R_i to the total equivalent input noise PSD appears to be doubled when compared to an integrator without loss compensation.

In contrast to a gmC -opamp integrator (Fig. 8.3b), high linearity is preserved with this solution, because any non-linearity of the active stage that represents R_{neg} sees only the small swing of V_n . In the first stage of a $\Sigma\Delta$ -modulator, this swing is strongly suppressed by the quantized feedback around the loop filter. Also the impact of any non-linearity of the opamp itself is significantly reduced, because at low frequency the loop gain around the opamp is higher by a factor of

$$G(s) = 1 + \frac{2\pi f_n}{s} \quad (8.3.7)$$

than without R_{neg} . Close-to-carrier intermodulation products are lower by approximately this factor at the same level of the fundamental tones at the integrator output [123]. The load for the opamp due to the feedback network is reduced to the series connection of C and C_{par} at the same time. This further increases the loop gain especially with Operational Transconductance Amplifier (OTA)-based opamps and it helps to reduce the power consumption.

Implementing the active stage that represents R_{neg} with cross-coupled differential-pairs increases the parasitic capacitance C_{par} , which in turn increases the capacitive load for the opamp. Its effect on the transfer function of the integrator can be compensated by adjusting the time constant $R_i C$ in (8.3.1).

In Fig. 8.5, the concept of loss reduction is depicted for the implemented third order integrator. The basic idea is the same as in Fig. 8.3: Infinite output impedance of the feed-in network prevents swing of V_n from influencing injected currents.

A negative resistor towards ground for the R_i feed-in path is generated by an inverter-based gm stage that is cross-coupled to the virtual ground node of the opposite half-ADC (indicated by the -1 gain stage). At the high-pass

feed-in paths, unity gain amplifiers are realized by R_x , R_f and gm stages in such a way that both terminals of the capacitors C_x , C_f track the swing of V_n . This prevents currents from flowing through C_x , C_f .

The resulting broadband current source behavior not only boosts the DC gain, but also the quality factor of the resonator. For optimum results, the impedance of the feedback network Z_b needs to be compensated by a parallel impedance $-Z_b$ as well. For a perfect pole at the origin of the s -plane, the gm in the R_i -path must be modified to

$$gm_i = \frac{1}{Z_b(f=0)} + \frac{1}{R_i}. \quad (8.3.8)$$

A broadband compensation of Z_b would require extra circuitry due to the complex feedback network. However, compensating it only at DC and at f_0 by slightly detuning the inverter gms in the high-pass feed-in paths to obtain a perfect resonance is sufficient in most cases. This corrects the denominator of (4.2.5) and (8.2.1) accordingly. The slight modification of the numerator due to this narrowband compensation can be neglected.

The single-ended impedance seen into the CXX notch network is at DC

$$Z_b(f=0) = R_{DC} = \left(2 + \frac{1}{a}\right) R \quad (8.3.9)$$

and at f_0

$$Z_b(f=f_0) = \frac{Z_{f_0,2}}{2} = \frac{R}{4} (1 - j\sqrt{3}). \quad (8.3.10)$$

Compensating at f_0 requires finding modified gm for the high-pass feed-in paths that satisfy the equation

$$\frac{gm_f - \frac{1}{R_f}}{1 - jff/f_0} + \frac{gm_x - \frac{1}{R_x}}{1 - jfx/f_0} = \frac{1}{Z_b(f=f_0)} - \frac{1}{Z_b(f=0)} \quad (8.3.11)$$

in the real and imaginary domain. Fig. 8.6 shows the transistor level simulation of the loop filter in the mostly-digital testchip according to Fig. 8.5 along with the desired transfer function.

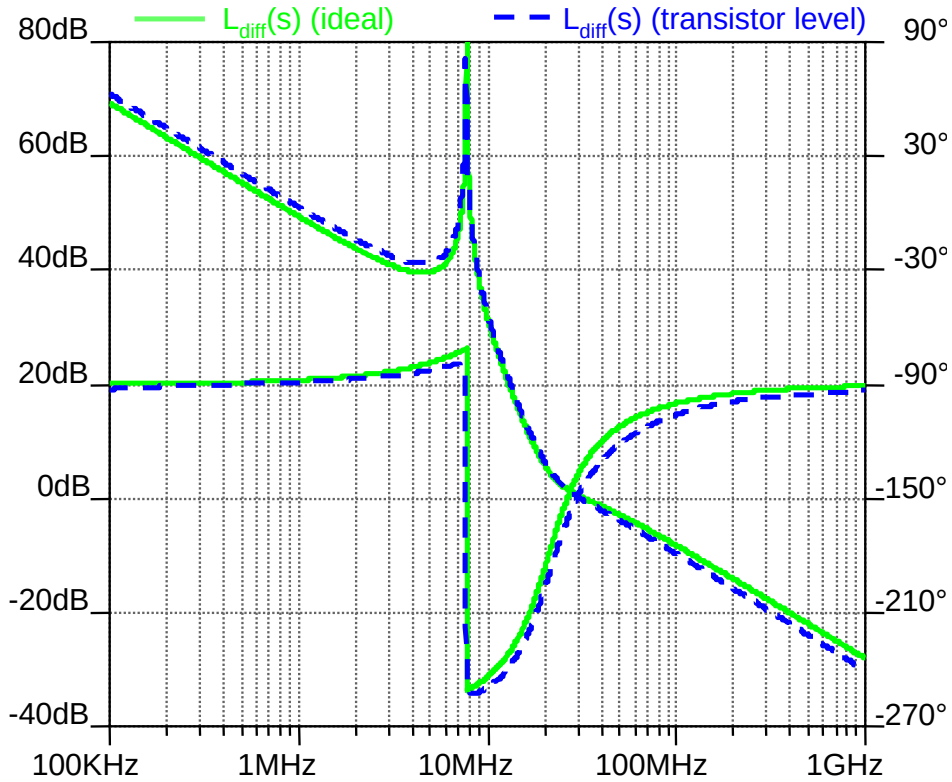


Figure 8.6.: Ideal $L_{diff}(s)$ and transistor level implementation.

8.4 Inverter-Based Opamp

Integrator loss compensation provides the extra gain that enables using a single gain stage instead of a multi-stage opamp in the loop filter. One goal of this testchip has been to investigate if a high performance CT- $\Sigma\Delta$ -ADC could be implemented using only CMOS inverters as gain stages for high power efficiency and low supply voltage compliance.

In a standard differential modulator topology with RC loop filter, it is not possible to substitute each opamp with two inverters, because their common mode output voltage would be undefined. There is no common mode DC feedback, neither locally via the capacitive feedback of the integrators nor

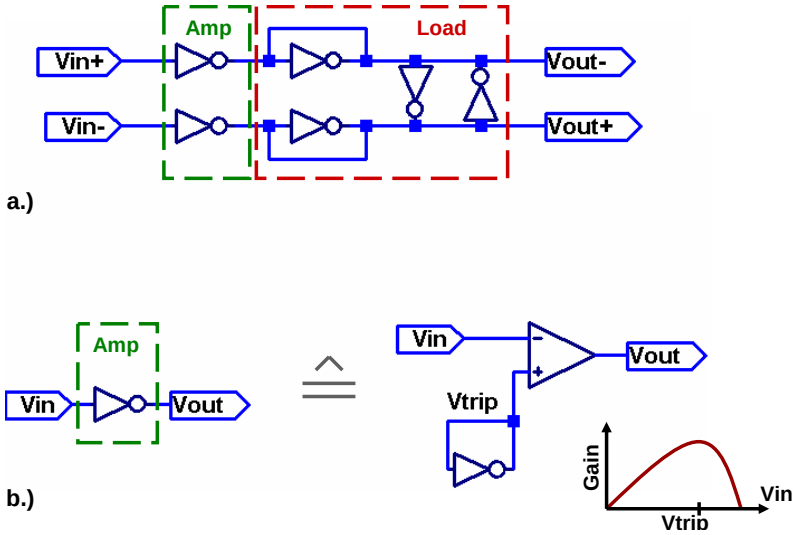


Figure 8.7.: a.) Inverter-based differential opamp [118], b.) inverter with equivalent circuit and illustration of its gain around the trip point voltage V_{trip} .

globally via the quantized feedback, leading to saturation towards the supply rails.

A pseudo-differential inverter opamp (Fig. 8.7a) could have been used instead [118]. These opamps have a load stage that has a high differential resistance and a low common mode resistance to define the common mode output voltage. However, this load stage consumes extra power, reduces the gain and contributes noise. It can be omitted by implementing the whole ADC instead of only the opamp as a pseudo-differential system. In this way, the common mode bias voltage is implicitly defined by single-ended quantized feedback in the positive and negative half-ADCs (Fig. 8.2).

A simple single-ended inverter-based modulator is depicted in Fig. 8.8a. The linearized equivalent circuit in Fig. 8.8b illustrates the implicit common mode control loop, where the gain element k represents both the quantizer gain and the DAC conversion gain. Let two of these modulators form a pseudo-differential ADC with no differential input signal present, so that V_a and all internal voltages are equal to the common mode voltages of the system.

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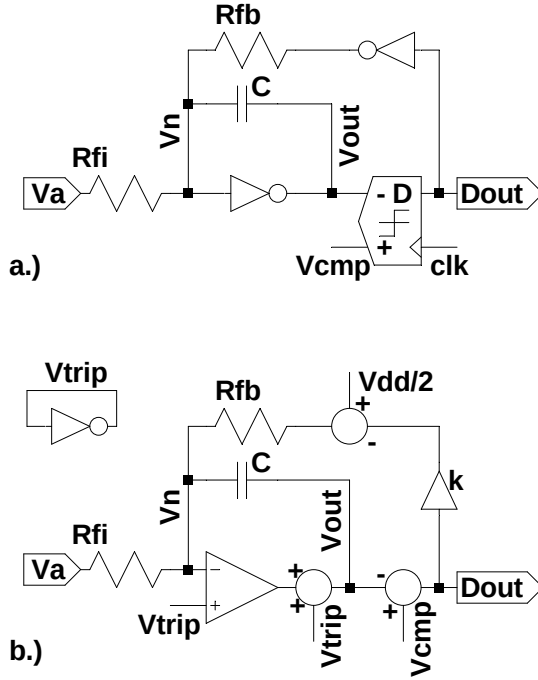


Figure 8.8: a.) Simplified inverter-based modulator, b.) linearized equivalent circuit.

An inverter has maximum voltage gain around its trip point voltage V_{trip} (Fig. 8.7b). Therefore, it is desirable to ensure that the inverter-opamp always operates at its trip point. This requires for all V_a that

$$V_{out} = V_n = V_{trip}. \quad (8.4.1)$$

For maximum dynamic range in differential mode, it is further desirable to ensure that the common mode D_{out} is always zero. Opening the loop by setting $k = 0$ allows to find the condition under which both requirements are fulfilled:

$$V_{cmp} = V_{trip} = V_n = \frac{V_{dd}R_{fi} + 2V_aR_{fb}}{2R_{fi} + 2R_{fb}} \quad (8.4.2)$$

The comparator reference voltage V_{cmp} can be derived in the same way as V_n by a resistive divider from V_a and $V_{dd}/2$. In Fig. 8.2 $V_{dd}/2$ is generated already

implicitly by DAC 2, which compensates the FIR transfer function of DAC 1 at the same time according to the discussions in Section 6.5. In this way, a resistive load due to active or passive summation in front of the quantizer can be avoided. This allows to use an inverter-based OTA instead of a real opamp in the loop filter.

As a side effect from (8.4.2), adding V_a in front of the quantizer via its reference input implements the wideband topology proposed in [122]. This minimizes the swing at the inverter output for reduced distortion due to the decay of the inverter voltage gain around V_{trip} . Self-cascoding has been applied in Fig. 8.5 to relax the required gm -to-resistor matching that determines the achievable gain boost A_{boost} via loss compensation.

The implemented inverter consists of composite transistors at both supply rails. Each contains a stack of four different minimum length devices with successively declining threshold voltages. All five inverters in Fig. 8.5 are implemented with the same unit cells on common bulks.

Adaptive bulk biasing has been implemented to define V_{trip} according to (8.4.2): Digitally-assisted control of V_{trip} guarantees the required DC gain under Process Voltage Temperature (PVT) and input common mode variations. Using the same DC conversion gain for DAC 1 and 2 in Fig. 8.2 and controlling the global bulk potentials V_{bulkp} , V_{bulkn} (Fig. 8.5) in such a way that the mean common mode digital signal $\overline{D_{cm}}$ becomes zero. This equalizes the mean common mode voltages

$$\begin{aligned} \frac{\overline{V_{out-}} + \overline{V_{out+}}}{2} &= \frac{\overline{V_{cmp-}} + \overline{V_{cmp+}}}{2} = \\ \frac{\overline{V_{in-}} + \overline{V_{in+}}}{2} &= \frac{\overline{V_{n-}} + \overline{V_{n+}}}{2} = V_{trip}. \end{aligned} \quad (8.4.3)$$

Table 8.1.: Bulk Control Algorithm

	gm too low	gm too high
$\overline{D_{cm}} < 0$	incr. V_{bulkn}	incr. V_{bulkp}
$\overline{D_{cm}} > 0$	decr. V_{bulkp}	decr. V_{bulkn}

The unit-cell gm is controlled together with V_{trip} by a digital algorithm according to Tab. 8.1. This algorithm monitors $\overline{D_{cm}}$ and controls V_{bulkn} in a

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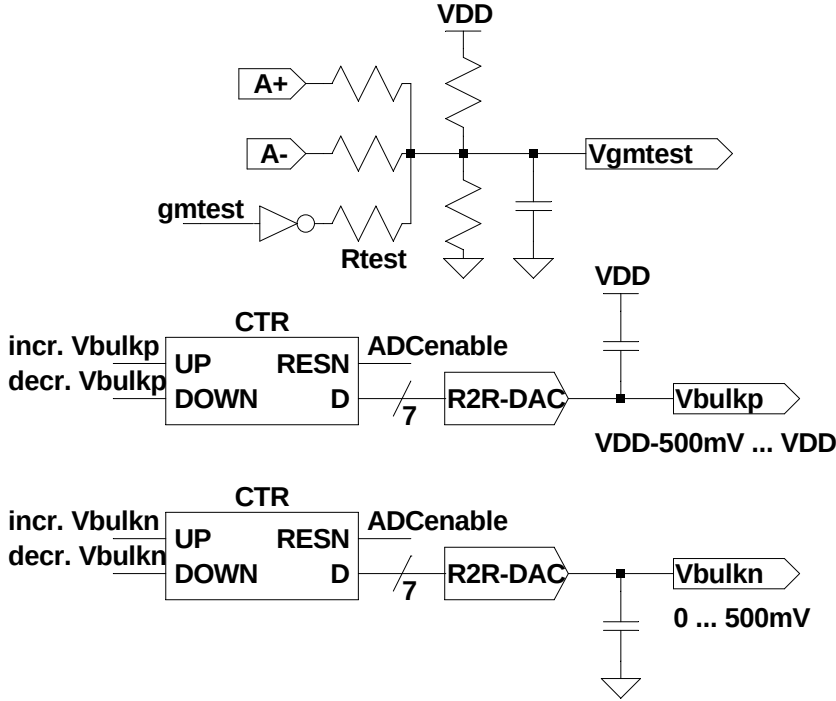


Figure 8.9.: Reference circuit for unit cell g_m measurement and adaptive bulk bias generation.

range of $0 - 500$ mV and V_{bulkp} in a range of 600 mV – 1.1 V respectively via two passive R/2R-DACs (Fig. 8.9).

Switching the global reference voltage V_{gmtest} in Fig. 8.5 between two voltages derived by resistive dividers from VDD allows to extract the unit cell g_m . The conversion gain $\frac{\Delta D_{cm}}{\Delta V_{gmtest}}$ is proportional to $g_m R_i$. In a chip with internal VDD generation, the g_m alignment range can be extended by adjusting VDD in addition to the bulk potentials.

The orthogonality of D_{out} and D_{cm} allows to run the alignment algorithm in the background without disturbing the conversion of the differential signal. However, overloading the quantizers with a strong differential signal may disturb the alignment algorithm. Freezing the state of the algorithm during overload avoids that.

If the inverter- g_m becomes significantly too high, instability may occur, especially at startup when the common mode levels settle. Therefore, the

up/down-counters that control the R/2R-DACs are reset during power-up to start with the smallest possible gm for a stable initial operation of the modulator. A 7-bit resolution and a slow update rate of the alignment DACs prevent them from coupling significant common mode noise via the back gates of the inverters into the modulator.

For reduced finite-GBW-induced ELD, most of the high frequency quantization noise current into the feedback network is provided by the high-pass path C_h and

$$R_h = \frac{R_i R_f R_x}{R_x R_f + R_i R_x - R_i R_f} \quad (8.4.4)$$

instead of the inverter in Fig. 8.5. This unburdens the opamp in a similar way as the assisted-opamp technique proposed in [124]. The idea here is that the limited GBW of the OTA-opamp can have an impact only on the residual current into the feedback network. Fig. 8.10 illustrates this concept for a first

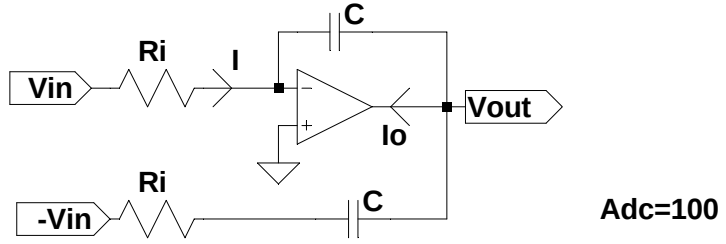


Figure 8.10.: Integrator output assistance using a RC-path.

order integrator. For an ideal opamp, the $-V_{in}$ RC-path modifies the current ratio $I_o/I = 1$ to

$$\frac{I_o(s)}{I(s)} = \frac{2}{1 + sR_iC} \quad (8.4.5)$$

This relaxes the required bandwidth of the OTA. The $-V_{in}$ RC-path also eliminates the right half-plane zero in

$$\frac{V(s)}{V_{in}(s)} = -\frac{1 - sC/gm}{s(R_i + 1/gm)C} \quad (8.4.6)$$

that is caused by finite OTA transconductance gm and restores ideal integration with

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{s(R_i + 2/gm)C}. \quad (8.4.7)$$

This technique allows to operate the inverters with a smaller gm and deeper in weak inversion for reduced power dissipation and lower supply voltage. This applies also to the implemented third order integrator, because at high frequency it falls back to first order integration.

8.5 Pseudo-Differential Modulator Topology

The output common mode voltage of the loop filter $V_{cm} = \frac{V_{out-} + V_{out+}}{2}$ in Fig. 8.2 is defined implicitly by two single-ended quantizer-DAC feedback loops. However, in contrast to a fully-differential design, V_{cm} is not constant in this topology; it rather exhibits quantization noise and it follows the common mode voltage at the ADC input due to the trip point control loop. The resulting differential ADC still achieves a high CMRR by subtracting D_+ and D_- in the digital domain.

The noise in both single-ended modulators is highly decorrelated, because both modulators are only weakly-coupled at the loop filter in Fig. 8.2. An alternative interpretation is that V_{cm} represents a strong dither signal that breaks the correlation of both quantizers that would exist in a fully-differential implementation. The resulting 3 dB SNR-improvement at the digital subtraction corresponds to a quasi-1.5 bit quantization [125] that is not impaired by mismatch-induced out-of-band noise intermodulation at the DAC stages.

However, mismatch of both half-ADCs results in mode conversion, i.e. in-band common mode quantization noise from D_{cm} leaks into the differential output signal D_{out} . The common mode NTF is less pronounced than the differential NTF (Fig. 4.6), because the loop filter resonates and the integrator loss is compensated only in differential mode. The required gain matching of both half-ADCs is determined to first order by the maximum ratio of the in-band common and differential mode noise PSD. In the mostly-digital testchip design this corresponded to only 3% component matching requirements which can easily be guaranteed by compact structures in UDSM

CMOS¹. The matching requirements of the gm stages in particular are dictated mostly by the integrator loss compensation technique. In this design the required gain boost due to this technique is limited to 30 dB which corresponds also to approximately 3 % matching of the transistor threshold voltages.

8.6 Feedback DACs and Quantizer

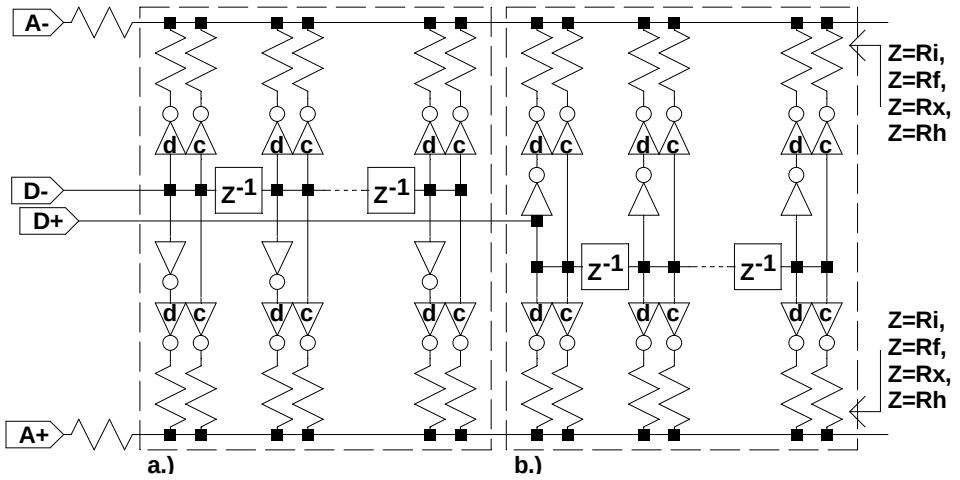


Figure 8.11.: a.) ISI-free FIR-DAC 1 for negative half-ADC, b.) for positive half-ADC.

The DACs 1 and 2 in Fig. 8.2 are implemented as single-bit semi-digital NRZ-FIR-DACs with inverter-resistor taps for good scalability in modern technologies. Inverter-resistor DACs are more linear and less noisy than current-steering DACs, but their lower output impedance increases the amplification of the input referred noise of the first opamp in the loop filter.

¹ The matching of components with given dimensions tends to even improve at shrinking technology feature size. However, at the same time the voltage headroom tends to become smaller which requires to have lower offset and noise and thereby better matching for a given SNRp.

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Integrator loss compensation avoids that noise amplification, making inverter-resistor DACs more attractive. The reference voltage of an Inverter-resistor DAC is its supply voltage VDD . Multiplicative mixing of supply noise with the data signal of the DAC requires a low noise VDD .

Using an NRZ pulse shape and a FIR low-pass transfer function (Fig. 6.17) within the DAC improves not only the robustness to clock jitter [82, 87, 92], but relaxes also the required supply filtering to prevent images of in-band signals and the strong out-of-band quantization noise from demodulating supply noise into the band of interest.

Mixing of in-band signals with low frequency supply noise according to Chapter 5 can be reduced by low noise supply regulation. The mostly-digital testchip has a separate supply domain for the ADC core with off-chip regulation and decoupling to prevent supply noise of the high power LVDS clock-/data interfaces from coupling into VDD . In addition some on-chip supply decoupling has been implemented. For reasons of simplicity Metal Isolator Metal (MIM) decoupling capacitors have been placed in void areas besides the ADC core. In a SoC environment without any void area on the metal levels, MOS capacitors could be placed below the MIM capacitors of the loop filter for this purpose without requiring extra chip area.

The FIR-DACs and the gm stages share the same supply within the ADC core. In a first order approximation and neglecting switching transients this keeps the supply current constant despite single-ended operation, because depending on the data at the input of the feedback DAC, the current flows from VDD to ground either via the inverters of the FIR-DAC into the gm inverter gain stage of the integrator or vice versa via the gm inverter into the FIR-DAC inverters.

The JNR-DAC structure from Section 6.4 has been implemented in addition to FIR-DAC 1 in Fig. 8.2 for the R_i feed-in path (Fig. 8.5) only because the jitter-induced noise in the other feed-in paths is already high-pass shaped.

Using the same time-constant for $R_i C_i$ in Fig. 6.10 and for $R_x C_x$ in Fig. 8.5 allowed to simplify the implementation by omitting branches with currents that cancel at the virtual ground of the integrator and merging others. Therefore, the design effort has been limited to extending the shift-register by one D-flip-flop and recalculating the FIR coefficients.

The transfer function of FIR-DAC 1 is compensated using FIR-DAC 2 in Fig. 8.2. The small required gain of the compensation loop around the quantizer intuitively calls for a passive implementation by a resistive network that

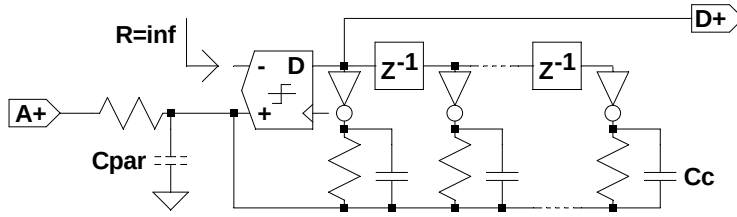


Figure 8.12.: Compensation FIR-DAC 2 with swing minimization, cancellation of parasitic pole and load-free subtraction using a differential comparator.

sums up the FIR taps and the ADC input signal (Fig. 8.12). Small parallel capacitors C_c have been added at the FIR taps to compensate the limited bandwidth of the poly resistors and the parasitic capacitance C_{par} at the comparator input [47].

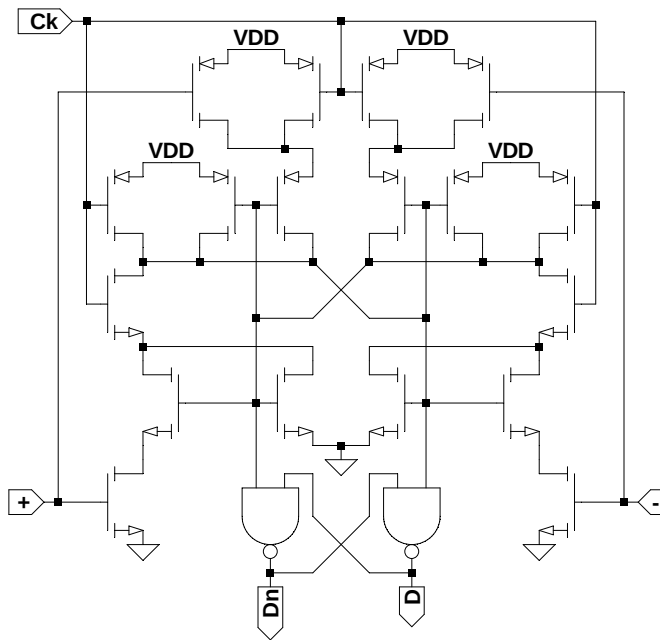


Figure 8.13.: Rail-to-rail compatible dynamic latched comparator.

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Using both input terminals of a differential comparator to perform single-ended subtraction minimizes the load for the loop filter inverter-OTA to preserve high DC gain and low power consumption (Fig. 8.12). This comparator must have a rail-to-rail input common mode range to enable a safe startup of the ADC.

The proposed dynamic latched comparator is depicted in Fig. 8.13. It has a complementary input stage for a large input common mode range and for a short decision time at small differential input voltages due to a higher drive capability of its regenerative latch than traditional latched comparators [107]. It also has a lower complexity and current consumption than other rail-to-rail latched comparators [126]. There are no static currents in this design and all internal nodes are discharged during the low clock phase to avoid an offset that depends on the previous decision.

The input signal of FIR-DAC 1 is delayed in Fig. 8.2 by half a sampling period for reduced impact of quantizer metastability on the first tap.

A single-ended operation of NRZ-DACs gives rise to ISI-induced non-linearity [11, pp. 113–114]. A linearization technique for DAC 1 is proposed that is able to convert the error charges at the integrator due to ISI into a common mode signal. In Fig. 8.11 all single-ended taps are split into two differential taps (marked with 'd') and two common mode taps (marked with 'c'). Matching ensures that the differential taps are ISI-free, while the ISI-distortion of the common-mode taps is canceled by digital subtraction. This structure remains a single-ended DAC for each half-ADC, because the low-side taps in Fig. 8.11a and the high-side taps in Fig. 8.11b do not contribute due to opposite polarity.

Each of the feed-in resistors in Fig. 8.5 represents the output impedance of such a linearized single-ended FIR-DAC. The -1 gain stage that drives R_x and R_h is realized by inverting the FIR taps and exchanging A_+ and A_- in Fig. 8.11. All FIR-DACs share a common 6-stage shift register (not shown).

8.7 Optimizer-based Design

In Sections 6.6 and 6.7, two design methods for modulators based on the IIR-quantizer have been discussed that require determination or optimization of one parameter by simulation. Instead of using one of these approaches that require transient simulation anyway, a fast transient-simulation-

based optimization of the whole modulator has been used to design the testchip.

The concept behind this optimization is to reduce the number of significant degrees of design freedom as much as possible and then to automatically step through the design space and simulate the peak SNDR with a Simulink model at each step. On state of the art PCs this optimization is a matter of minutes, since each simulation requires only a fraction of a second.

Rewriting (4.2.5) with

$$A_0 = sH_0(s) \frac{R_{DC}}{R_i}, \quad (8.7.1)$$

$$f_2 = \sqrt{\frac{f_x f_f}{1 - \frac{R_i}{R_x} + \frac{R_i}{R_f}}} \quad (8.7.2)$$

and

$$Q = \frac{1}{\left(\frac{1 - \frac{R_i}{R_x}}{f_x} + \frac{1 + \frac{R_i}{R_f}}{f_f} \right) f_2} \quad (8.7.3)$$

yields

$$L_{diff}(s) = -\frac{A_0}{s} \frac{\frac{s^2}{(2\pi f_2)^2} + \frac{s}{Q 2\pi f_2} + 1}{\frac{s^2}{(2\pi f_0)^2} + 1}. \quad (8.7.4)$$

The parameter f_0 defines the location of the conjugate complex NTF zeros. Since for low-pass modulators this frequency is far away from the transit frequency f_T of the modulator loop, it does not have a significant impact on the stability of the loop which depends mostly on parameters A_0 , f_2 and Q .

The frequency f_0 depends only on the desired bandwidth. Optimum values of f_0 for various modulator orders can be found in [10, pp. 107–111]. For a third order modulator the optimum frequency is $f_0 = \sqrt{3/5}BW$ where BW is the bandwidth of interest.

The parameter Q is the quality factor of the two numerator zeros, where $Q \leq 0.5$ means real zeros, $Q = 0.5$ means real zeros at the same frequency, $Q > 0.5$ means conjugate complex zeros, and $Q = 0.7$ means zeros in maximally flat Butterworth configuration.

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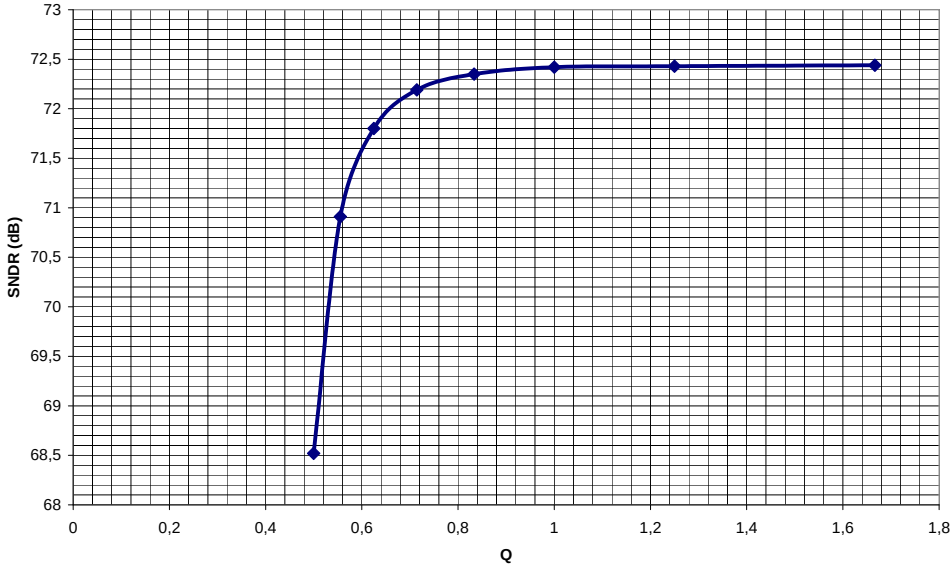


Figure 8.14.: SNDR plot for third order modulator with $OSR = 32.5$ versus quality factor Q .

Fig. 8.14 shows an exemplary SQNR versus Q plot for a third order modulator with single-bit quantization at $OSR = 32.5$ and $H_\infty = 1.6$. Empirically, no significant dependence of the peak SQNR on Q has been found if Q is above 0.7 ².

With increasing Q , the peaking in the quantization noise at the transition region from the band-of interest to the strong high frequency quantization noise becomes higher (Fig. 8.18). Hence, Q should not be chosen larger than necessary; a quality factor $Q = 1$ has been found to be a good choice for most designs.

With fixed f_0 and Q , the only unknown parameters of the loop filter are A_0 and f_2 .

² Significant deviations from this empirical rule have been found only for very low OSR.

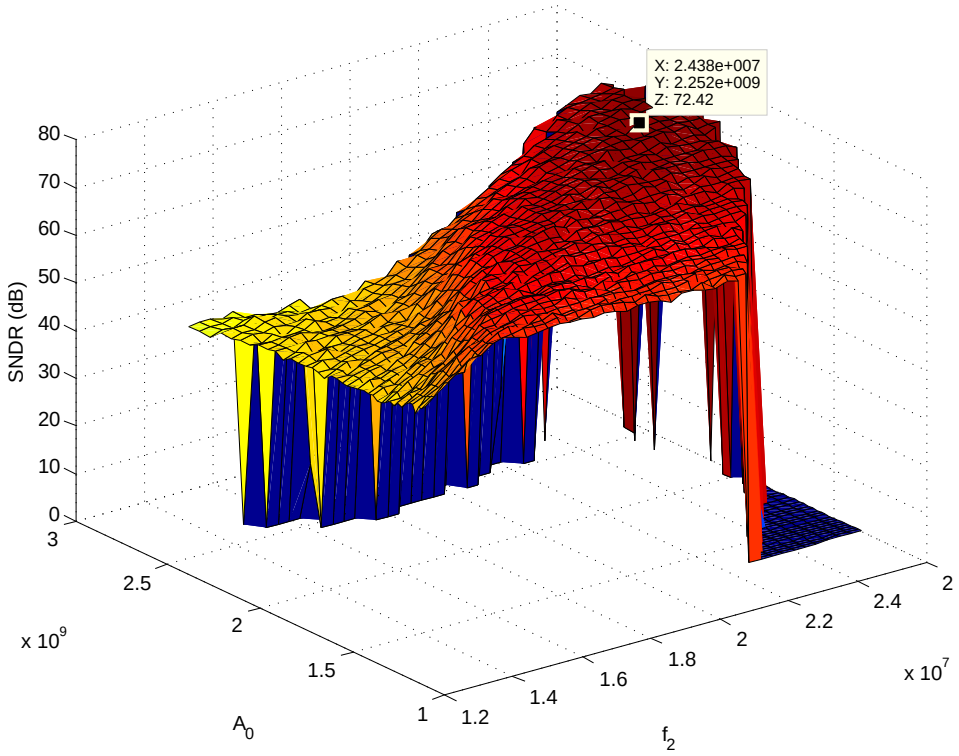


Figure 8.15.: Optimizer plot for third order modulator with $OSR = 32.5$ and $Q = 1$.

Hence, the proposed design procedure for a third order modulator with IIR-quantizer becomes the following:

1. Define the desired Transfer Function (TF) of FIR-DAC 1, obeying $b_0 = 1$ and $b_1 + \dots + b_n = n$.
2. Derive the coefficients of FIR-DAC 2 with $a_1 = b_1, \dots, a_n = b_n$.
3. Define the desired bandwidth of interest, OSR and maximum stable amplitude.
4. Select a quality factor Q that determines the amount of peaking of the quantization noise.

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5. Start the optimizer.
6. Select a data point in the 3D plot (Fig. 8.15) that is sufficiently far away from the edges of the SQNR surface such that PVT parameter variation can be tolerated.
7. Define the parameters a and b for the third order CXX resonator (Fig. 4.2).
8. Rerun the optimizer in single-step mode to obtain the output spectrum and the SPICE include file that contains the calculated RC component values.
9. Run the automatically generated LTspice schematic to simulate the equivalent thermal input noise level of the loop filter.
10. Adjust the parameter for the impedance level of the loop filter and repeat the last two steps until the RMS level of the thermal noise is approximately 6 dB above the RMS level of the quantization noise within the band of interest. This ensures that the quantization noise contributes with only approximately 1 dB to the total noise which yields a good compromise of power-efficiency and usable bandwidth.

A simplified single-ended Simulink model that has been used during the optimization is shown in Fig. 8.16. For ELD compensation the Simulink model shown in Fig. 8.17 has been used to determine the impulse response due to the deliberately introduced delay of half a clock cycle.

Opamp GBW-induced ELD has not been considered for the optimization for this mostly-digital testchip, because the single-stage inverter has a very high bandwidth and also the RC high-pass opamp assistance relaxes the GBW-requirements.

For the ELD compensation only the first sample of the impulse response is considered to implement a direct path around the quantizer, because later samples are much less significant for stability and the FIR-DAC relaxes the impact of ELD anyway.

Integrator scaling is done implicitly via optimizing the parameter A_0 if the output voltage range of the opamp is at least as large as the overload-free input voltage range of the quantizer which is always smaller than the supply voltage. For the second and third order integrators that have been discussed

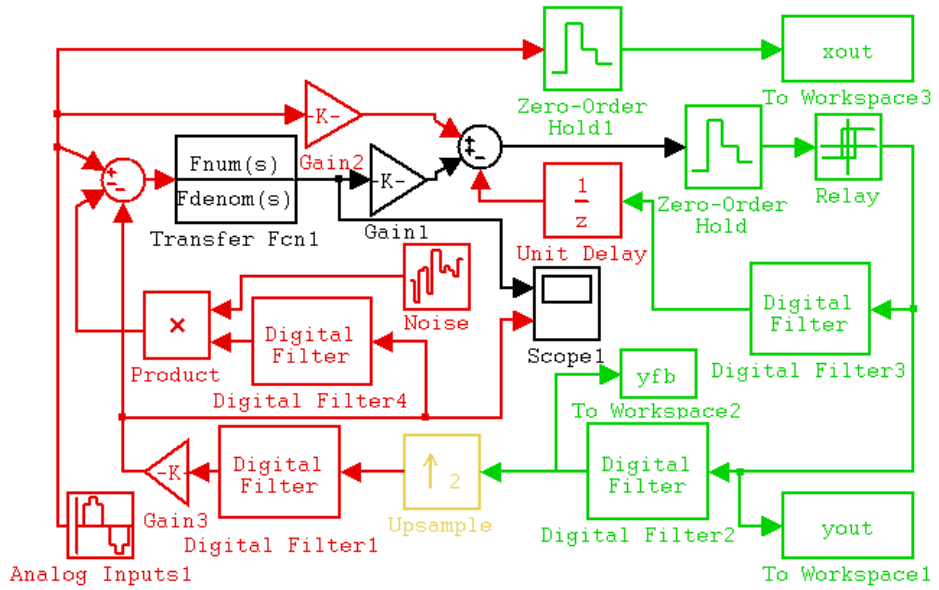


Figure 8.16.: Simulink model that was used for optimization.

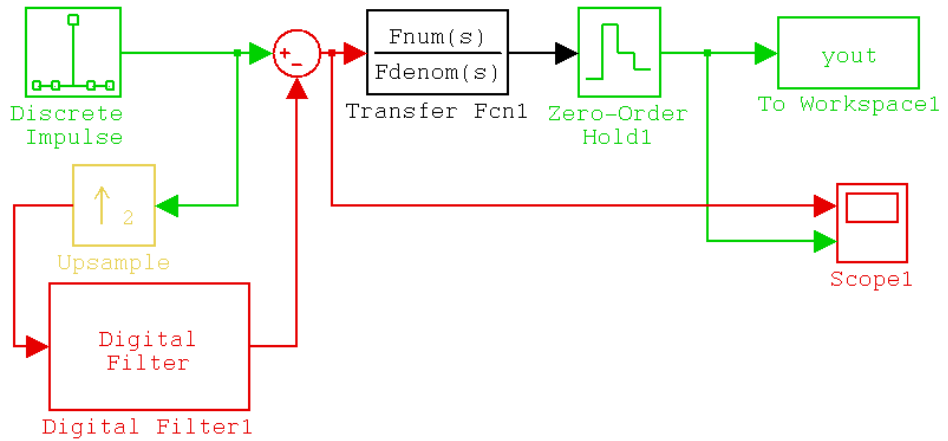


Figure 8.17.: Simulink model that was used for ELD compensation.

in Chapter 4, there are no internal nodes that can saturate. Thus, for a third order modulator no further scaling is required.

A benefit of this optimizer approach is that many non-idealities can be included in the optimization of the NTF, whereas tools such as Schreier's $\Sigma\Delta$ -Toolbox [27] for MatLab do not allow to do that.

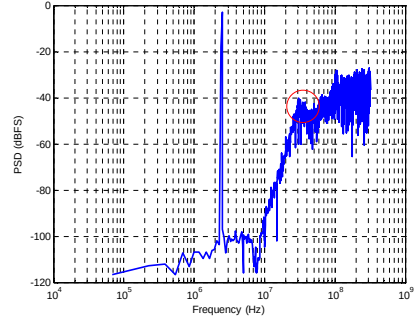
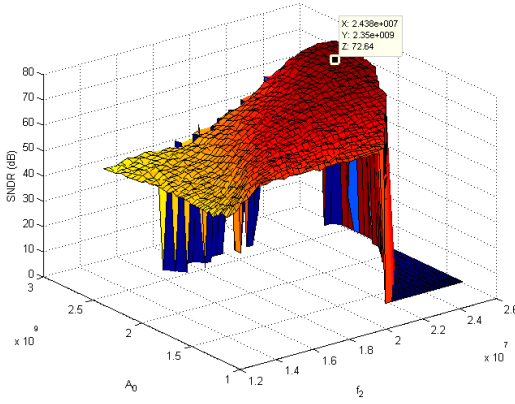
For example, in Chapter 5 the folding mechanism of clock phase noise and quantization noise has been discussed. For a given phase noise mask, there is an optimum NTF, that results in the lowest jitter-induced in-band noise.

Thus, for high performance ADCs that are clocked by a PLL it makes sense to optimize the NTF not only for low in-band quantization but also for low jitter-induced noise. This can be done with the model in Fig. 8.16, where the discrete-time approximation of the folding mechanism has been implemented for white phase noise. Colored phase noise requires to modify the amplitude noise source in Fig. 8.16 accordingly.

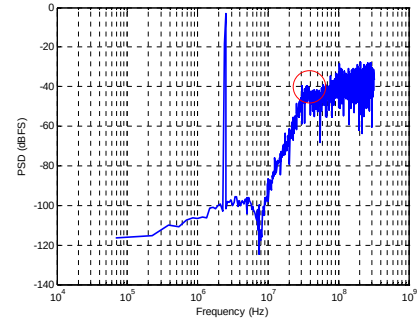
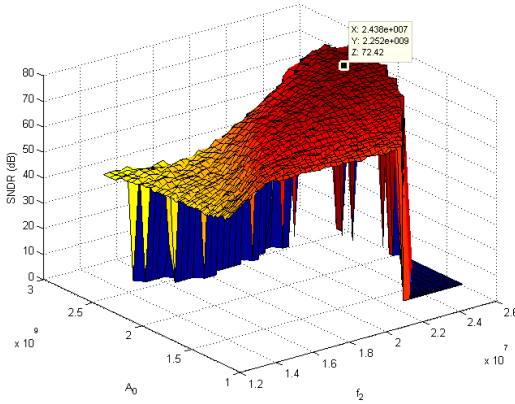
Another example is the droop in the Bode-plot of the JNR-DAC that has been discussed in Chapter 6. It can be included with minor modifications to Fig. 8.16. And a last example is the pseudo-differential modulator topology that has been discussed in Section 8.5. This topology can also be modeled and included in the optimization³.

³ Although in terms of stability, no significant difference has been found for the pseudo-differential and the single-ended version.

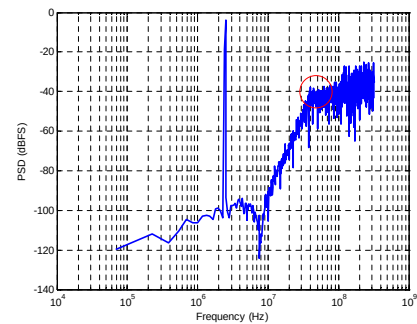
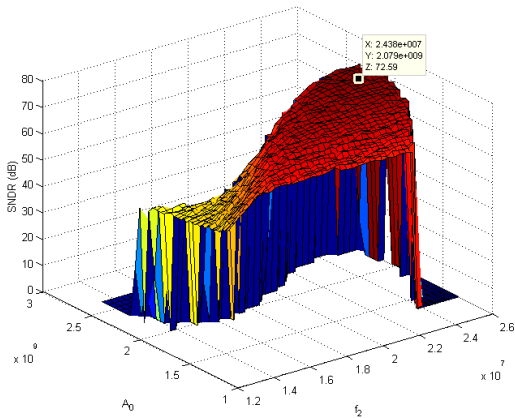
8.7. Optimizer-based Design



$Q=1.3$



$Q=1$



$Q=0.7$

Figure 8.18.: Optimizer plots for third order modulator with $OSR = 32.5$ and different quality factors.

8.8 Implementation and Testbench

A simplified top schematic of the complete ADC that has been implemented is shown in Fig. 8.19. This mostly-digital testchip has been implemented with Cadence Virtuosos 6 using Mentor Graphics Calibre for layout verification and post layout simulation (Fig. 8.20). It has been manufactured by STMicroelectronics in a 65 nm dual- V_t , triple gate oxide two poly seven metal CMOS process with MIM-capacitors (Fig. 8.21).

The dice have been mounted in a QFN24 package and the chip is supplied with 1.1 V from two voltage regulators via separate pins for the LVDS-IO-interface and the ADC core.

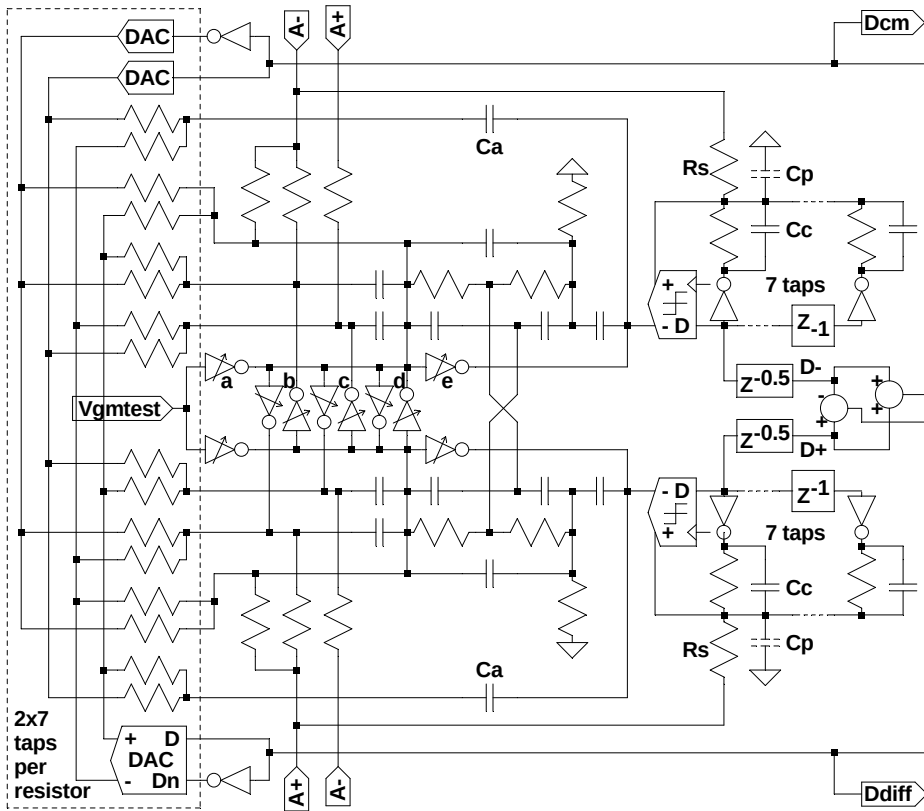


Figure 8.19.: Simplified schematic of the complete CT- $\Sigma\Delta$ modulator.

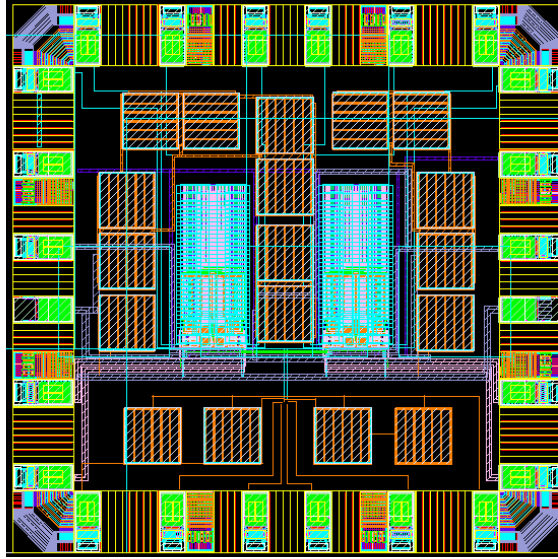


Figure 8.20.: Top layout of the mostly-digital testchip 2.

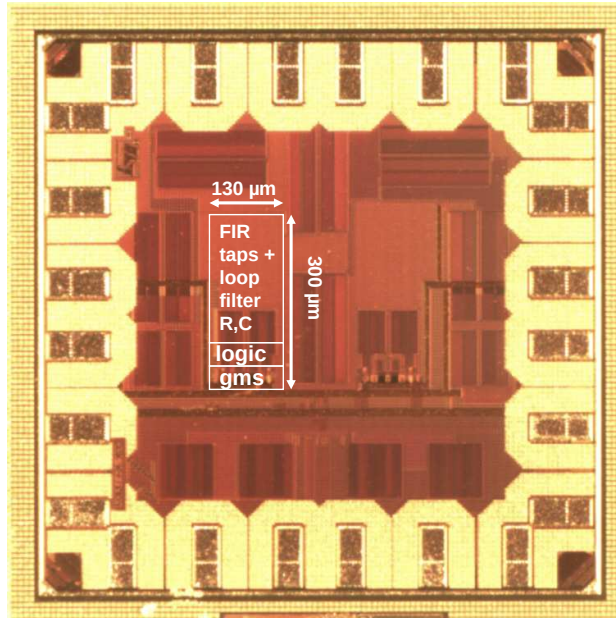


Figure 8.21.: Die micrograph of the mostly-digital testchip 2 in 65 nm CMOS.

8. Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

The RC-product of the process can be measured reusing the gm test circuitry. Temporarily replacing R_{test} in Fig. 8.9 with a switched capacitor resistor (not shown) allows to measure the RC-product after the settling of the gm control loop. The PLL-clock is initially set assuming low R and C process corners to obtain a stable loop for the measurement of the RC-product. It is then adjusted to the measured RC-product; no RC-trimming-circuitry has been implemented on this mostly-digital testchip, but circuit area has been reserved for capacitor trimming.

8.9 Measurement Results

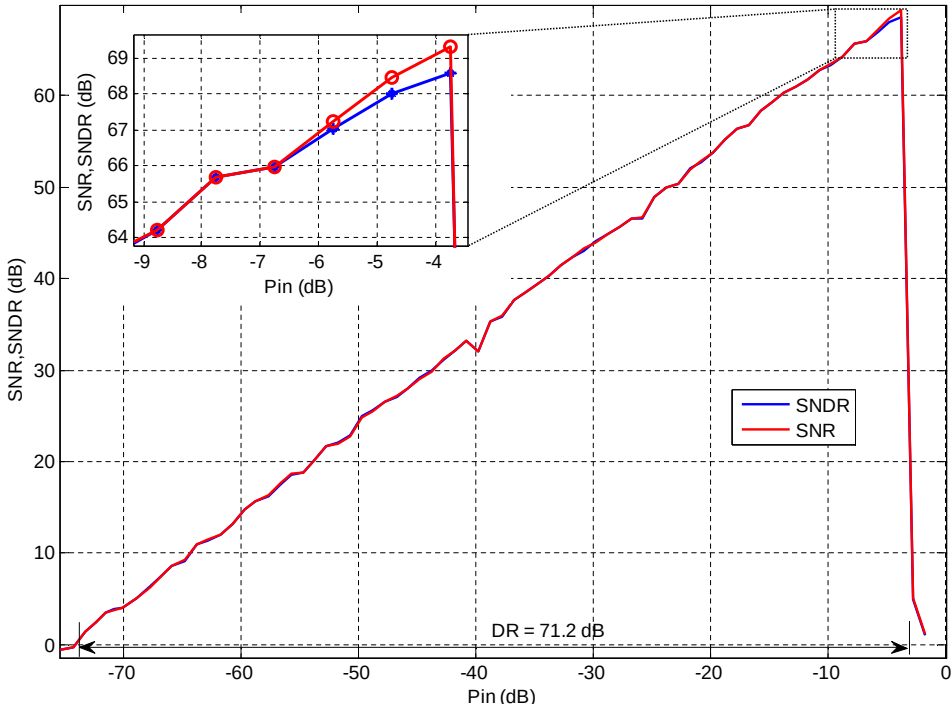


Figure 8.22.: Differential SNR/ SNDR (BW=10 MHz) sweep for a 1 MHz test signal.

Fig. 8.22 shows the measured differential SNR/ SNDR in the 10 MHz BW of interest as a function of the amplitude of a 1 MHz test signal. Fig. 8.23 and Fig. 8.24 show the PSDs of the captured bitstream for 1 MHz and 10 MHz

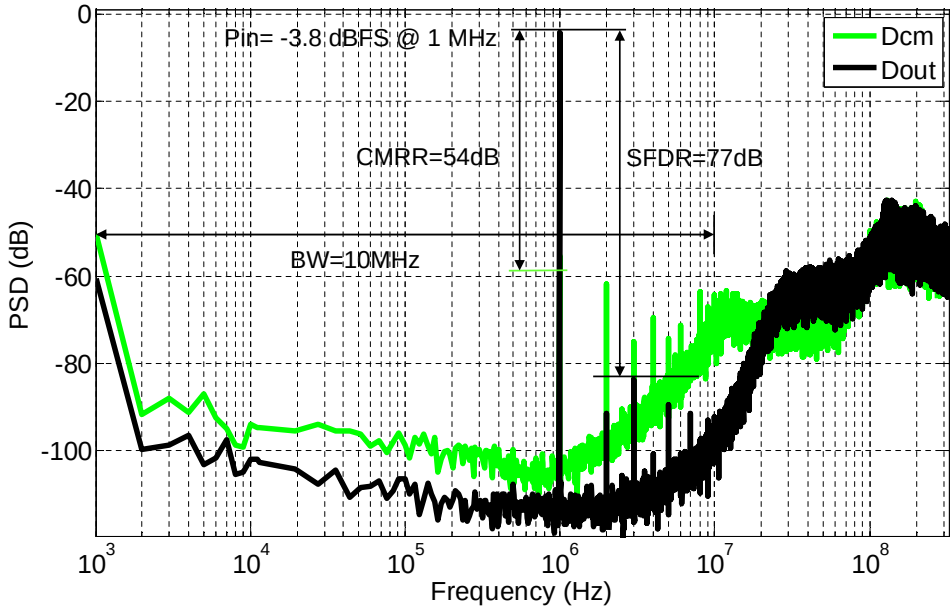


Figure 8.23.: PSDs of the differential and common mode bitstream output signals for a 1 MHz test signal.

test signals. Both the differential output signal D_{out} and the common mode output signal D_{cm} show strong quantization noise close to $f_s/2$. This is the internal quantization noise of the IIR-quantizer.

FIR-DAC 1 in Fig. 8.2 suppresses this noise very effectively because according to the IIR-quantizer concept, it is designed to have the reciprocal transfer function of the internal NTF (6.8.1) of the quantizer. The ADC offers excellent immunity against clock jitter for this reason. Inserting an LVDS buffer chain at the 650 MHz sampling clock input to increase the measured RMS phase jitter from 0.5 ps to 10 ps did not degrade the measured peak SNR.

The differential output signal D_{out} shows a slightly higher noise leakage from the common mode signal D_{cm} at the upper edge of the BW of interest than expected. This has been found to be caused by mismatch between both half-ADCs due to non-optimum layout of the inverter- gm -stages.

8. Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

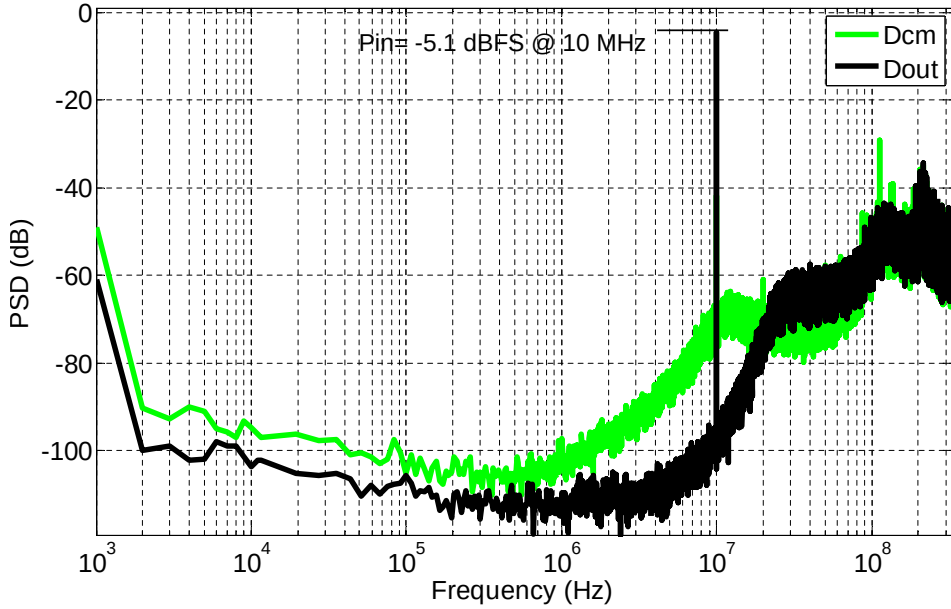


Figure 8.24.: PSDs of the differential and common mode bitstream output signals for a 10 MHz test signal.

The measured CMRR is 54 dB which corresponds to the distance between the differential and the common mode PSDs at 1 MHz in Fig. 8.23. In Fig. 8.25, the effect of a 1.5 MHz test signal that is injected into VDD with the same amplitude as a 2 MHz differential test signal is shown. Its leakage into D_{out} depends on the DC offset at the ADC input. The measured Power Supply Rejection Ratio (PSRR) is in good accordance with the measured DC offset. However, sidebands due to multiplicative mixing are present independently of the DC offset.

The STF is shown in Fig. 8.26. It peaks at high frequency due to (6.8.1) and rolls-off afterwards due to the limited bandwidth of the poly resistors at the ADC input.

Finally, Fig. 8.27 and Fig. 8.28 show the robustness of the ADC versus variations of supply voltage and ambient temperature, which is approximately equal to the die temperature due to the very small power dissipation of the chip.

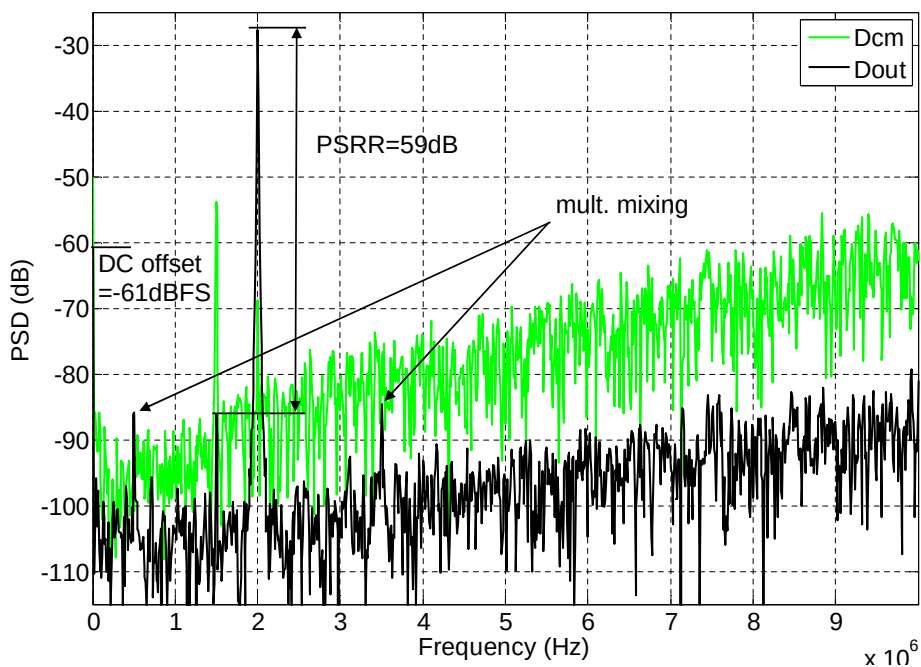


Figure 8.25.: PSDs of the bitstream output signals for a 2 MHz differential test signal under the influence of supply noise at 1.5 MHz with equal amplitude.

All other measurement results are in good accordance with simulations. The performance of this testchip is summarized in Tab. 8.2.

Table 8.2.: Performance Summary

Technology	65 nm	f_s	650 MHz
Area	0.039 mm ²	FoM	$41.4 \frac{fJ}{conv.-step}$
P_{diss}	1.82 mW	SFDR	77 dB
$SNDR_p$	68.6 dB	Supply	1.1 V
BW	10 MHz	SNR_p	69.3 dB
FoM_2	166 dB	MSA	-3.5 dBFS

8. Testchip 2: A Mostly-Digital Continuous-Time $\Sigma\Delta$ -ADC

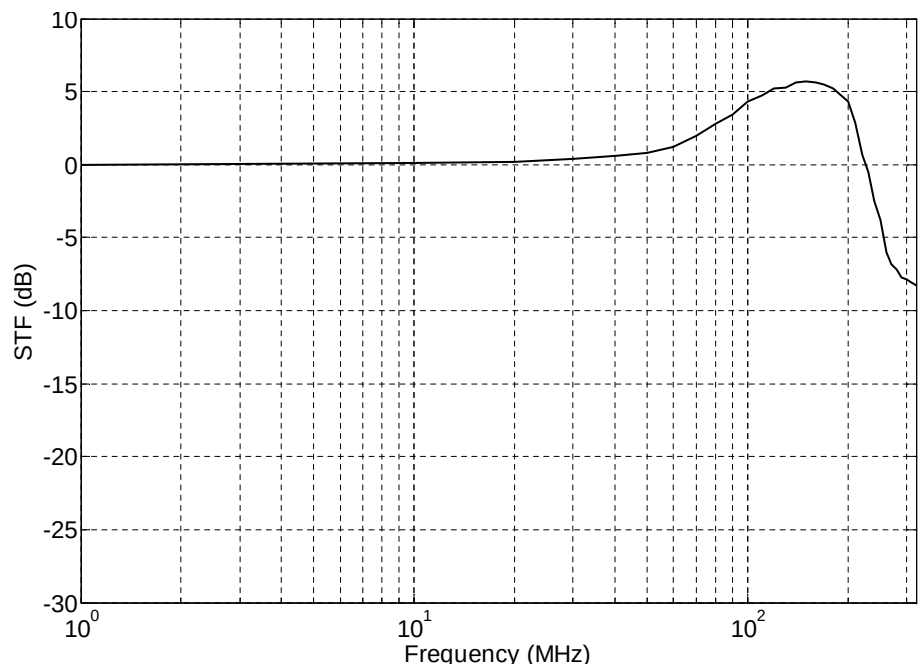


Figure 8.26.: Measured STF.

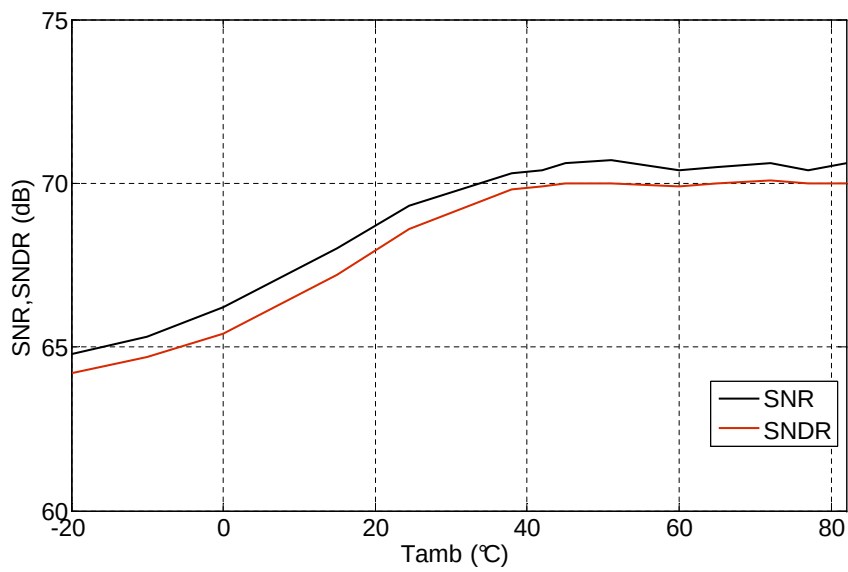


Figure 8.27.: SNR, SNDR versus ambient temperature.

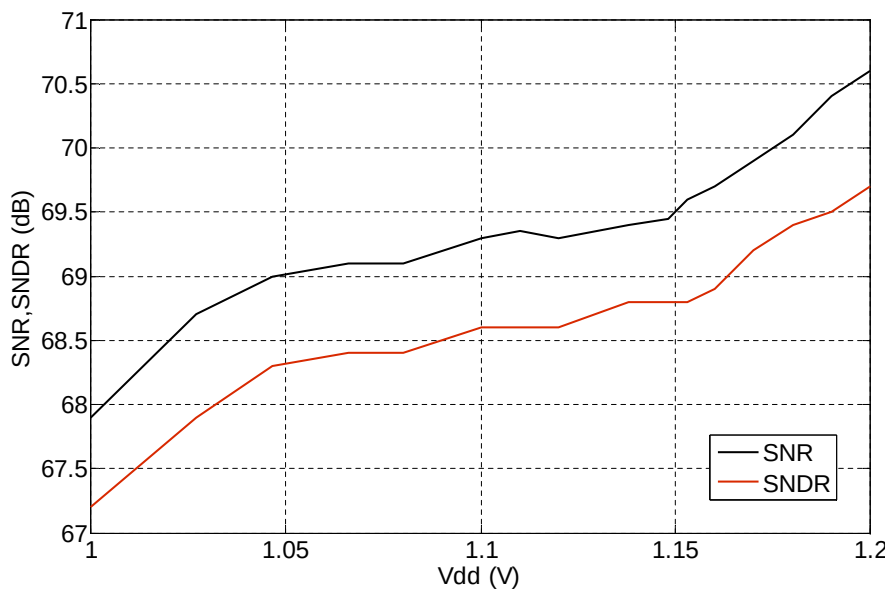


Figure 8.28.: SNR, SNDR versus supply voltage.

9 Conclusion

In this Chapter the contributions of this work are summarized. Moreover, the performance of the second implemented testchip is compared with state of the art publications and an outlook to future works is given.

9.1 Summary of Original Contributions

In this work, the following novel design techniques for improving the power- and area-efficiency of CT- $\Sigma\Delta$ -ADCs at the loop filter, DAC and quantizer stages and at the topology level have been introduced:

- **A class of cross-coupled single-opamp resonators** that allow to reduce the number of opamps in RC-loop-filters of low- and band-pass CT- $\Sigma\Delta$ -modulators. These resonators have been extended in various ways to enable the implementation of resonant second and third order single-opamp loop filter building blocks. Low-power NTF-zero-optimized CT- $\Sigma\Delta$ -modulators with any order larger than one can be implemented by cascading those building blocks.
- **Two compact passive FIR-DAC concepts** that do not require expensive DAC linearization and compensation of the FIR transfer function within the loop filter. Rigorous analysis of jitter and DAC reference noise folding mechanisms has led to a single-bit Jitter Noise Reduction DAC using standard NRZ pulses and an intrinsically linear variant of a multi-bit tracking ADC using a quantizer embedded in a semi-digital IIR-filter; the so called IIR-quantizer. A rapid optimizer-based design method for CT- $\Sigma\Delta$ -ADCs that is considering parasitic effects such as clock jitter has been proposed to design robust modulators based on these concepts.

- **An integrator loss compensation technique** that is using negative impedance to boost the DC gain of integrators without compromising linearity. This technique allows to implement high performance RC-loop-filters using single-gain-stage opamps that do not require frequency compensation. A wideband CMOS-inverter-based opamp with digitally-assisted background PVT stabilization and RC-assistance has been proposed for this purpose.
- **A pseudo-differential CT- $\Sigma\Delta$ -ADC architecture** with intrinsically linear decorrelated dual quantization that improves the SQNR by 3 dB. In addition, the common mode voltages are stabilized using pseudo-differential quantized feedback in order to avoid wasting power in extra stages for local common mode control. A linearization technique for single-ended NRZ-DACs and a rail-to-rail capable dynamic latched comparator complement this technique.

These concepts scale well for future CMOS technology nodes and may be useful even beyond the field of CT- $\Sigma\Delta$ -ADCs. Some of these techniques have been recognized as important innovations in the field of $\Sigma\Delta$ -ADCs [115].

9.2 Benchmark

Two testchips proving these concepts have been implemented:

The first mostly-analog testchip served as a test vehicle for design techniques such as the cross-coupled single-opamp resonator and the JNR-DAC [68, 69, 71, 108, 132–134]. This testchip showed that ninth order NTF zero-optimized noise shaping is possible with an active-RC loop filter that consists of only five opamps.

Moreover, compared to the standard single-bit CT- $\Sigma\Delta$ -modulator architecture significantly higher jitter-robustness has been achieved despite power- and area-advantageous single-bit quantization and NRZ-DAC pulses.

A more refined second mostly-digital testchip has been implemented to prove the effectiveness of the novel concept for power- and area-efficiency in UDSM technologies [93, 116, 135–137]. This testchip has been implemented with a minimalistic active analog section of only 10 CMOS inverters. It occupies a silicon area of only 0.039 mm^2 in 65 nm CMOS and consumes only 1.82 mW from a 1.1 V supply.

Table 9.1.: Comparison with Prior Art

	This	ISSCC	VLSI	ISSCC	ISSCC	ISSCC	VLSI	ISSCC	ISSCC	ISSCC	VLSI	VLSI	VLSI	VLSI
	work	'06[39]	'12[117]	'12[83]	'12[94]	'12[41]	'13[61]	'9[64]	'11[47]	'11[60]	'12[127]	'12[128]	'14[129]	'15[130] '15[131]
Tech. (nm)	65	130	40	90	45	90	28	110	45	90	90	65	20	130 40
Area (mm ²)	0.039	1.2	0.051	0.12	0.49	0.23	0.08	0.32	0.9	0.15	0.36	0.075	0.1	0.08 0.019
P _{diss} (mW)	1.82	20	2.57	15	20	8.5	3.9	5.32	260	8	16	11.5	23	7.2 5.25
SNDR _p (dB)	68.6	74	70	70.9	60.6	67.5	73.6	62.5	65	63.5	76.6	69	67.5	75.3 66.9
BW (MHz)	10	20	10	36	60	25	18	10	125	25	10	20	80	10 40
f _s (MHz)	650	640	300	3600	6000	500	640	300	4000	500	600	1300	2814	640 2400
FoM ($\frac{f_s}{P_{conv}}$)	41.4	122	50	72.8	190	88	27.7	240	710	130	145	123	74.2	75.7 36.3
SFDR (dB)	77	85	79.6	73.5	75	79	80.5	64.2	75.7	81	85.3	82		94.1 73
Supply (V)	1.1	1.2		1.2	1.4/1.8	1.2	1.2/1.5	1.1	1.1/1.8	1.2	1.0/1.4	0.9	1.0/1.2/1.5	1.2
SNR _p (dB)	69.3	76		76.4	61.5	69.1		68.2	65.5	64	80.5	70	70	75.5

9. Conclusion

The measured peak SNR/SNDR is 69.3 dB/68.6 dB within 10 MHz usable bandwidth, the SFDR is 77 dB and the FoM according to (2.2.2) is 41.4 fJ/conv.-step.

Tab. 9.1 compares the performance of this design with state of the art CT- $\Sigma\Delta$ -ADCs in the class with more than 10 MHz usable bandwidth and with other mostly-digital ADCs [128, 138]. This ADC is one of the smallest and most power-efficient designs published so far.

9.3 Future Work

Minimizing the analog sections of CT- $\Sigma\Delta$ -ADCs using robust and scalable circuit concepts such as FIR-DACs or digitally-assisted techniques has and continues to become a major trend in state of the art CT- $\Sigma\Delta$ -ADC design for UDSM technologies [115, 129–131]. At low bandwidths of interest passive circuit concepts will become more attractive [37], while at higher bandwidths CT- $\Sigma\Delta$ -ADCs using minimalistic active sections will further evolve.

For example, the second testchip presented in this work still has considerable potential for further optimization of the loop filter towards reduced thermal noise. Preliminary investigations indicate that shifting the definition of the numerator polynomial of the loop filter transfer function from the feed-in network to the output of the loop filter and using the Chh cross-coupled notch instead of the CXX structure could significantly lower the FoM.

Furthermore, the very high bandwidth of the inverter gain stages should allow to increase the bandwidth of this design significantly and the high slew rate of these stages together with the loss compensation technique and the inverter-resistor FIR-DAC concept might enable highly linear data conversion, which is necessary for future wideband receiver architectures that digitize not only single channels but whole frequency bands that contain many channels at diverse power levels.

A Appendix

A.1 Derivation of Cross-coupled Resonator from Multistage Polyphase RC-Filters

Polyphase Active RC Low-Pass Resonator

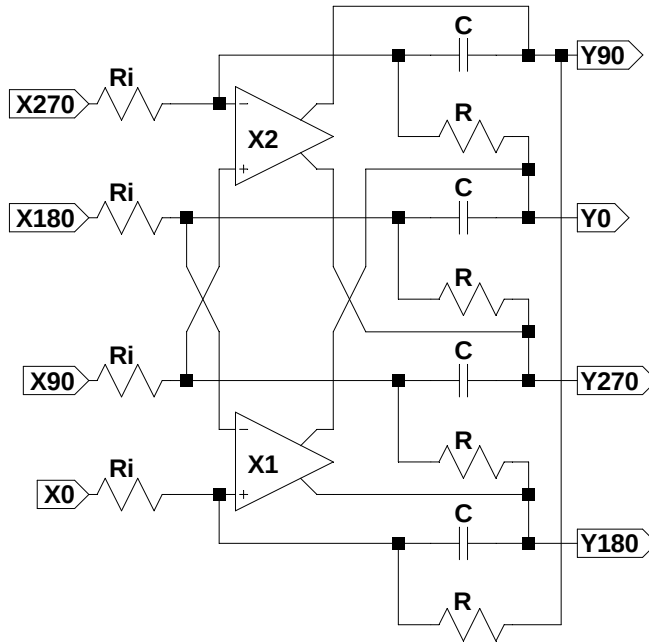


Figure A.1.: Polyphase active-RC low-pass resonator.

Fig. A.1 shows a complex polyphase notch filter that is placed in the feed-back of two operational amplifiers. There is one frequency (either positive or

negative) which is completely suppressed by the notch filter. Hence, the gain of this stage becomes the open loop gain of the opamp at this frequency.

At frequencies with a magnitude that is higher than the magnitude of the notch frequency the admittance of the capacitors dominates over the admittance of the resistors and the stage approximates the frequency response of an integrator. Thus, in total this stage represents a complex low-pass resonator (Fig. A.2).

For a complex input signal

$$X_0(s) = jX_{90}(s) = -X_{180}(s) = -jX_{270}(s) \quad (\text{A.1.1})$$

one complex pole at either $+j\omega_0$ or $-j\omega_0$ is obtained and the transfer function becomes

$$H_{QI}(s) = \frac{Y_0(s)}{X_0(s)} = \frac{Y_{90}(s)}{X_{90}(s)} = -H_{BP}(s) - jH_{LP}(s) = -\frac{R}{R_i} \frac{1}{j - sRC}. \quad (\text{A.1.2})$$

And for a complex input signal

$$X_0(s) = -jX_{90}(s) = -X_{180}(s) = jX_{270}(s) \quad (\text{A.1.3})$$

the transfer function becomes

$$H_{IQ}(s) = \frac{Y_0(s)}{X_0(s)} = \frac{Y_{90}(s)}{X_{90}(s)} = -H_{BP}(s) + jH_{LP}(s) = -\frac{R}{R_i} \frac{1}{j + sRC}. \quad (\text{A.1.4})$$

Multistage Polyphase Active RC Low-Pass Resonator

Several passive polyphase RC notch filter stages can be cascaded. This is a common configuration for image reject filters in RF receivers because it allows to increase the bandwidth where high image suppression is obtained and it improves the robustness of the filter against RC spread.

Cascading is also possible in the feedback of an active polyphase RC low-pass resonator (Fig. A.3). In this way, one independent complex pole per stage is obtained (Fig. A.4).

In the following subsection it will be shown how this technique can be adapted to low-pass $\Sigma\Delta$ -ADCs with real signals.

RCXX Resonator

Passive polyphase RC filter stages can be also cascaded with opposite RC rotation (Fig. A.7). Equal R s and C s in both stages yield a conjugate complex pair of poles.

Complex filters can be driven by real signals, because any real signal can be represented by a sum of two complex signals. For

$$X_0 = X_{90} = -X_{180} = -X_{270}, \quad (\text{A.1.5})$$

it becomes

$$Y_0 = Y_{90} = -Y_{180} = -Y_{270} \quad (\text{A.1.6})$$

and¹

$$V_0 = V_{90} = -V_{180} = -V_{270} \quad (\text{A.1.7})$$

for reasons of symmetry.

Thus, the nodes X_0 and X_{90} , X_{180} and X_{270} , V_0 and V_{90} , V_{180} and V_{270} , Y_0 and Y_{90} , Y_{180} and Y_{270} can be connected (Fig. A.6) without modifying the transfer function.

Furthermore, the connections of the in-phase capacitive and resistive dividers at nodes A and B can be opened, because there is no current flowing between the resistive and the capacitive 1 : 1 dividers. The complex low-pass resonator collapses to a single-opamp real low-pass resonator that is called the RCXX resonator and depicted in Fig. A.7.

¹ Assuming swing at the virtual ground due to non-ideal opamps.

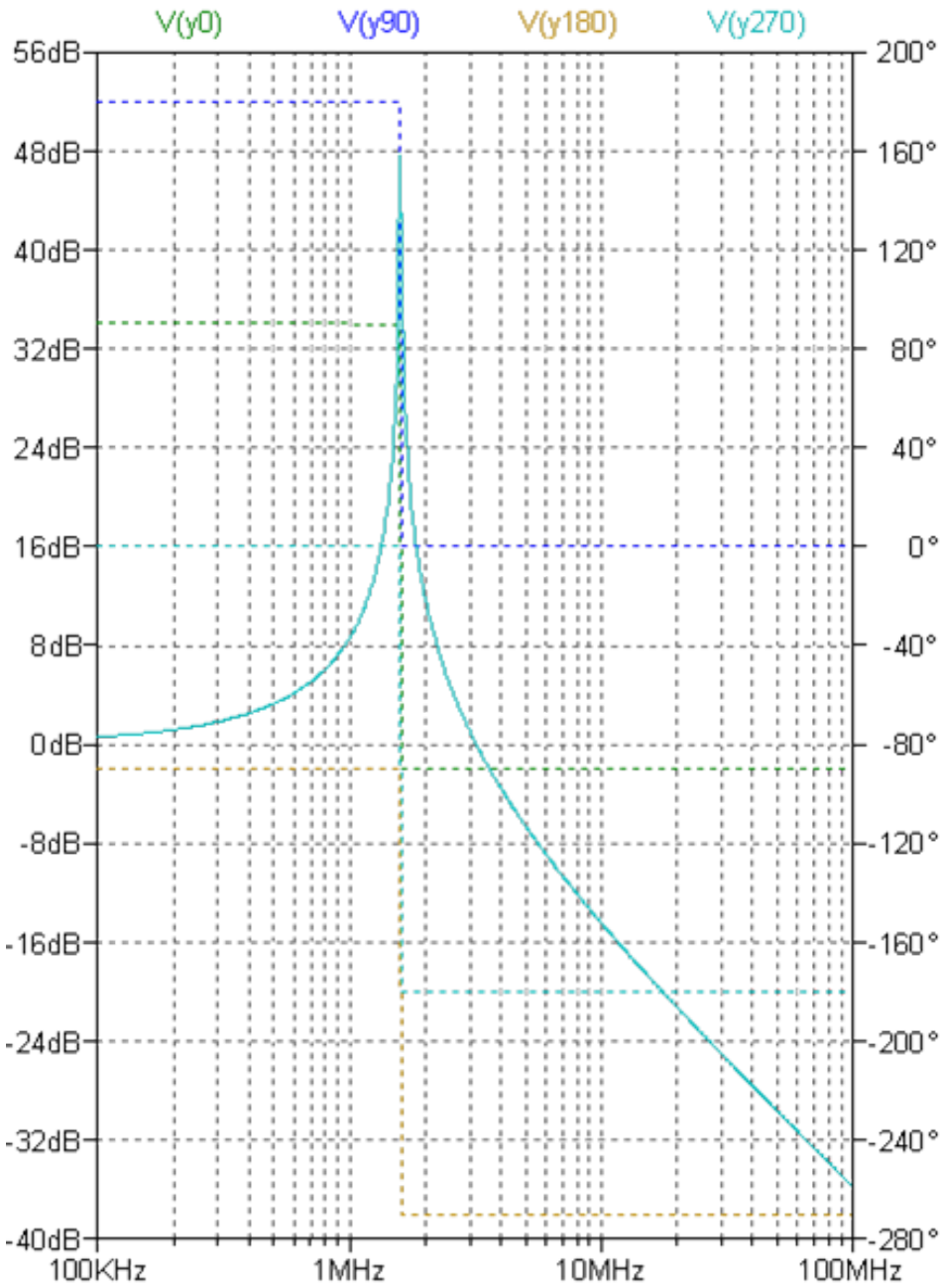


Figure A.2.: Polyphase active-RC resonator.

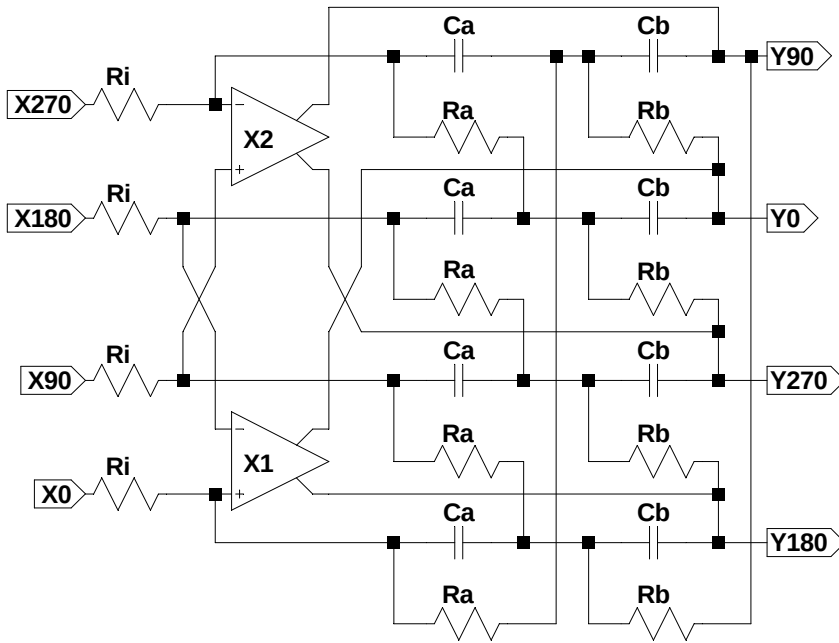


Figure A.3.: Multistage polyphase active-RC low-pass resonator.

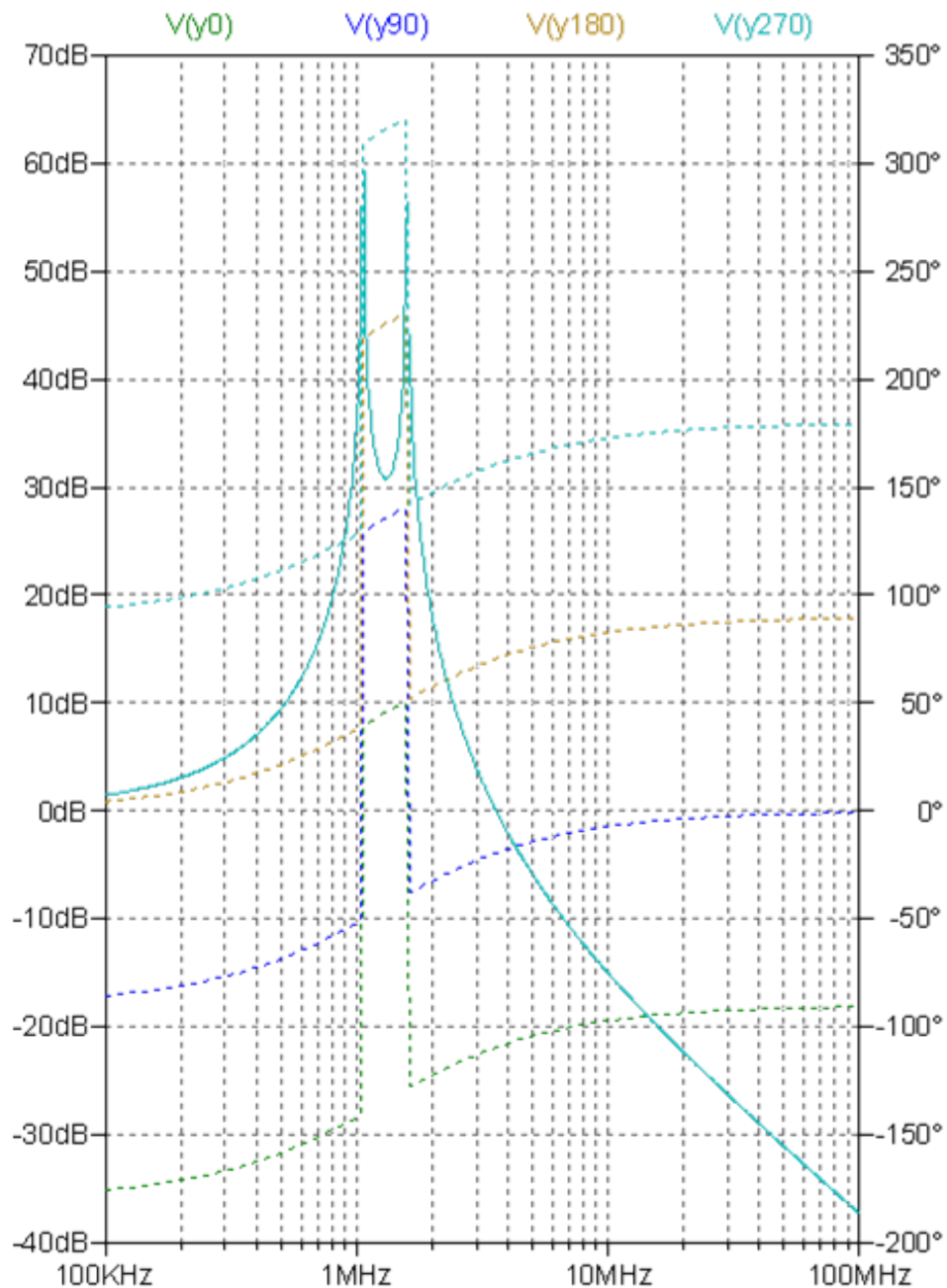


Figure A.4.: Multistage polyphase active-RC resonator.

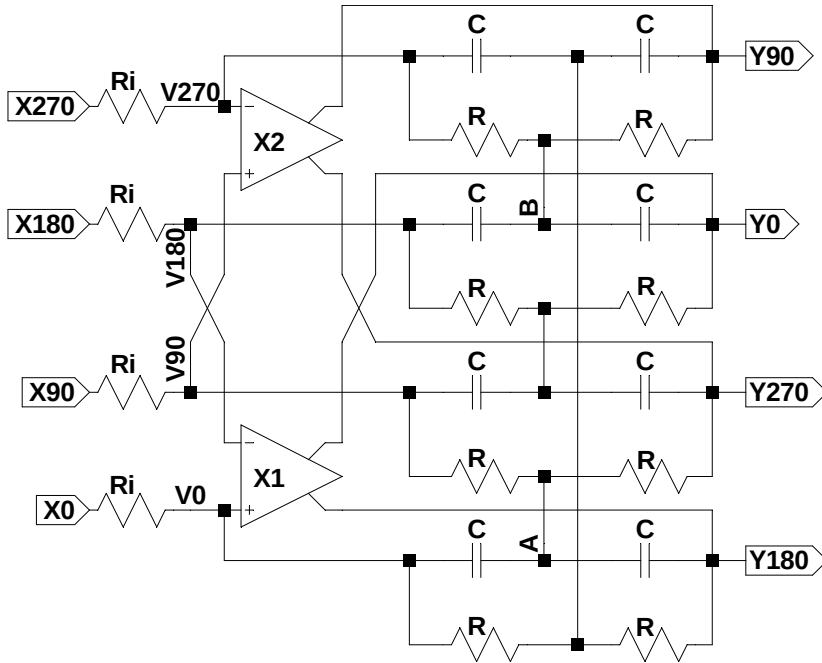


Figure A.5.: RCXX low-pass resonator before simplification.

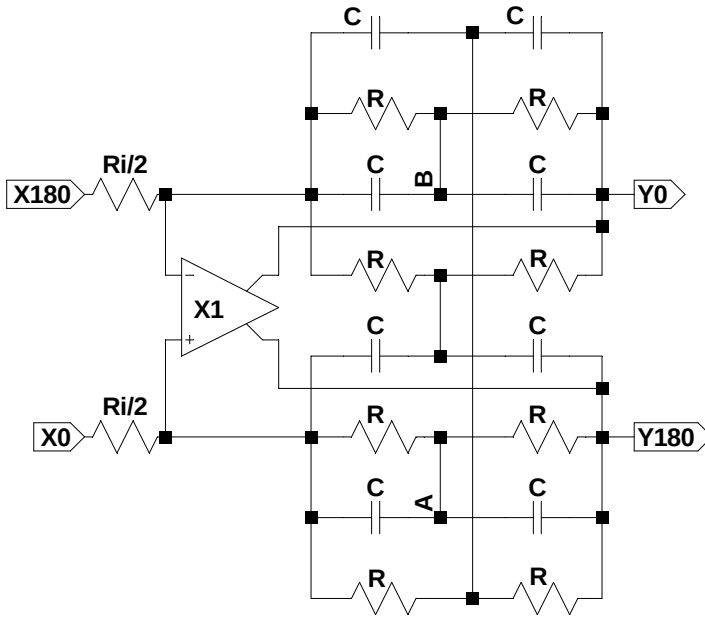


Figure A.6.: Real (non-complex) multistage polyphase active-RC resonator with connection of nodes that have same potentials.

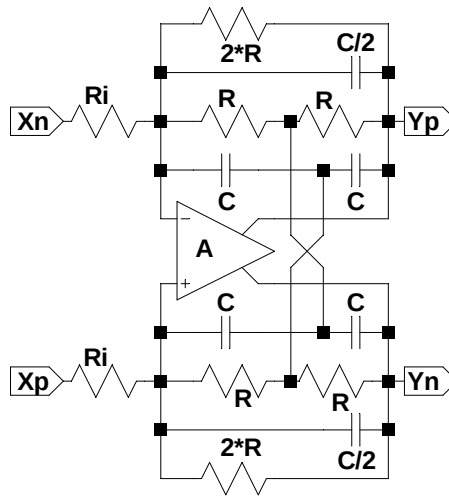


Figure A.7.: RCXX low-pass resonator after simplification.

A.2 Derivation of Cross-coupled Resonator from Twin-T Resonator

The T-networks in the Twin-T structure can be transformed into Π -networks using (A.2.1), i.e. the double-T becomes a double- Π structure.

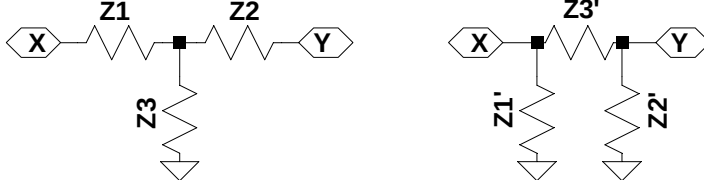


Figure A.8.: (a) T-network (b) Π -network.

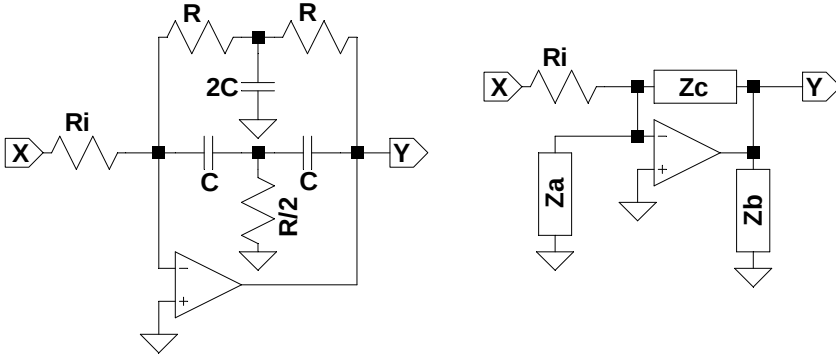


Figure A.9.: (a) Twin-T resonator (b) Π -transformed Twin-T resonator.

$$\begin{aligned} Z_1' &= (Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3) / Z_2, \\ Z_2' &= (Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3) / Z_1, \\ Z_3' &= (Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3) / Z_3. \end{aligned} \quad (\text{A.2.1})$$

The equivalent impedances in Fig. A.9 become

$$Z_a = Z_b = \frac{R}{2} + \frac{1}{2sC} \quad (\text{A.2.2})$$

and

$$Z_c = \frac{2sR^2C + 2R}{s^2R^2C^2 + 1} = \left(\frac{1}{2R} + \frac{sC}{2} + \left(-R - \frac{1}{sC} \right)^{-1} \right)^{-1}. \quad (\text{A.2.3})$$

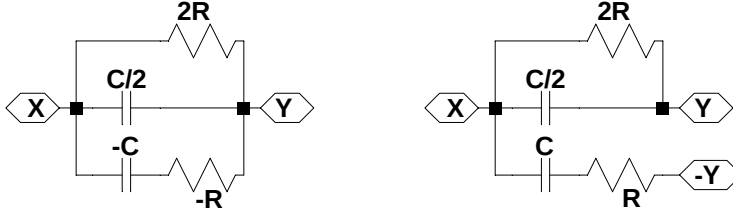


Figure A.10.: (a) Direct synthesis of Z_c , (b) with realization of negative components by coupling to negative terminal in differential circuit.

The impedances $Z_{a,b}$ can be omitted, because they are either connected between ground and virtual ground or represent only an additional load for the opamp. The impedance Z_c can be directly synthesized from (A.2.3) using the structures depicted in Fig. A.10. The negative resistance and capacitance respectively can be realized by cross-coupling in a differential structure.² The resulting structure is identical to the RCX resonator.

A.3 Second and Third Order Integrator with Generic Cross-coupled RC-Notch

The parameters for the transfer functions in Section 8.2 are

$$H_0(s) = 1 \quad (\text{A.3.1})$$

for the second order integrator,

$$H_0(s) = \frac{1}{sR_4C_4}, \quad (\text{A.3.2})$$

² This is possible because of the virtual ground and the zero output impedance of the ideal opamp.

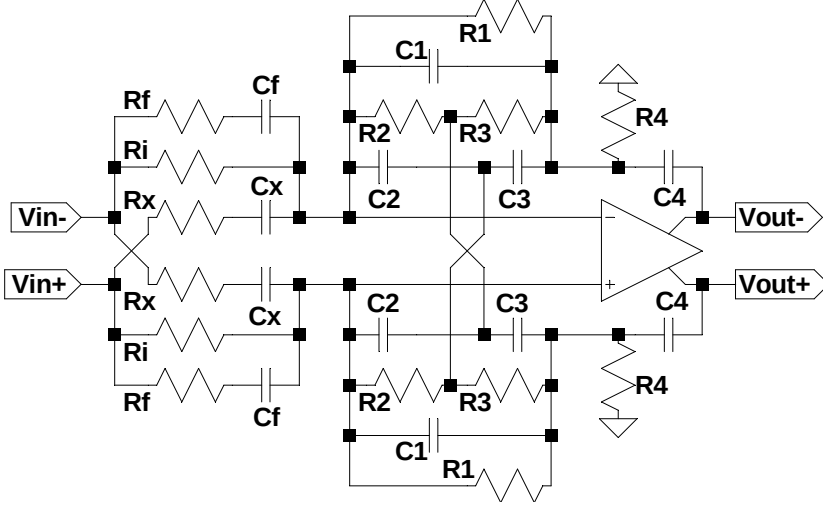


Figure A.11.: Resonant third order single-opamp integrator with generic cross-coupled RC-notch.

for the third order integrator and

$$R_0 = R_4 + \frac{R_1(R_2 + R_3)}{R_1 + R_2 + R_3} \quad (\text{A.3.3})$$

$$f_x = f_1 - \sqrt{f_1^2 - f_2^2}, \quad (\text{A.3.4})$$

$$f_f = f_1 + \sqrt{f_1^2 - f_2^2} \quad (\text{A.3.5})$$

with

$$f_1 = \frac{1}{2\pi} \frac{\frac{C_2+C_3}{2R_4} + \frac{2C_3+C_4}{2R_2} + \frac{2C_2+4C_3+C_4}{2R_3}}{C_1C_2 + C_1C_3 + C_2C_3 + C_2C_4 + C_3C_4}, \quad (\text{A.3.6})$$

$$f_2 = \frac{1}{2\pi} \sqrt{\frac{\frac{1}{R_1R_2} + \frac{1}{R_1R_3} + \frac{1}{R_2R_3} + \frac{1}{R_4R_2} + \frac{1}{R_4R_3}}{C_1C_2 + C_1C_3 + C_2C_3 + C_2C_4 + C_3C_4}}. \quad (\text{A.3.7})$$

A. Appendix

The generic expression in case the resonance condition (3.4.2) is not met becomes:

$$L_{diff}(s) = -H_0(s) \frac{R_4}{R_i} \left(1 + \frac{s^2 C_4 (C_2 + C_3) + s \left(\frac{C_2 + C_3}{R_4} + \frac{2C_3 + C_4}{R_2} + \frac{2C_2 + 4C_3 + C_4}{R_3} \right) + \frac{1}{R_4 R_2} + \frac{1}{R_4 R_3}}{s^2 (C_1 C_2 + C_1 C_3 + C_2 C_3) + s \left(\frac{C_1 - C_2}{R_3} + \frac{C_1 - C_3}{R_2} + \frac{C_2 + C_3}{R_1} \right) + \frac{1}{R_1 R_2} + \frac{1}{R_1 R_3} + \frac{1}{R_2 R_3}} \right) \quad (\text{A.3.8})$$

The expression for the peak gain (3.4.7) remains valid for this improved integrator, if $Z_{f0,3}$ in Tab. 3.1 is substituted with

$$Z_{f0,3}^* = R_4 + \frac{Z_{f0,3}}{1 + sC_4 Z_{f0,3}} \quad (\text{A.3.9})$$

in case of the second order integrator and with

$$Z_{f0,3}^* = \frac{1}{sC_4} + \frac{R_4 Z_{f0,3}}{R_4 + Z_{f0,3}} \quad (\text{A.3.10})$$

in case of the third order integrator respectively.

A.4 Analytic Common Mode Transfer Function

The analytical common mode transfer function of the second and third order integrator becomes:

$$L_{cm}(s) = \frac{-H_0(s) R_0 \left(\frac{s f_z}{2\pi f_f f_x} + 1 \right) \left(s^2 \frac{\frac{1}{R_i} - \frac{1}{R_x} + \frac{1}{R_f}}{(2\pi)^2 f_f f_x} + s \left(\frac{\frac{1}{R_i} - \frac{1}{R_x}}{2\pi f_x} + \frac{\frac{1}{R_i} + \frac{1}{R_f}}{2\pi f_f} \right) + \frac{1}{R_i} \right)}{\left(\frac{s}{2\pi f_f} + 1 \right) \left(\frac{s}{2\pi f_x} + 1 \right) \left(\frac{s f_z}{2\pi f_0^2} + 1 \right)} \quad (\text{A.4.1})$$

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Ever-increasing bandwidth demand, growing system complexity and cost pressure require to implement smart consumer devices with analog mixed signal systems on chip (SoCs) that are manufactured in state of the art ultra deep sub-micron (UDSM) CMOS semiconductor technologies. Continuous-time-sigma-delta-analog-to-digital converters (CT-SD-ADCs) have become an important interface building block of these SoCs as they provide an excellent compromise of dynamic range, bandwidth and power dissipation.

However, efforts to further reduce the area and power consumption of this class of data converters are needed for future mobile devices such as wearable computers and smart sensor interfaces for the internet of things that require a long battery lifetime and low production cost despite high complexity. Moreover, this improvement has to be achieved under steadily degrading properties of analog components due to shrinking feature size in digital CMOS technologies.

In this work, several novel design techniques that reduce the chip size and power consumption and improve the performance and clock jitter robustness of CT-SD-ADCs on architectural and transistor level are proposed with an emphasis on UDSM CMOS implementation.

Two testchips have been manufactured to prove these concepts: A robust mostly-analog ninth order and a mostly-digital third order single-bit CT-SD-ADC. Using a minimalistic active analog section that consists of only ten inverters, the second testchip is one of the most compact and power-efficient wideband CT-SD-ADCs published so far.

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